

HD74LV373A

Octal D-type Transparent Latches with 3-state Outputs

REJ03D0331-0200Z
 (Previous ADE-205-274 (Z))
 Rev.2.00
 Jun. 25, 2004

Description

The HD74LV373A has eight D type latches with three state outputs in a 20 pin package. When the latch enables input is high, the Q outputs will follow the D inputs. When the latch enables goes low, data at the D inputs will be retained at the outputs until latch enable returns high again. When a high logic level is applied to the output control input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements. Low-voltage and high-speed operation is suitable for the battery-powered products (e.g., notebook computers), and the low-power consumption extends the battery life.

Features

- $V_{CC} = 2.0\text{ V to }5.5\text{ V}$ operation
- All inputs $V_{IH} (\text{Max.}) = 5.5\text{ V}$ (@ $V_{CC} = 0\text{ V to }5.5\text{ V}$)
- All outputs $V_O (\text{Max.}) = 5.5\text{ V}$ (@ $V_{CC} = 0\text{ V}$)
- Typical V_{OL} ground bounce $< 0.8\text{ V}$ (@ $V_{CC} = 3.3\text{ V}$, $T_a = 25^\circ\text{C}$)
- Typical V_{OH} undershoot $> 2.3\text{ V}$ (@ $V_{CC} = 3.3\text{ V}$, $T_a = 25^\circ\text{C}$)
- Output current $\pm 8\text{ mA}$ (@ $V_{CC} = 3.0\text{ V to }3.6\text{ V}$), $\pm 16\text{ mA}$ (@ $V_{CC} = 4.5\text{ V to }5.5\text{ V}$)
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LV373AFPEL	SOP-20 pin (JEITA)	FP-20DAV	FP	EL (2,000 pcs/reel)
HD74LV373ARPEL	SOP-20 pin (JEDEC)	FP-20DBV	RP	EL (1,000 pcs/reel)
HD74LV373ATELL	TSSOP-20 pin	TTP-20DAV	T	ELL (2,000 pcs/reel)

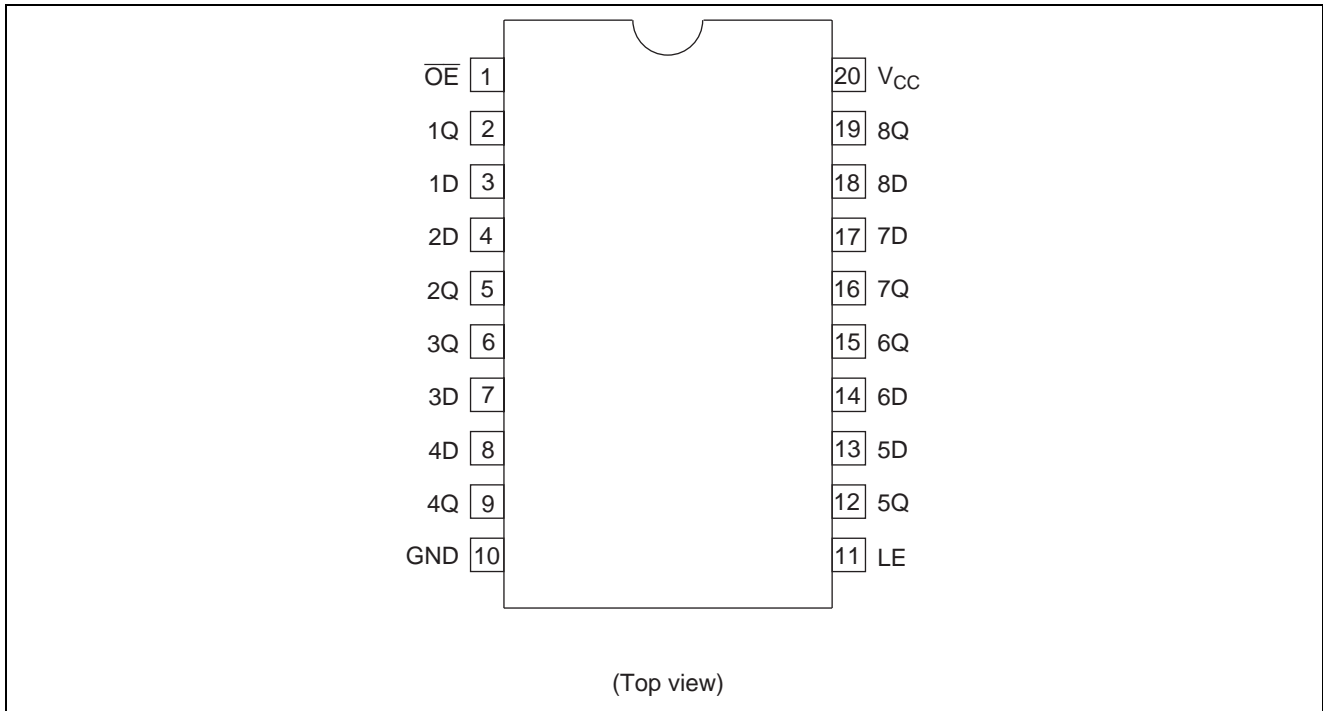
Note: Please consult the sales office for the above package availability.

Function Table

Inputs				Output Q
\overline{OE}	LE	D		
H	X	X	Z	
L	H	L	L	
L	H	H	H	
L	L	X	Q_0	

Note: H: High level
 L: Low level
 X: Immaterial
 Z: High impedance
 Q_0 : Output level before the indicated steady state input conditions were established.

Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	V_{CC}	-0.5 to 7.0	V	
Input voltage range ^{*1}	V_I	-0.5 to 7.0	V	
Output voltage range ^{*1,2}	V_O	-0.5 to $V_{CC} + 0.5$ -0.5 to 7.0	V	Output: H or L V_{CC} : OFF or Output: Z
Input clamp current	I_{IK}	-20	mA	$V_I < 0$
Output clamp current	I_{OK}	±50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	I_O	±35	mA	$V_O = 0$ to V_{CC}
Continuous current through V_{CC} or GND	I_{CC} or I_{GND}	±70	mA	
Maximum power dissipation at $T_a = 25^\circ\text{C}$ (in still air) ^{*3}	P_T	835 757	mW	SOP TSSOP
Storage temperature	T_{stg}	-65 to 150	°C	

Notes: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

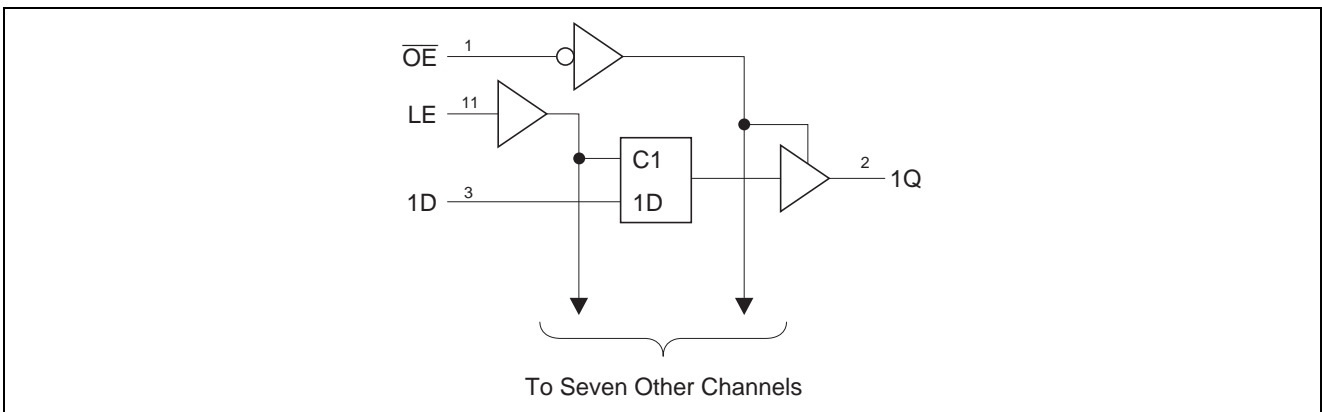
1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The maximum package power dissipation was calculated using a junction temperature of 150°C.

Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	V_{CC}	2.0	5.5	V	
Input voltage range	V_I	0	5.5	V	
Output voltage range	V_O	0	V_{CC}	V	H or L
		0	5.5		High impedance state
Output current	I_{OH}	—	-50	μA	$V_{CC} = 2.0 V$
		—	-2	mA	$V_{CC} = 2.3 \text{ to } 2.7 V$
		—	-8		$V_{CC} = 3.0 \text{ to } 3.6 V$
		—	-16	$V_{CC} = 4.5 \text{ to } 5.5 V$	
	I_{OL}	—	50	μA	$V_{CC} = 2.0 V$
		—	2	mA	$V_{CC} = 2.3 \text{ to } 2.7 V$
		—	8		$V_{CC} = 3.0 \text{ to } 3.6 V$
		—	16	$V_{CC} = 4.5 \text{ to } 5.5 V$	
Input transition rise or fall rate	$\Delta t / \Delta v$	0	200	ns/V	$V_{CC} = 2.3 \text{ to } 2.7 V$
		0	100		$V_{CC} = 3.0 \text{ to } 3.6 V$
		0	20		$V_{CC} = 4.5 \text{ to } 5.5 V$
Operating free-air temperature	T_a	-40	85	$^{\circ}C$	

Note: Unused or floating inputs must be held high or low.

Logic Diagram



DC Electrical Characteristics

Ta = -40 to 85°C

Item	Symbol	V _{CC} (V)*	Min	Typ	Max	Unit	Test Conditions		
Input voltage	V _{IH}	2.0	1.5	—	—	V			
		2.3 to 2.7	V _{CC} × 0.7	—	—				
		3.0 to 3.6	V _{CC} × 0.7	—	—				
		4.5 to 5.5	V _{CC} × 0.7	—	—				
	V _{IL}	2.0	—	—	0.5				
		2.3 to 2.7	—	—	V _{CC} × 0.3				
		3.0 to 3.6	—	—	V _{CC} × 0.3				
		4.5 to 5.5	—	—	V _{CC} × 0.3				
Output voltage	V _{OH}	Min to Max	V _{CC} - 0.1	—	—	V	I _{OH} = -50 μA		
		2.3	2.0	—	—		I _{OH} = -2 mA		
		3.0	2.48	—	—		I _{OH} = -8 mA		
		4.5	3.8	—	—		I _{OH} = -16 mA		
	V _{OL}	Min to Max	—	—	0.1		I _{OL} = 50 μA		
		2.3	—	—	0.4		I _{OL} = 2 mA		
		3.0	—	—	0.44		I _{OL} = 8 mA		
		4.5	—	—	0.55		I _{OL} = 16 mA		
	Input current	I _{IN}	0 to 5.5	—	—		±1	μA	V _{IN} = 5.5 V or GND
	Off-state output current	I _{OZ}	5.5	—	—		±5	μA	V _O = V _{CC} or GND
Quiescent supply current	I _{CC}	5.5	—	—	20	μA	V _{IN} = V _{CC} or GND, I _O = 0		
Output leakage current	I _{OFF}	0	—	—	5	μA	V _I or V _O = 0 to 5.5 V		
Input capacitance	C _{IN}	3.3	—	2.9	—	pF	V _I = V _{CC} or GND		

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Switching Characteristics

V_{CC} = 2.5 ± 0.2 V

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	t _{PLH}	—	8.3	15.2	1.0	17.0	ns	C _L = 15 pF	D	Q
	t _{PHL}	—	9.1	15.7	1.0	19.0			LE	
		—	10.4	18.0	1.0	21.0		C _L = 50 pF	D	
		—	11.1	18.6	1.0	22.0			LE	
Enable time	t _{ZH}	—	8.9	15.8	1.0	19.0	ns	C _L = 15 pF C _L = 50 pF	OE	Q
	t _{ZL}	—	10.9	18.8	1.0	22.0				
Disable time	t _{HZ}	—	6.2	12.6	1.0	15.0	ns	C _L = 15 pF C _L = 50 pF	OE	Q
	t _{LZ}	—	8.3	17.4	1.0	19.0				
Setup time	t _{SU}	4.5	—	—	5.0	—	ns		Data before LE ↓	
Hold time	t _H	1.5	—	—	1.5	—	ns		Data after LE ↓	
Pulse width	t _w	6.0	—	—	6.5	—	ns		LE "H"	

V_{CC} = 3.3 ± 0.3 V

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	t _{PLH}	—	5.8	11.4	1.0	13.5	ns	C _L = 15 pF	D	Q
	t _{PHL}	—	6.4	11.0	1.0	13.0			LE	
		—	7.3	14.9	1.0	17.0		C _L = 50 pF	D	
		—	7.8	14.5	1.0	16.5			LE	
Enable time	t _{ZH}	—	6.3	11.4	1.0	13.5	ns	C _L = 15 pF C _L = 50 pF	OE	Q
	t _{ZL}	—	7.7	14.9	1.0	17.0				
Disable time	t _{HZ}	—	4.7	10.0	1.0	12.0	ns	C _L = 15 pF C _L = 50 pF	OE	Q
	t _{LZ}	—	6.0	13.2	1.0	15.0				
Setup time	t _{SU}	4.0	—	—	4.0	—	ns		Data before LE ↓	
Hold time	t _H	1.0	—	—	1.0	—	ns		Data after LE ↓	
Pulse width	t _w	5.0	—	—	5.0	—	ns		LE "H"	

V_{CC} = 5.0 ± 0.5 V

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	t _{PLH}	—	4.1	7.2	1.0	8.5	ns	C _L = 15 pF	D	Q
	t _{PHL}	—	4.5	7.2	1.0	8.5			LE	
		—	5.1	9.2	1.0	10.5		C _L = 50 pF	D	
		—	5.5	9.2	1.0	10.5			LE	
Enable time	t _{ZH}	—	4.5	8.1	1.0	9.5	ns	C _L = 15 pF C _L = 50 pF	OE	Q
	t _{ZL}	—	5.5	10.1	1.0	11.5				
Disable time	t _{HZ}	—	3.3	7.2	1.0	8.5	ns	C _L = 15 pF C _L = 50 pF	OE	Q
	t _{LZ}	—	4.0	9.2	1.0	10.5				
Setup time	t _{SU}	4.0	—	—	4.0	—	ns		Data before LE ↓	
Hold time	t _H	1.0	—	—	1.0	—	ns		Data after LE ↓	
Pulse width	t _w	5.0	—	—	5.0	—	ns		LE "H"	

Output-skew Characteristics

$C_L = 50 \text{ pF}$

Item	Symbol	$V_{CC} = (V)$	$T_a = 25^\circ\text{C}$		$T_a = -40 \text{ to } 85^\circ\text{C}$		Unit
			Min	Max	Min	Max	
Output skew	$t_{sk(O)}$	2.3 to 2.7	—	2.0	—	2.0	ns
		3.0 to 3.6	—	1.5	—	1.5	
		4.5 to 5.5	—	1.0	—	1.0	

Note: Skew between any outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

Operating Characteristics

$C_L = 50 \text{ pF}$

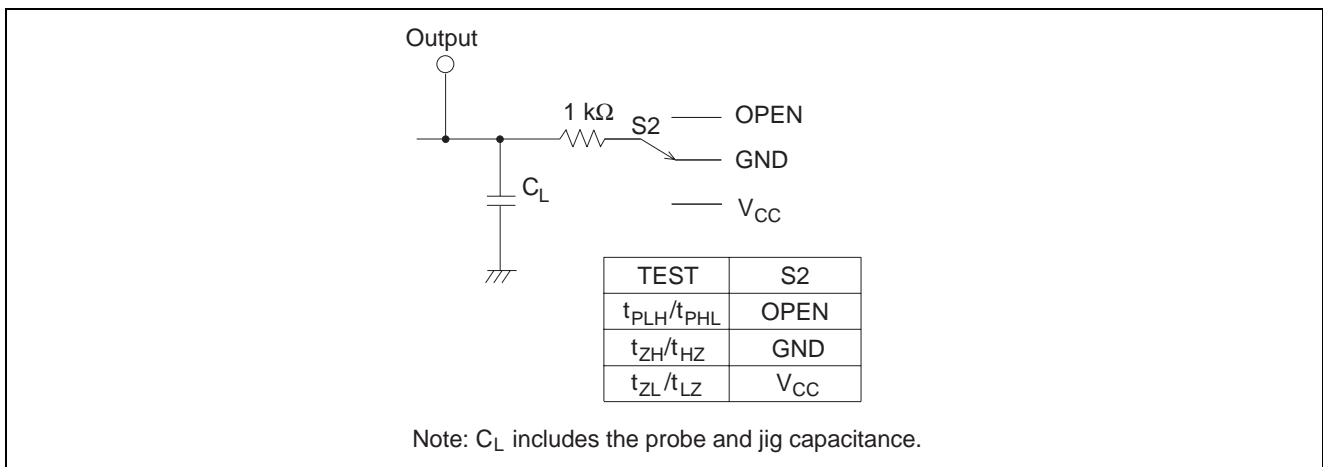
Item	Symbol	$V_{CC} = (V)$	$T_a = 25^\circ\text{C}$			Unit	Test Conditions
			Min	Typ	Max		
Power dissipation capacitance	C_{PD}	3.3	—	16.6	—	pF	$f = 10 \text{ MHz}$
		5.0	—	18.2	—		

Noise Characteristics

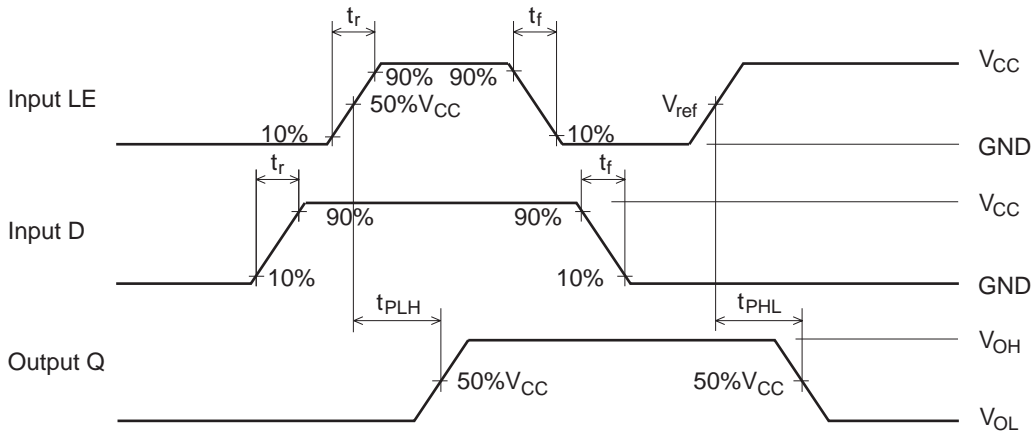
$C_L = 50 \text{ pF}$

Item	Symbol	$V_{CC} = (V)$	$T_a = 25^\circ\text{C}$			Unit	Test Conditions
			Min	Typ	Max		
Quiet output, maximum dynamic V_{OL}	$V_{OL(P)}$	3.3	—	0.6	0.8	V	
Quiet output, minimum dynamic V_{OL}	$V_{OL(V)}$	3.3	—	-0.6	-0.8	V	
Quiet output, minimum dynamic V_{OH}	$V_{OH(V)}$	3.3	—	2.9	—	V	
High-level dynamic input voltage	$V_{IH(D)}$	3.3	2.31	—	—	V	
Low-level dynamic input voltage	$V_{IL(D)}$	3.3	—	—	0.99	V	

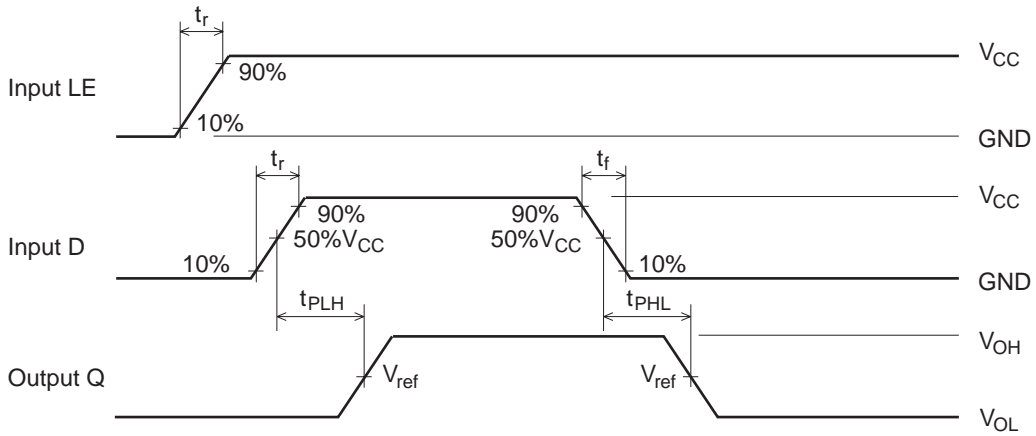
Test Circuit



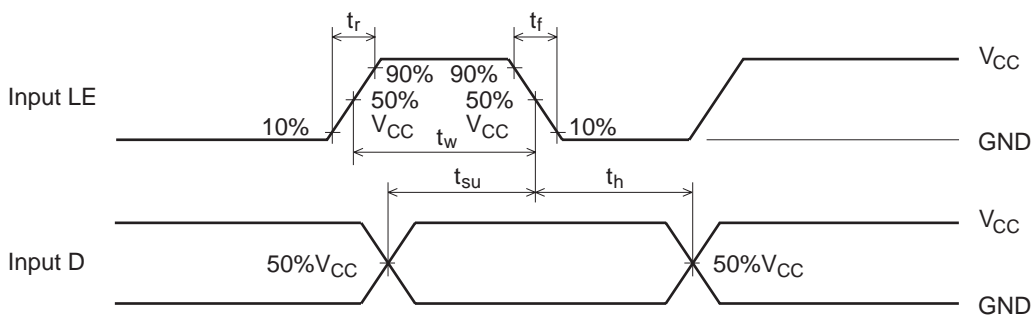
• Waveform – 1



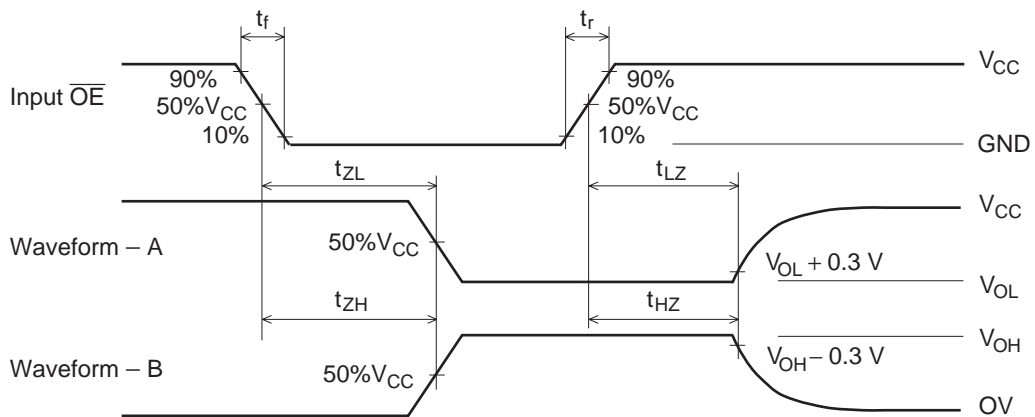
• Waveform – 2



• Waveform – 3

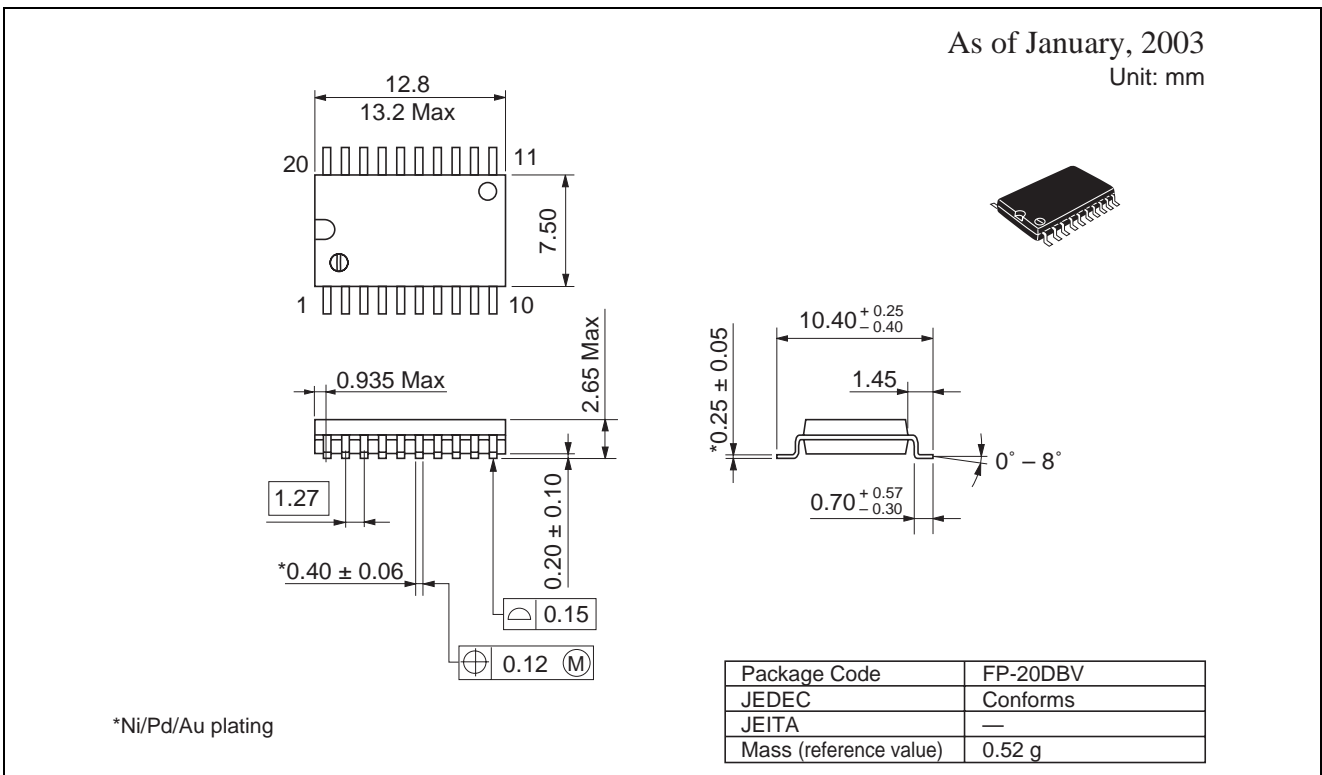
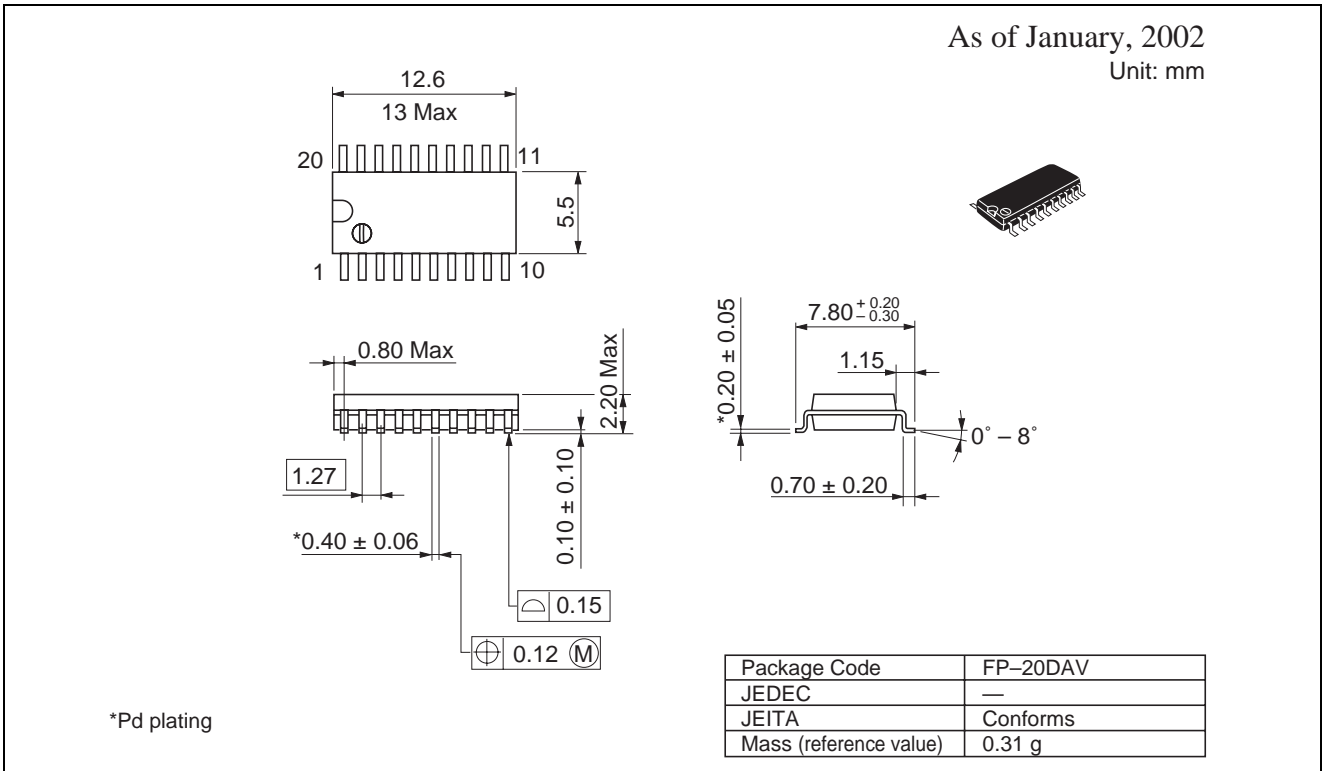


• Waveform – 4

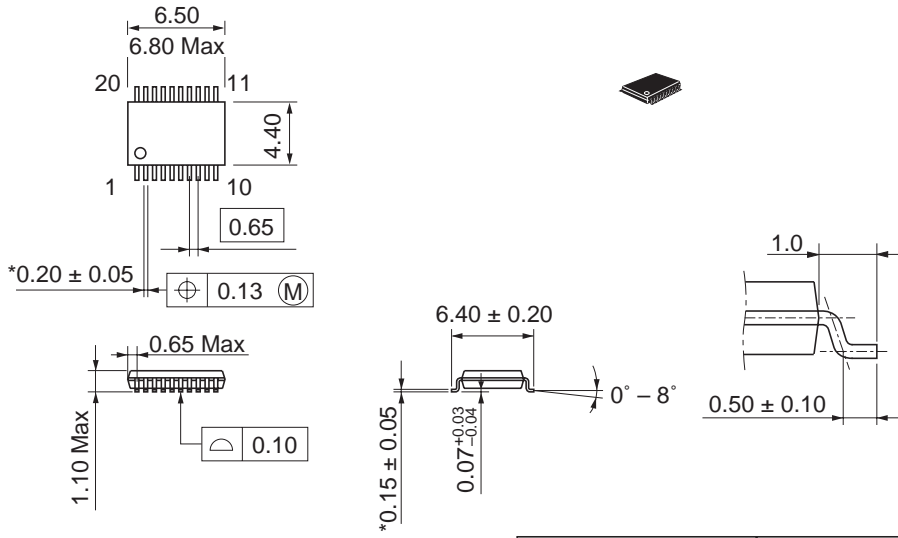


- Notes:
1. $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$
 2. Input waveform: PRR $\leq 1 \text{ MHz}$, duty cycle 50%
 3. Waveform-A is for an output with internal conditions such that the output is low except when disabled by the output control.
 4. Waveform-B is for an output with internal conditions such that the output is high except when disabled by the output control.

Package Dimensions



As of January, 2002
Unit: mm



*Pd plating

Package Code	TTP-20DAV
JEDEC	—
JEITA	—
Mass (reference value)	0.07 g

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