



CTH8003PS-T52

P-Channel Enhancement MOSFET

Features

- Drain-Source Breakdown Voltage $V_{DS} = -30V$
- Drain-Source On-Resistance
 $R_{DS(ON)} 6.7m\Omega$, at $V_{GS} = -10V$, $I_D = -20A$
 $R_{DS(ON)} 8.4m\Omega$, at $V_{GS} = -4.5V$, $I_D = -20A$
- Continuous Drain Current at $T_C = 25^\circ C$ $I_D = -80A$
- Advanced high cell density Trench Technology
- RoHS Compliance & Halogen Free

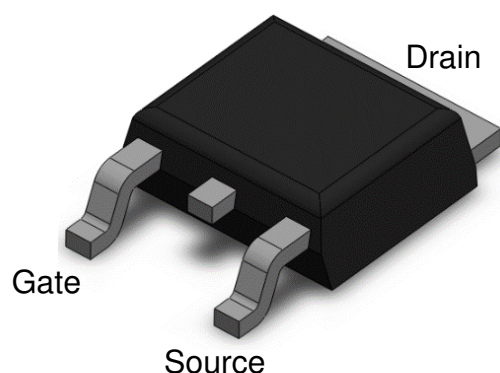
Description

The CTH8003PS-T52 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

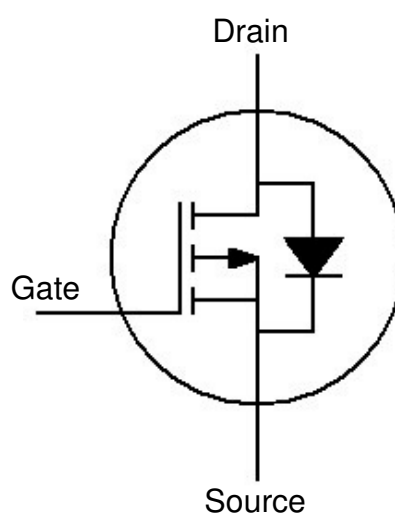
Applications

- Load Switch
- DC/DC Converter
- LCD Display inverter

Package Outline



Schematic





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Absolute Maximum Rating at 25°C

Symbol	Parameters	Test Conditions	Min	Note
V _{DS}	Drain-Source Voltage	-30	V	
V _{GS}	Gate-Source Voltage	±20	V	
I _D	Continuous Drain Current @T _C =25°C	-80	A	1
I _{DM}	Pulsed Drain Current	-200	A	1
P _D	Total Power Dissipation @T _C =25°C	83	W	2
T _{STG}	Storage Temperature Range	-55 to 150	°C	
T _J	Operating Junction Temperature Range	-55 to 150	°C	

Thermal Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
R _{θJC}	Thermal Resistance Junction-Case		--	--	1.5	°C /W	1,4

**CTH8003PS-T52****P-Channel Enhancement MOSFET****Electrical Characteristics** $T_A = 25^\circ\text{C}$ (unless otherwise specified)**Static Characteristics**

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
$B_{V_{DS}}$	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = -250\mu A$	-30	-	-	V	
I_{DSS}	Drain-Source Leakage Current	$V_{DS} = -30V, V_{GS} = 0V$	-	-	-1	μA	
I_{GSS}	Gate-Source Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$	-	-	± 100	nA	

On Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
$R_{DS(ON)}$	Drain-Source On-Resistance	$V_{GS} = -10V, I_D = -20A$	-	6.7	8	m Ω	3
		$V_{GS} = -4.5V, I_D = -20A$	-	8.4	11	m Ω	3
$V_{GS(th)}$	Gate-Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250\mu A$	-1.0	-	-3.0	V	3

Dynamic Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
C_{ISS}	Input Capacitance	$V_{GS} = 0V,$ $V_{DS} = -15V$ $f = 1MHz$	-	3650	-	pF	
C_{OSS}	Output Capacitance		-	485	-		
C_{RSS}	Reverse Transfer Capacitance		-	165	-		

Switching Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
$T_{D(ON)}$	Turn-On Delay Time	$V_{DS} = -15V, R_L = 15\Omega,$ $V_{GS} = -10V, R_G = 6\Omega,$ $I_D = -1A$	-	48	-	ns	
T_R	Rise Time		-	20	-		
$T_{D(OFF)}$	Turn-Off Delay Time		-	170	-		
T_F	Fall Time		-	55	-		
Q_G	Total Gate Charge	$V_{DS} = -15V,$ $V_{GS} = -4.5V,$ $I_D = 20A$	-	44	-	nC	
Q_{GS}	Gate-Source Charge		-	12.5	-		
Q_{GD}	Gate-Drain (Miller) Charge		-	19.5	-		



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Drain-Source Diode Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
V_{SD}	Body Diode Forward Voltage	$V_{GS} = 0V, I_{SD} = -1A$	-	-0.7	-1.2	V	1
I_{SD}	Body Diode Continuous Current		-	-	-1.0	A	1

Note:

1. The power dissipation is limited by 150°C junction temperature.
2. The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
3. Thermal Resistance follow JESD51-3.



Typical Characteristic Curves

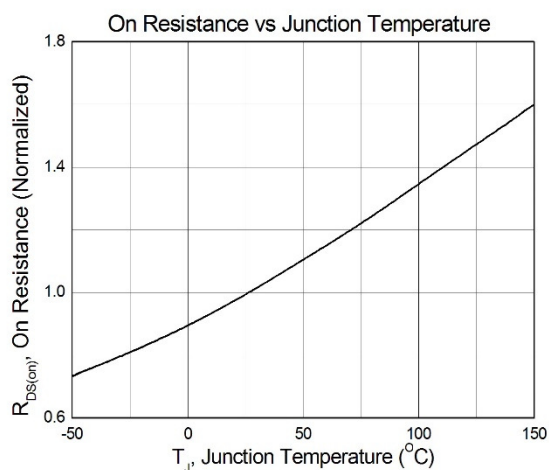


Figure 1

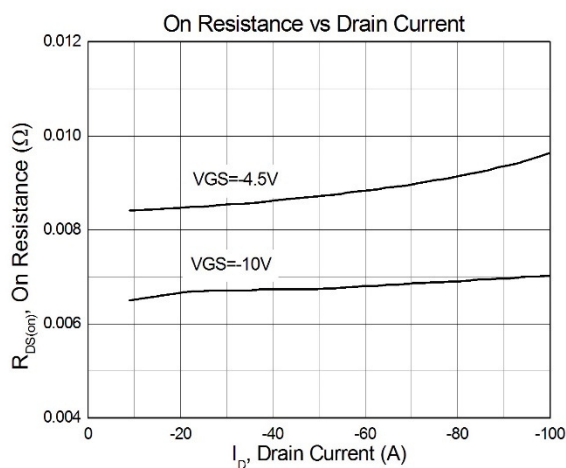


Figure 2

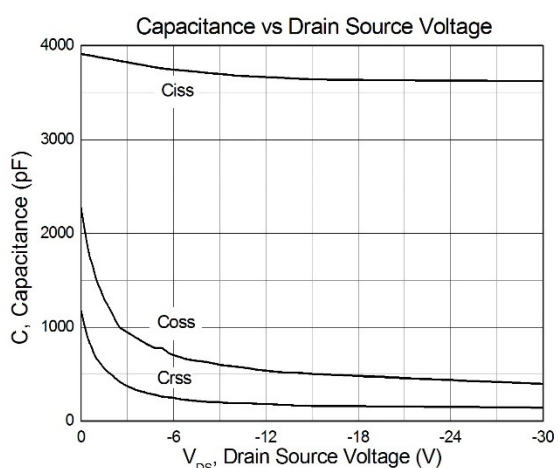


Figure 3

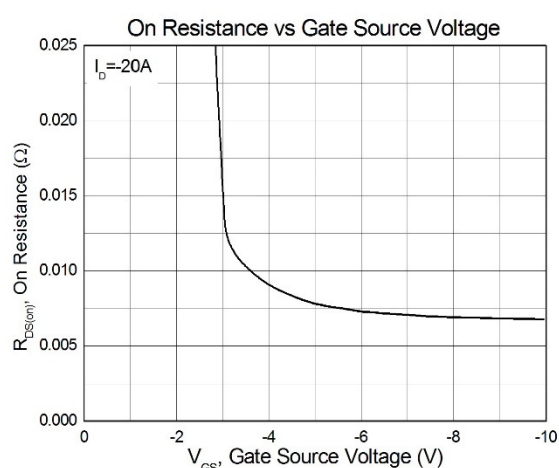


Figure 4

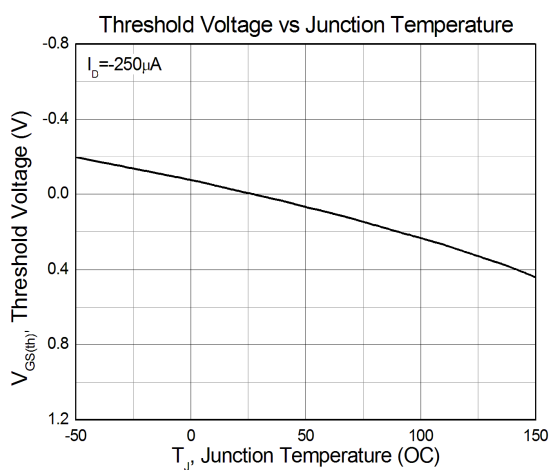


Figure 5

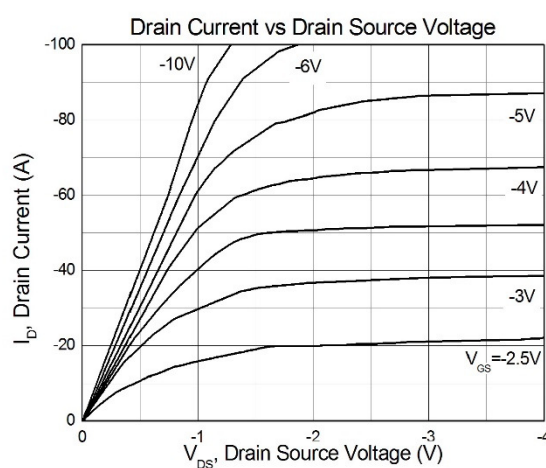


Figure 6

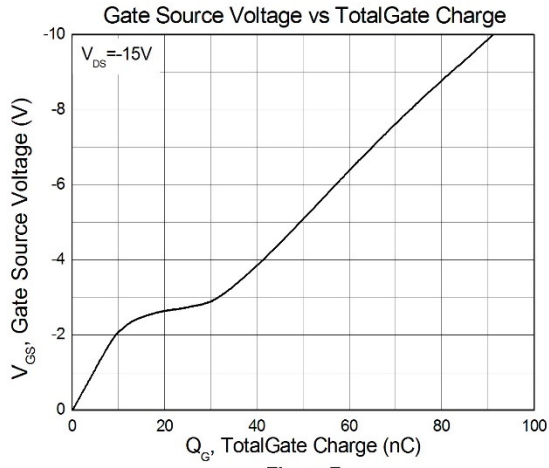


Figure 7

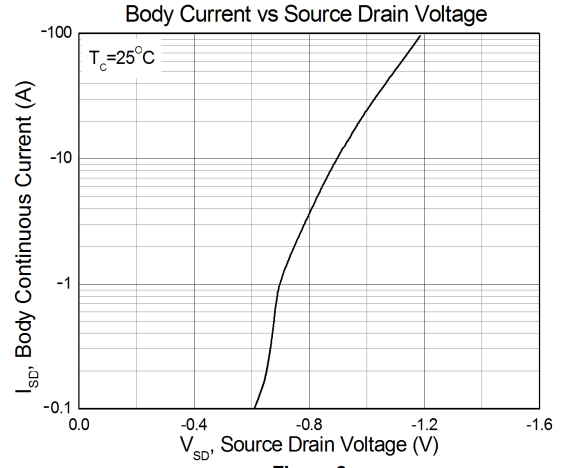


Figure 8



Test Circuits & Waveforms

Figure 9: Gate Charge Test Circuit

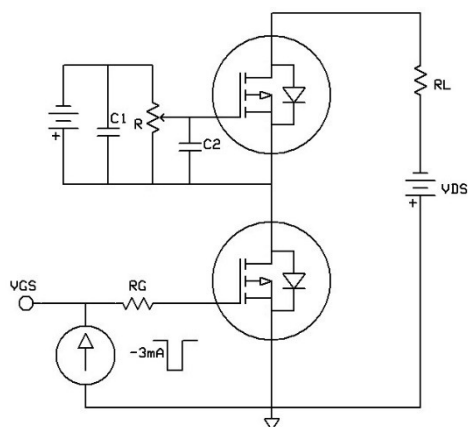


Figure 10: Gate Charge Waveform

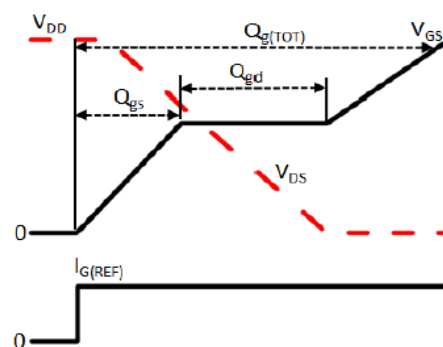


Figure 11: Switching Time Test Circuit

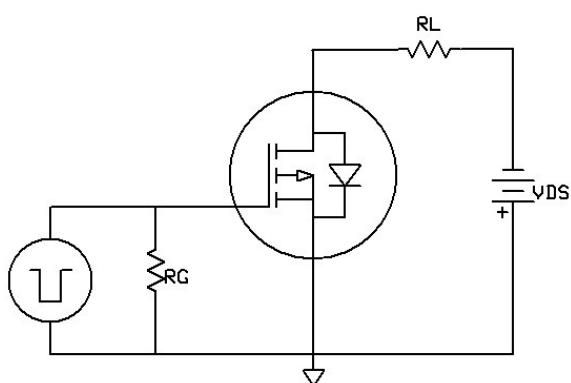
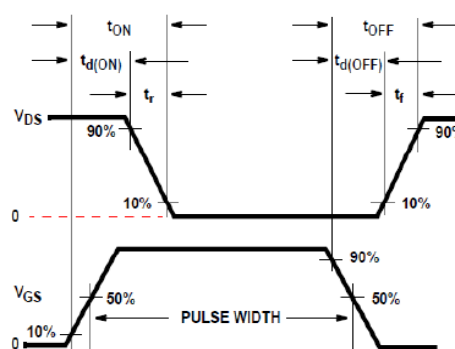
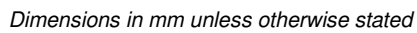


Figure 12: Switching Time Waveform





Package Dimension (TO-252)



Dimensions in mm unless otherwise stated

CTH8003PS-T52

Channel Enhancement MOSFET

CT : Denotes “ CT M
H8003P : Device Number
Y : Fiscal Year
WW : Work Week
A : Production Code

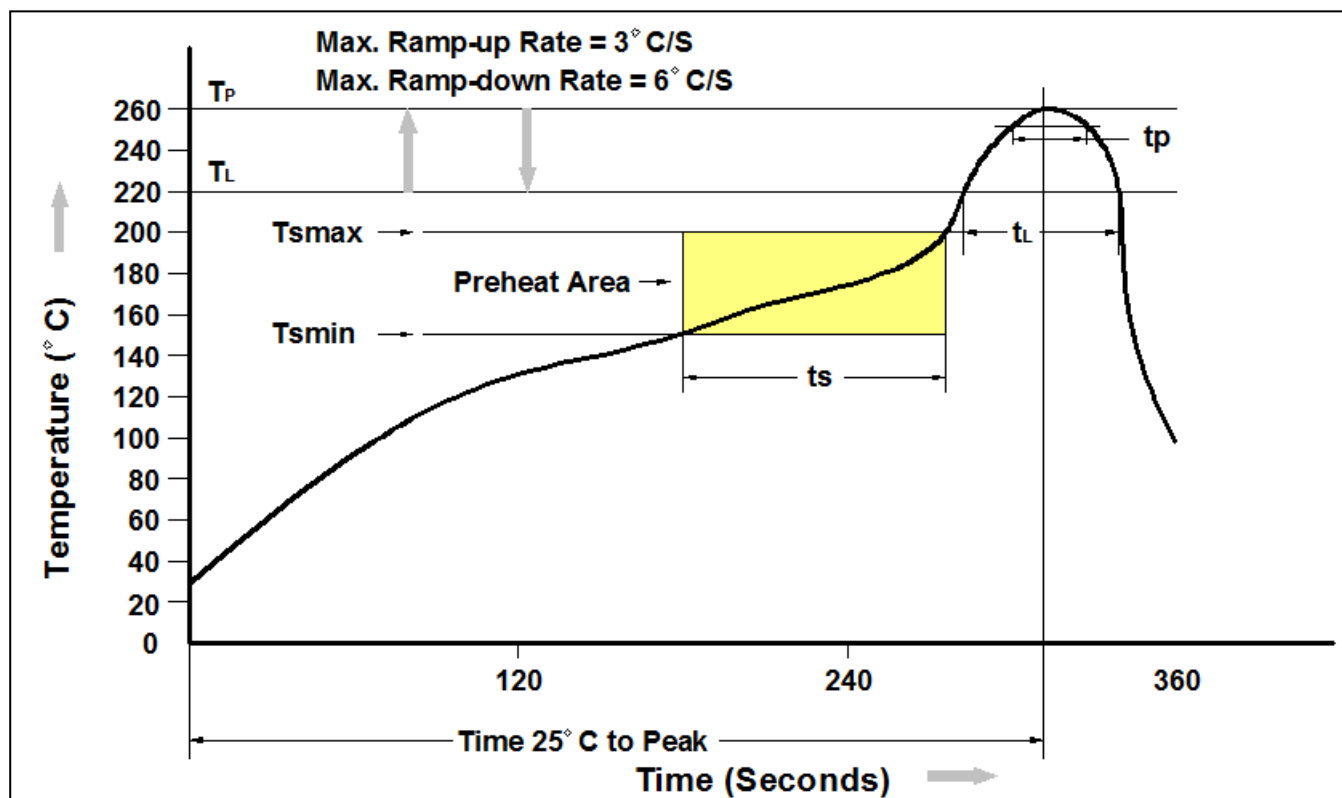
CT
H8003P
YWWA

Ordering Information

Part Number	Description	Quantity
CTH8003PS-T52	TO-252 Reel	2500 pcs



Reflow Profile



Profile Feature	Pb-Free Assembly Profile
Temperature Min. (T _{min})	150 °C
Temperature Max. (T _{max})	200 °C
Time (t _s) from (T _{min} to T _{max})	60-120 seconds
Ramp-up Rate (t _L to t _P)	3°C/second max.
Liquidous Temperature (T _L)	217 °C
Time (t _L) Maintained Above (T _L)	60 – 150 seconds
Peak Body Package Temperature	260 °C +0 °C / -5 °C
Time (t _P) within 5 °C of 260 °C	30 seconds
Ramp-down Rate (T _P to T _L)	6°C/second max
Time 25 °C to Peak Temperature	8 minutes max.



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