ASM3P2508A

Product Preview
Peak EMI Reducing Solution

Description

The ASM3P2508A is a versatile spread spectrum frequency modulator. The ASM3P2508A reduces electromagnetic interference (EMI) at the clock source. The ASM3P2508A allows significant system cost savings by reducing the number of circuit board layers and shielding that are required to pass EMI regulations. The ASM3P2508A modulates the output of PLL in order to spread the bandwidth of a synthesized clock, thereby decreasing the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most clock generators. Lowering EMI by increasing a signal's bandwidth is called spread spectrum clock generation.

The ASM3P2508A has a feature to power down the 72 MHz / 48 MHz output by writing data into specific registers in the device via I2C. By writing a '0' into bit 1 of Byte 0, the PLL block generating 72 MHz / 48 MHz can be powered down. Writing '0' into bit '7' of Byte 1 selects an output of 72 MHz on FOUT2CLK while a '1' at the same location selects a 48 MHz clock output. However, the I2C block, crystal oscillator, and the PLL block generating 120 MHz would be always running.

Features

- Generates an EMI Optimized Clocking Signal at Output
- Input Frequency − 14.31818 MHz
- Frequency Outputs:
  - 120 MHz (modulated) − Default
  - 72 MHz (modulated) or 48 MHz (modulated) Selectable via I2C
- ±1% Centre Spread
- Modulation Rate: 40 KHz
- Byte Write via I2C
- Supply Voltage Range 3.3 V ± 0.3 V
- Available in 8−pin SOIC Package
- Available in Commercial and Industrial
- Temperature Ranges
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

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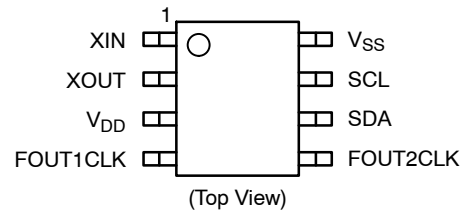
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http://onsemi.com

SOIC−8
S SUFFIX
CASE 751BD

PIN CONFIGURATION

XIN		V_{SS}
XOUT		SCL
V_{DD}		SDA
FOUT1CLK		FOUT2CLK

(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.
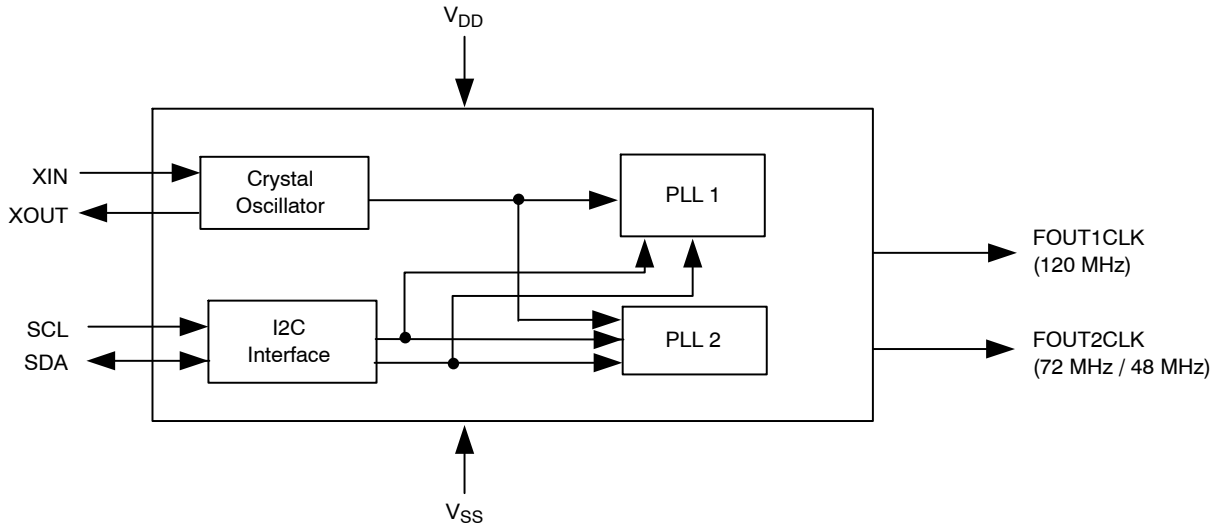
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Figure 1. Block Diagram

Table 1. PIN DESCRIPTION

Pin Name	Type	Description
XIN	I	Connection to crystal
XOUT	O	Connection to crystal
V_{DD}	P	Power supply for the analog and digital blocks
FOUT1CLK	O	Clock output−1 (120 MHz) – default
FOUT2CLK	O	Clock output−2 (72 MHz / 48 MHz)
SDA	I/O	I2C Data
SCL	I	I2C Clock
V_{SS}	P	Ground to entire chip

Table 2. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to Ground	−0.5 to +4.6	V
T_{STG}	Storage temperature	−40 to +85	°C
T_A	Operating temperature	0 to 70	°C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22− A114−B)	2	KV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. OPERATING CONDITIONS

Symbol	Parameter	Condition / Description	Min	Typ	Max	Unit
V_{DD}	Supply Voltage	3.3 V ± 10%	3	3.3	3.6	V
T_A	Ambient Operating Temperature Range		−10		+70	°C
F_{XIN}	Crystal Resonator Frequency			14.31818		MHz
	Serial Data Transfer Rate	Standard Mode	10		100	Kb/s
C_L	Output Driver Load Capacitance				15	pF

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Table 4. DC ELECTRICAL CHARACTERISTICS

(Test Condition: All the parameters are measured at room temperature (25°C), unless otherwise stated.)

Parameter	Symbol	Conditions / Description	Min	Typ	Max	Unit
OVERALL						
Supply Current, Dynamic	I_{cc}	V_{DD} = 3.3 V, F_{CLK} = 14.31818 MHz, C_L = 15 pF	40	49	60	mA
Supply Current, Static	I_{DD}	V_{DD} = 3.3 V, Software Power Down (Note 1)	27	35	43	mA
ALL INPUT PINS						
High–Level Input Voltage	V_{IH}	V_{DD} = 3.3 V	2.0	–	V_{DD}+0.3	V
Low–Level Input Voltage	V_{IL}	V_{DD} = 3.3 V	V_{SS}–0.3	–	0.8	V
High–Level Input Current	I_{IH}		–1	–	1	μA
Low–Level Input Current (pull–up)	I_{IL}		–20	–36	–80	μA
CLOCK OUTPUTS (FOUT1CLK, FOUT2CLK)						
High–Level Output Voltage	V_{OH}	V_{DD} = 3.3 V, I_{OH} = 20 mA	2.5	–	3.3	V
Low–Level Output Voltage	V_{OL}	V_{DD} = 3.3 V, I_{OL} = 20 mA	0	–	0.4	V
Output Impedance	Z_{OH}	V_O = 0.5 V_{DD}; output driving high	–	29	–	Ω
	Z_{OL}	V_O = 0.5 V_{DD}; output driving low	–	27	–	

1. FOUT1CLK (120 MHz) is functional and not loaded.

Table 5. AC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions / Description		Min	Typ	Max	Unit
Rise Time	t_r	V_O = 0.8 V to 2.0 V; C_L = 15 pF	FOUT1CLK	640	680	750	pS
			FOUT2CLK	440	480	600	
Fall Time	t_f	V_O = 2.0 V to 0.8 V; C_L = 15 pF	FOUT1CLK	660	720	800	pS
			FOUT2CLK	460	520	570	
Clock Duty Cycle	t_D	Ratio of pulse width (as measured from rising edge to next falling edge at 2.5 V) to one clock period		45	–	55	%
Frequency Deviation	f_D	Output Frequency = 120 MHz		–	±2.73	–	%
		Output Frequency = 72 MHz / 48 MHz		–	±1.78	–	
Jitter, Long Term	$T_{j\ (LT)}$	On rising edges 500 μS apart at 2.5 V relative to an ideal clock, PLL B inactive (Note 2)		–	45	–	pS
		On rising edges 500 μS apart at 2.5 V relative to an ideal clock, PLL B active (Note 2)		–	165	–	
Jitter, peak to peak	$T_{j\ (\Delta T)}$	From rising edge to next rising edge at 2.5 V, PLL B inactive (Note 2)		–	110	–	pS
		From rising edge to next rising edge at 2.5 V, PLL B active (Note 2)		–	390	–	
Clock Stabilization Time	t_{STB}	Output active from power up, RUN Mode via Software Power Down		–	125	–	μS

2. C_L = 15 pF, F_{xin} = 14.31818 MHz.

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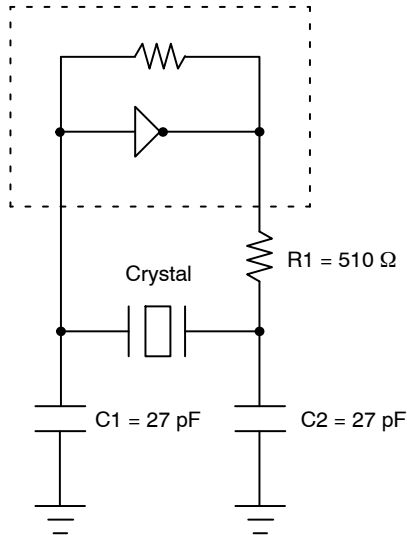**Figure 2. Typical Crystal Oscillator Circuit**

Table 6. TYPICAL CRYSTAL SPECIFICATIONS

Fundamental AT Cut Parallel Resonant Crystal	
Nominal Frequency	14.31818 MHz
Frequency Tolerance	±50 ppm or better at 25°C
Operating temperature range	−20°C to +85°C
Storage Temperature	−40°C to +85°C
Load Capacitance	18 pF
Shunt capacitance	7 pF maximum
ESR	25 Ω

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I2C Serial Interface Information

The information in this section assumes familiarity with I2C programming.

How to Program ASM3P2508A through I2C:

- Master (host) sends a start bit.
- Master (host) sends the write address D4 (H).
- ASM3P2508A device will acknowledge.
- Master (host) sends the beginning byte location (N = 0, 1).
- ASM3P2508A device will acknowledge.
- Master (host) sends a byte count (X = 1, 2).
- ASM3P2508A device will acknowledge.
- Master (host) starts sending byte N through byte (N+X−1).
- ASM3P2508A device will acknowledge each byte one at a time.
- Master (host) sends a Stop bit.

Controller (Host)	ASM3P2508A (slave/receiver)
Start Bit	
Slave Address D4 (H)	
	ACK
Beginning byte location (=N)	
	ACK
Byte count (=X)	
	ACK
Beginning byte (Byte N)	
	ACK
Next Byte (Byte N+1)	
	ACK
_____	
	____
Last Byte (Byte N+X−1)	
	ACK
Stop Bit	

How to Read from ASM3P2508A through I2C:

- Master (host) will send start bit.
- Master (host) sends the write address D4 (H).
- ASM3P2508A device will acknowledge.
- Master (host) sends the beginning byte location (N = 0, 1).
- ASM3P2508A device will acknowledge.
- Master (host) will send a separate start bit.
- Master (host) sends the read address D5 (H).
- ASM3P2508A device will acknowledge.
- ASM3P2508A device will send the byte count (X = 1, 2).
- Master (host) acknowledges.
- ASM3P2508A device sends byte N through byte (N+X−1).
- Master (host) will need to acknowledge each byte.
- Master (host) will send a stop bit.

Controller (Host)	ASM3P2508A (slave/receiver)
Start Bit	
Slave Address D4 (H)	
	ACK
Beginning Byte = N	
	ACK
Repeat start	
Slave address D5 (H)	
	ACK
	Byte Count (= X)
ACK	
	Beginning byte N
ACK	
	Next Byte N+1
ACK	
	____
_____	
	Last Byte (Byte N+X−1)
Not Acknowledge	
Stop Bit	

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An example of a Byte Write via I2C to partially 'power down' the device:

ASM3P2508A can be partially 'powered down' using bit 1 of Byte 0. The organization of the register bits for Byte '0' is given with default values below:

Bit							
7	6	5	4	3	2	1	0
Resv	Resv	Resv	Resv	Resv	Resv	PLL2 Enable	PLL1 Enable
0	1	0	1	0	1	1	1

The function of partial power down of the device is of interest to us – that is bit 1 of Byte 0. In the default mode this bit is logic '1'. As such, the Byte 0 default value is 57 (H). To put ASM3P2508A in 'power down' mode, the bit 1 of Byte 0 is to be changed to logic '0'. Hence writing a 55 (H) via I2C into Byte 0 would put the device in partial 'power down' mode where the PLL block generating 72 MHz / 48 MHz would be powered down while I2C block, crystal oscillator, and the PLL block generating 120 MHz would still be active. The organization of the register bits is as below:

Bit							
7	6	5	4	3	2	1	0
Resv	Resv	Resv	Resv	Resv	Resv	PLL2 Enable	PLL1 Enable
0	1	0	1	0	1	0	1

	Byte 0	Byte 1	FOUT1CLK (MHz)	FOUT2CLK (MHz)
Power up default	6F (H)	3F (H)	120	72
48_MHz Mode	6F (H)	BF (H)	120	48
Power down PLL with 72 MHz	6D (H)	3F (H)	120	–
Power down PLL with 48 MHz	6D (H)	BF (H)	120	–

Figure Showing a Complete Data Transfer:
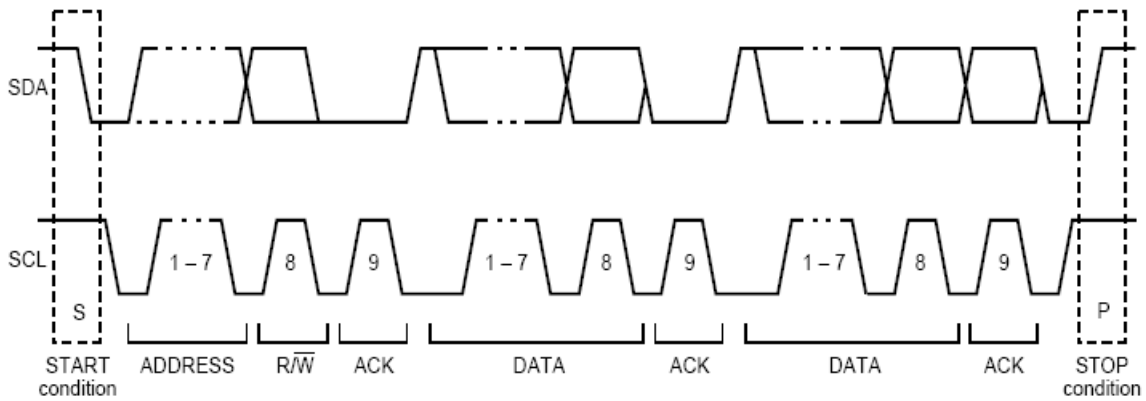
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PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD−01
ISSUE O

PIN # 1
IDENTIFICATION
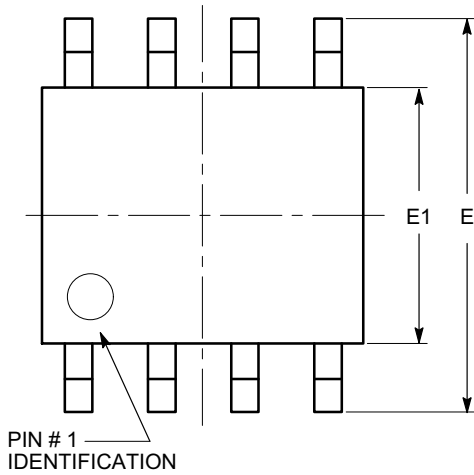
TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0°		8°
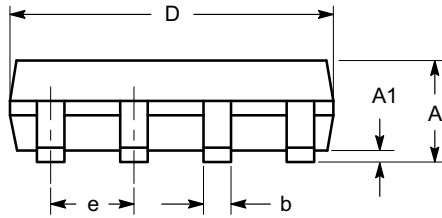
SIDE VIEW
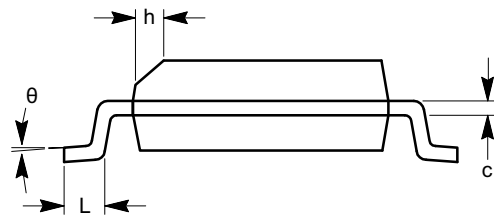
END VIEW

Notes:

(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

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Table 7. ORDERING INFORMATION

Part Number	Marking	Package Type	Temperature
ASM3P2508AG–08ST	3P2508AG	8–PIN SOIC, TUBE, Green	Commercial
ASM3P2508AG–08SR	3P2508AG	8–PIN SOIC, TAPE AND REEL, Green	Commercial
ASM3I2508AG–08ST	3I2508AG	8–PIN SOIC, TUBE, Green	Industrial
ASM3I2508AG–08SR	3I2508AG	8–PIN SOIC, TAPE AND REEL, Green	Industrial
ASM3P2508AF–08ST	3P2508AF	8–PIN SOIC, TUBE, Pb Free	Commercial
ASM3P2508AF–08SR	3P2508AF	8–PIN SOIC, TAPE AND REEL, Pb Free	Commercial
ASM3I2508AF–08ST	3I2508AF	8–PIN SOIC, TUBE, Pb Free	Industrial
ASM3I2508AF–08SR	3I2508AF	8–PIN SOIC, TAPE AND REEL, Pb Free	Industrial

ASM3P2508A/D