Panasonic

AN8920K

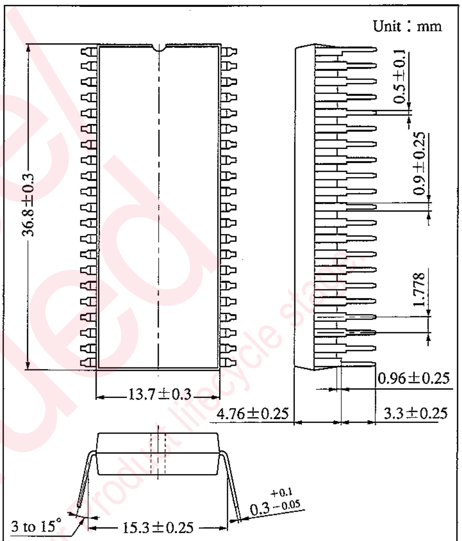
QPSK/QPR Demodulator IC

■ Overview

The AN8920K is a QPSK/QPR demodulator IC. It demodulates 44MHz QPR- or QPSK-modulated signals into digital signals.

■ Features

- Built-in clock detector for QPR demodulation
- 44MHz amplifier built-in
- AGC level detection built-in
- TTL-level output

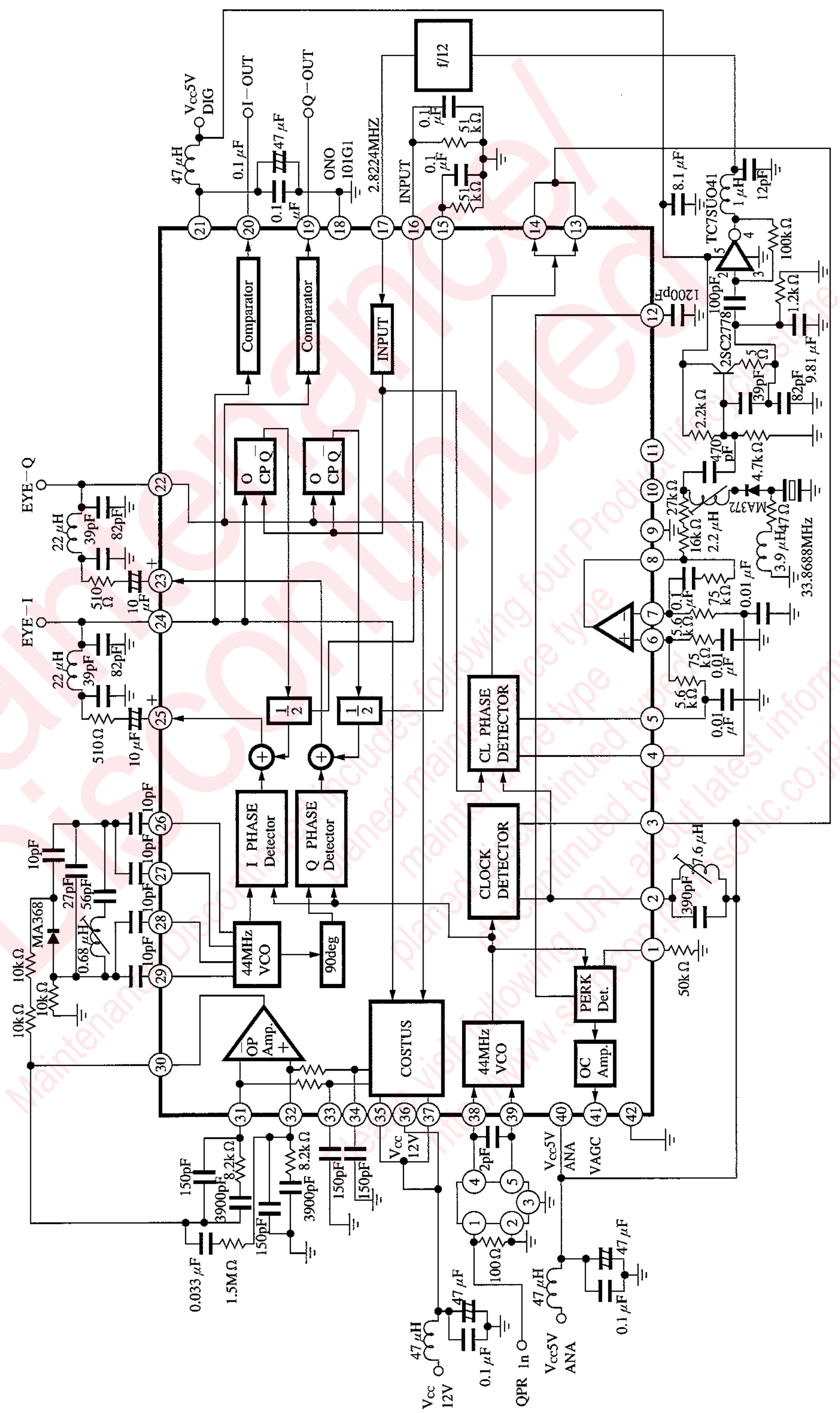


42-Pin SDIP Package (SDIP042-P-0600A)

■ Pin Descriptions

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	AGC level adj.	12	AGC peak detection	23	Eye pattern output Q	34	Costus output +
2	Clock extraction	13	2.8 MHz phase detection output −	24	Eye pattern input I	35	Costus adj. −
3	Clock extraction bias	14	2.8 MHz phase detection output +	25	Eye pattern output I	36	Analog V_{CC} (12V)
4	Clock PLL phase detection 1	15	1/2 shift adj. Q	26	VCO output −	37	Costus adj. +
5	Clock PLL phase detection 2	16	1/2 shift adj. I	27	VCO input −	38	QPR (QPSK) input+
6	OPAMP1 input +	17	Clock input	28	VCO input +	39	QPR (QPSK) input−
7	OPAMP1 input −	18	Digital GND	29	VCO output +	40	Analog V_{CC} (5V)
8	OPAMP1 output	19	Q−OUT	30	OPAMP2 output	41	AGC output
9	GND	20	I−OUT	31	OPAMP2 input −	42	Analog GND
10	NC	21	Digital V_{CC} (5V)	32	OPAMP2 input +		
11	NC	22	Eye pattern input Q	33	Costus output −		

■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC} (12V)	13.2	V
Supply current	V_{CC} (5V)	5.5	V
Power dissipation	P_D	1000	mW
Operating ambient temperature Note1)	T_{opr}	−20 to +75	℃
Storage temperature Note1)	T_{stg}	−55 to +150	℃

Note 1) Ta=25℃ except operating ambient temperature and storage temperature.

■ Recommended Operating Range (Ta=25℃)

Parameter	Symbol	Range
Operating supply voltage range	V_{CC} (12V)	10.8V to 12.6V
	V_{CC} (5V)	4.5V to 5.25V

■ Electrical Characteristics (Ta=25±2℃)

Parameter	Symbol	Condition	min	typ	max	Unit
Offset voltage (costus loop)	V_{32-31}	Pin㉒, ㉔=GND Voltage difference between Pin㉛ to ㉜	−100	0	100	mV
Costus loop gain Q	G_CQ	Gain between Pin㉒ and Pin㉜, when I_{22} is varied from −50 μA to +50 μA	1.5	3	4.5	dB
Costus loop gain I	G_CI	Gain between Pin㉔ and Pin㉛, when I_{22} is varied from −50 μA to +50 μA	1.5	3	4.5	dB
Comparator output level (HIGH)	V_H	DC voltage in HIGH output I_{22}, I_{24}=+50 μA	3.0	3.5	4.0	V
Comparator output level (LOW)	V_L	DC voltage in LOW output I_{22}, I_{24}=−50 μA	0.0	0.4	0.8	V
AGC HIGH level	V_{AH}	Pin㊶ voltage in HIGH output	8.0	8.5	9.0	V
AGC LOW level	V_{AL}	Pin㊶ voltage in LOW output	0	0.1	0.3	V
Input circuit HIGH level	V_{iH}	Pin⑰ voltage to become $V_{4-42} > V_{5-42}$	3.2	—	5.3	V
Input circuit LOW level	V_{iL}	Pin⑰ voltage to become $V_{4-42} < V_{5-42}$	0	—	1.8	V
I_{tot} (5V)	I_{tot}−5V	Pin㉑, ㊵ total current	—	34	43	mA
I_{tot} (12V)	I_{tot}−12V	Pin㊱ current	—	6.5	10	mA
QPR capture range	f_{QCR}	Adjust Pin㉖ output frequency at 44MHz ± 200kHz with VT	—	—	200	kHz
VCO (44MHz) variable width 1	ΔF1	Frequency difference between V_{OSC}= 11V and 6V	200	300	400	kHz
VCO (44MHz) variable width 2	ΔF2	Frequency difference between V_{OSC}= 1V and 6V	−500	−370	−240	kHz
Eye pattern output level	Veye	Voltage level at Pin㉒	210	250	345	mVrms
AGC ON level	V_{AGC}	Input voltage (QPRin) to become Pin㊶ < 4.0V	85	120	170	mV_{P-P}
Clock detection PLL capture range	ΔCc	Center f=2.8224 MHz	−34	—	21	ppm
90°-shift phase-difference	θ 90	Not modulated input fin=44.1MHz, Vin=110mV_{P-P} Phase difference between Pin⑲, ⑳ f_O=100kHz	(87)	(90)	(93)	deg

Unless otherwise specified : V_{CC}(5V)=5V, V_{CC}(12V)=12V
Input signal : QPR (44.0MHz), Input level : Vi=110mV_{P-P} (QPR in Termination)
When V_{OSC}=6.0V (S1 : ON), adjust the output frequency of Pin㉖ at 44MHz by the external supply VT.

Note) The characteristics value in parentheses is not a guaranteed value, but reference one on design.
V_{CC}(5V)=5V, V_{CC}(12V)=12V

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