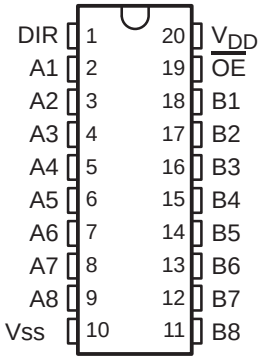
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- **Wide Operating Voltage Range of 2 V to 6 V**
- **High-Current 3-State Outputs Drive Bus Lines Directly or Up To 15 LSTTL Loads**
- **Low Power Consumption, 80-μA Max I_{CC}**
- **Typical t_{pd} = 12 ns**
- **±6-mA Output Drive at 5 V**
- **Low Input Current of 1 μA Max**

N, NS, PACKAGE
(TOP VIEW)



description/ordering information

These octal bus transceivers are designed for asynchronous bi-direction communication between data buses. The control-function implementation minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

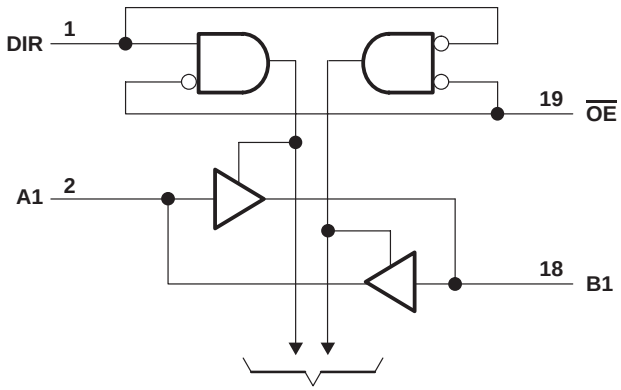
ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube of 20	WS74HC245N	WS74HC245N
	SOP – NS	Reel of 2000	WS74HC245NSR	HC245

FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic diagram (positive logic)



To Seven Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, VDD . . . . . –0.5 V to 7 V
Input clamp current, I_{IK} (V_I < 0 or V_I > VDD) (see Note 1) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) (see Note 1) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{DD}) . . . . . ±35 mA
Continuous current through V_{DD} or Vss . . . . . ±70 mA
Package thermal impedance, θ_{JA} (see Note 2):

N package . . . . . 69°C/W
NS package . . . . . 60°C/W
. . . . . .

Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			WS74HC245			UNIT
			MIN	NOM	MAX	
V_{DD}	Supply voltage		2	5	6	V
V_{IH}	High-level input voltage	V_{DD} = 2 V	1.5			V
		V_{DD} = 4.5 V	3.15			
		V_{DD} = 6 V	4.2			
V_{IL}	Low-level input voltage	V_{DD} = 2 V			0.5	V
		V_{DD} = 4.5 V			1.35	
		V_{DD} = 6 V			1.8	
V_I	Input voltage		0		V_{DD}	V
V_O	Output voltage		0		V_{DD}	V
$\Delta t/\Delta v$	Input transition rise/fall time	V_{DD} = 2 V			1000	ns
		V_{DD} = 4.5 V			500	
		V_{DD} = 6 V			400	
T_A	Operating free-air temperature		–40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{DD} or Vss to ensure proper device operation.

DC ELECTRICAL CHARACTERISTICS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{DD}	T_A = 25°C			WS74HC245		UNIT
					MIN	TYP	MAX	MIN	MAX	
V_{OH}		V_I = V_{IH} or V_{IL}	I_{OH} = –20 µA	2 V	1.9	1.998		1.9		V
				4.5 V	4.4	4.499		4.4		
				6 V	5.9	5.999		5.9		
			I_{OH} = –6 mA	4.5 V	3.98	4.3		3.84		
			I_{OH} = –7.8 mA	6 V	5.48	5.8		5.34		
V_{OL}		V_I = V_{IH} or V_{IL}	I_{OL} = 20 µA	2 V		0.002	0.1		0.1	V
				4.5 V		0.001	0.1		0.1	
				6 V		0.001	0.1		0.1	
			I_{OL} = 6 mA	4.5 V		0.17	0.26		0.33	
			I_{OL} = 7.8 mA	6 V		0.15	0.26		0.33	
I_I	DIR or $\overline{OE}$	V_I = V_{DD} or 0		6 V			±0.1	±100		nA
I_{OZ}	A or B	V_O = V_{DD} or 0		6 V			±0.01	±0.5		µA
I_{CC}		V_I = V_{DD} or 0,	I_O = 0	6 V			8		80	µA
C_i	DIR or $\overline{OE}$			2 V to 6 V		3	10		10	pF

AC ELECTRICAL CHARACTERISTICS

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{DD}	T_A = 25°C			WS74HC245		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	B or A	2 V		40	105		130	ns
			4.5 V		15	21		26	
			6 V		12	18		22	
t_{en}	$\overline{OE}$	A or B	2 V		125	230		290	ns
			4.5 V		23	46		58	
			6 V		20	39		49	
t_{dis}	$\overline{OE}$	A or B	2 V		74	200		250	ns
			4.5 V		25	40		50	
			6 V		21	34		43	
t_t		A or B	2 V		20	60		75	ns
			4.5 V		8	12		15	
			6 V		6	10		13	

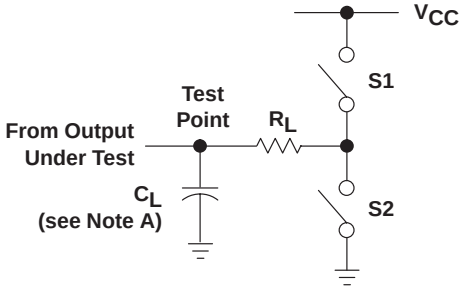
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{DD}	T_A = 25°C			WS74HC245		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	B or A	2 V		54	135		170	ns
			4.5 V		18	27		34	
			6 V		15	23		29	
t_{en}	$\overline{OE}$	A or B	2 V		150	270		335	ns
			4.5 V		31	54		67	
			6 V		25	46		56	
t_t		A or B	2 V		45	210		265	ns
			4.5 V		17	42		53	
			6 V		13	36		45	

operating characteristics, T_A = 25°C

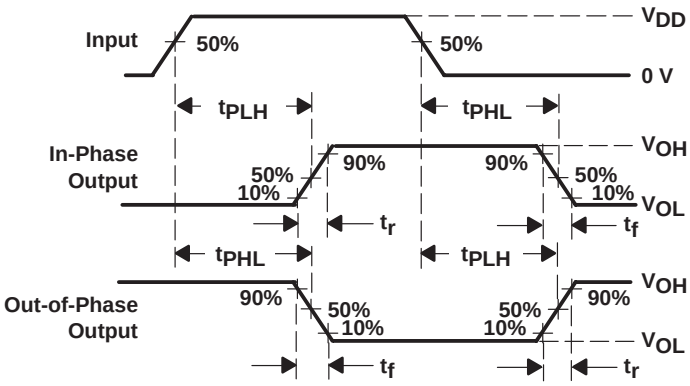
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	No load	40	pF

PARAMETER MEASUREMENT INFORMATION

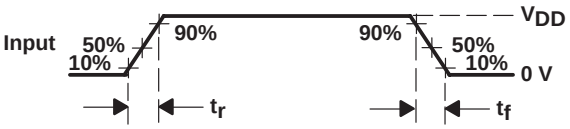


LOAD CIRCUIT

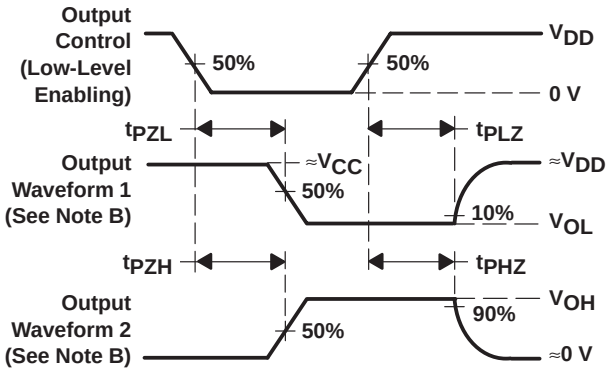
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		––	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

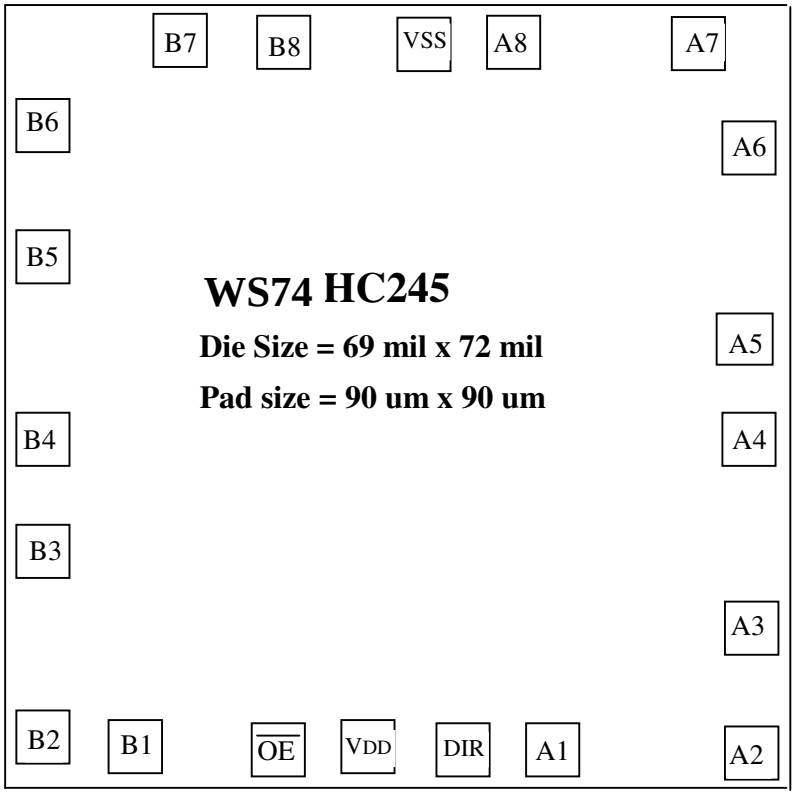
NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

PIN DESCRIPTION

PIN NO.	SYMBOL	
1	DIR	Direction control
2, 3, 4, 5, 6, 7, 8, 9	A1 – A8	Data inputs / Outputs
10	VSS	Ground (0V)
18, 17, 16, 15, 14, 13, 12, 11	$\overline{B1}$ – B8	Data inputs / Outputs
19	$\overline{OE}$	Output enable input (active Low)
20	VDD	Positive power supply

PAD DIAGRAM



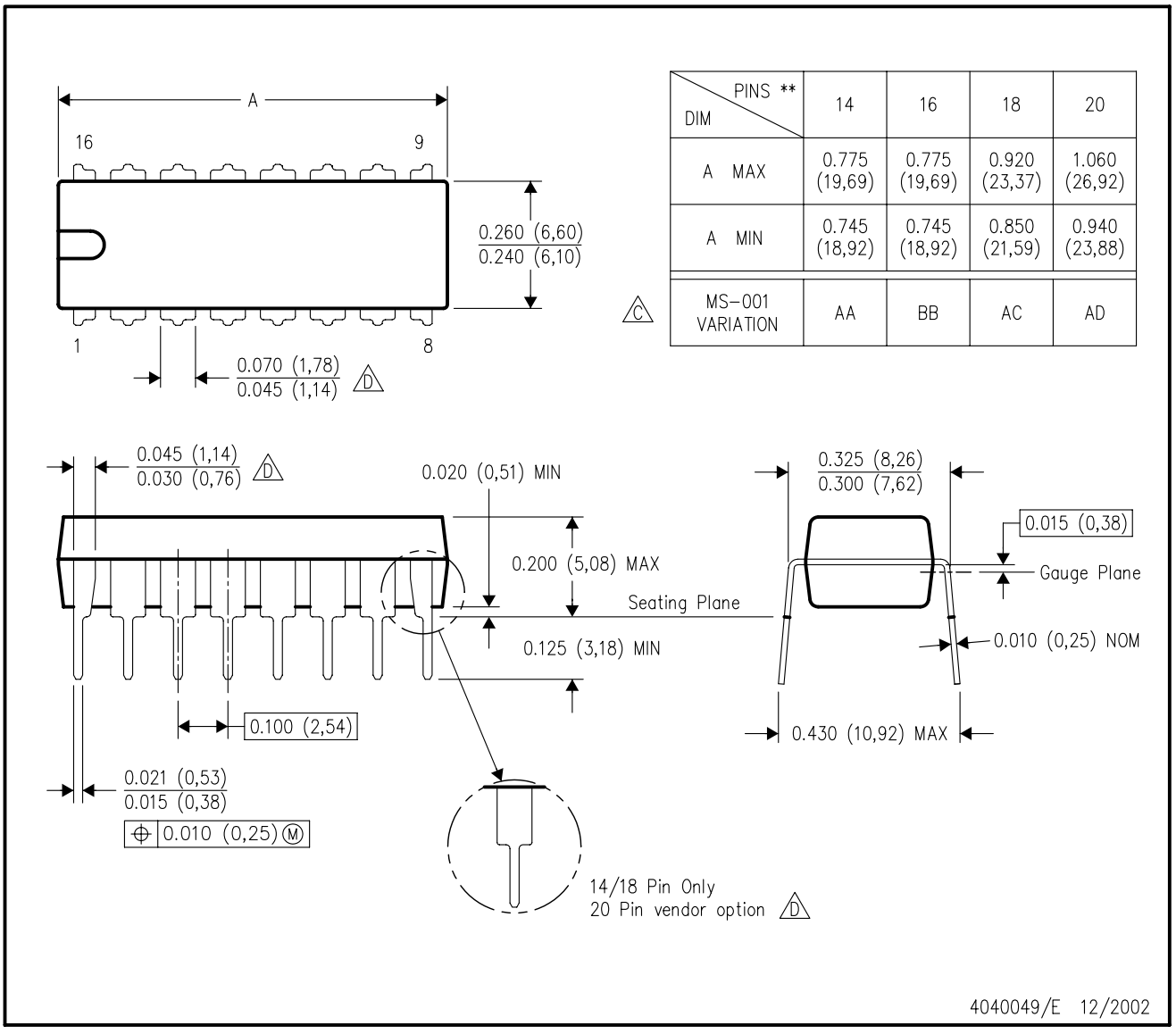
The Coordinate of Low Left Corner for Each Pad

B2 (-741.9, -722.4)	A3 (651.8, -503.2)	B8 (-267.8, 657.6)
$\overline{B1}$ (-558.3, -747.1)	A4 (651.8, -124.2)	B7 (-466.6, 657.6)
$\overline{OE}$ (-288.0, -747.1)	A5 (651.8, 74.6)	B6 (-741.9, 506.6)
VDD(-111.4, -742.5)	A6 (651.8, 454.0)	B5 (-741.9, 236.8)
DIR (85.8, -747.1)	A7 (559.5, 657.6)	B4 (-741.9, -143.4)
A1 (262.6, -747.1)	A8 (179.3, 657.6)	B3 (-741.9, -342.2)
A2 (642.8, -747.1)	VSS (2.7, 658.6)	

N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



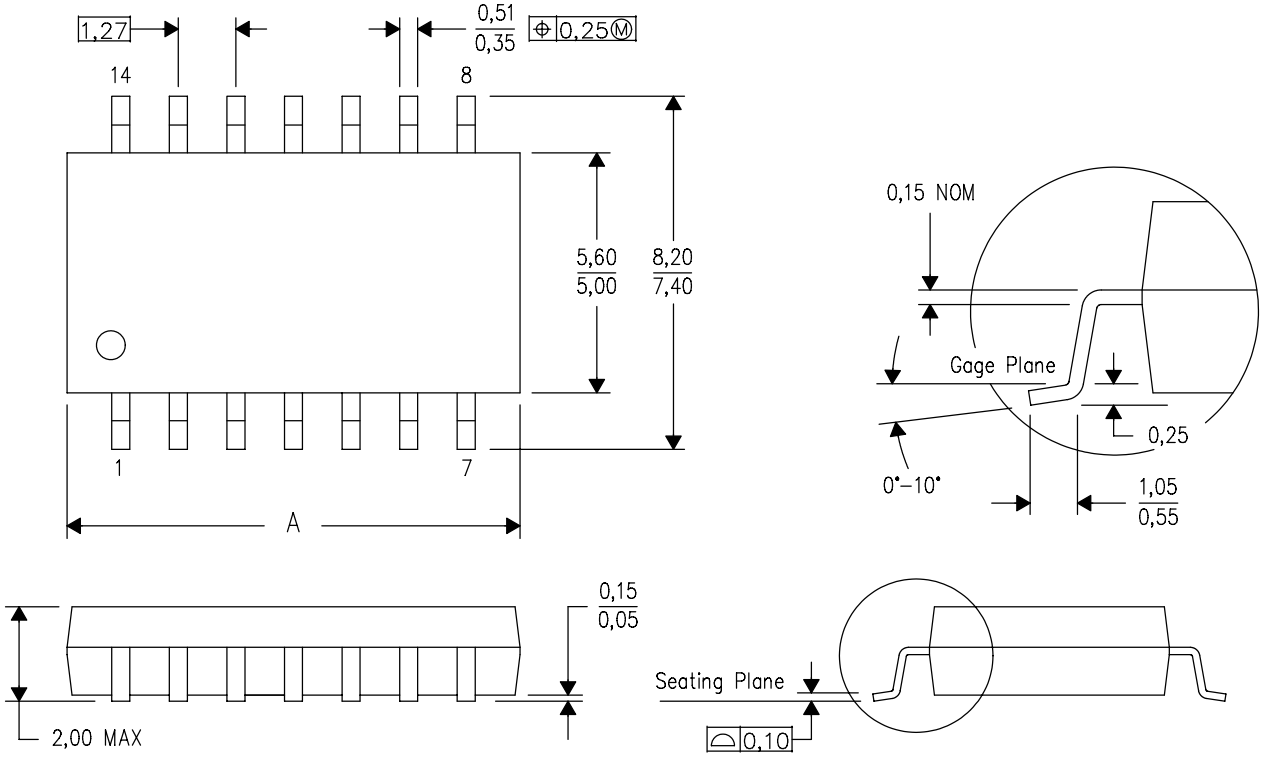
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

3/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.