AN985B
CardBus-to-Ethernet LAN Controller

DATASHEET

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***ADMtek**.com.tw*

GENERAL DESCRIPTIONS

The AN985B is a high performance CARDBUS Fast Ethernet controller with integrated physical layer interface for 10BASE-T and 100BASE-TX application.

The AN985B was designed with advanced 0.25um CMOS technology to provide glueless 32-bit bus master interface for CARDBUS, boot ROM interface, CSMA/CD protocol for Fast Ethernet, as well as the physical media interface for 100BASE-TX of IEEE802.3u and 10BASE-T of IEEE802.3. The auto-negotiation function is also supported for speed and duplex detection.

The AN985B provides both half-duplex and full-duplex operation, as well as support for full-duplex flow control.

It provides long FIFO buffers for transmission and receiving, and early interrupt mechanism to enhance performance.

The AN985B also supports ACPI and CARDBUS compliant power management function and Magic Packet wake-up event.

SYSTEM BLOCK DIAGRAM

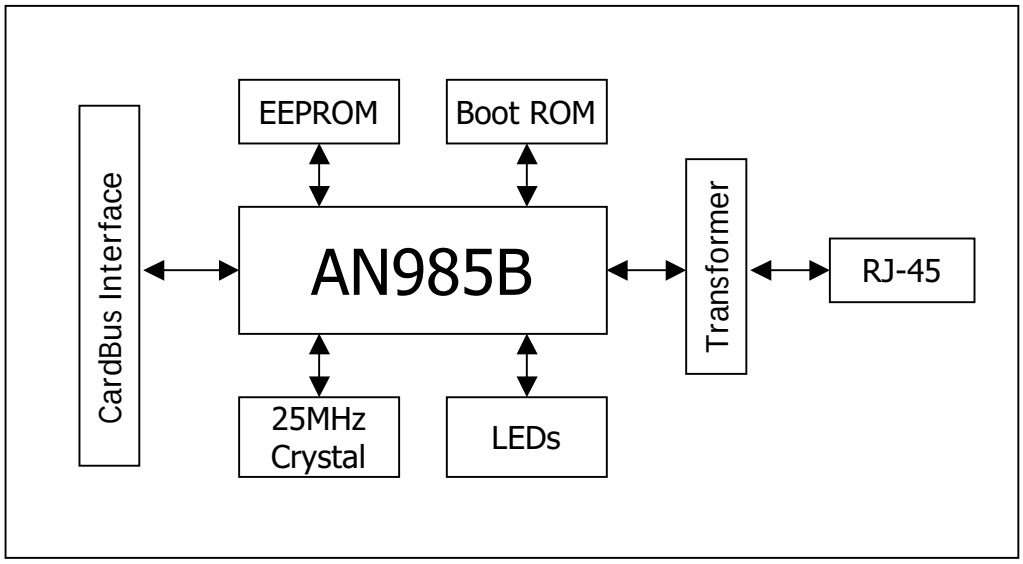


Fig.1 System Diagram of the AN985B

FEATURES

Industry standard

- ⇨ IEEE802.3u 100BASE-TX and IEEE802.3 10BASE-T compliant
- ⇨ Support for IEEE802.3x flow control
- ⇨ IEEE802.3u Auto-Negotiation support for 10BASE-T and 100BASE-TX
- ⇨ CARDBUS interface
- ⇨ ACPI and CARDBUS power management standard compliant
- ⇨ Support PC98 wake on LAN

FIFO

- ⇨ Provides two independent long FIFOs with 2k bytes each for transmission and receiving
- ⇨ Pre-fetch up to two transmit packets to minimize inter frame gap(IFG) to 0.96us
- ⇨ Retransmits collided packet without reload from host memory within 64 bytes.
- ⇨ Automatically retransmits FIFO under-run packet with maximum drain threshold until 3 times retry failure and that will not influence the registers and transmit threshold of next packet

CARDBUS I/F

- ⇨ Provides 32-bit CARDBUS bus master data transfer
- ⇨ Supports CARDBUS clock with frequency from 0Hz to 33MHz
- ⇨ Supports network operation with CARDBUS system clock from 20MHz to 33MHz
- ⇨ Provides performance meter, CARDBUS bus master latency timer, for tuning the threshold to enhance the performance
- ⇨ Provides burst transmit packet interrupt and transmit/receive early interrupt to reduce host CPU utilization

- ⇨ Supports memory-read, memory-read-line, memory-read-multiple, memory-write, memory-write-and-invalidate command while being bus master
- ⇨ Supports big or little endian byte ordering

EEPROM/Boot ROM I/F

- ⇨ Provides write-able Flash ROM and EPROM as boot ROM with size up to 128kB
- ⇨ Provides CARDBUS to access boot ROM by byte, word, or double word
- ⇨ Re-writes Flash boot ROM through I/O port by programming register
- ⇨ Provides serial interface for read/write 93C66 EEPROM
- ⇨ Automatically loads device ID, vendor ID, subsystem ID, subsystem vendor ID, Maximum-Latency , and Minimum-Grand from the 64 byte contents of 93C66 after CARDBUS reset de-asserted in CARDBUS environment.
- ⇨ CIS data is recalled from 93C66 to AN985B PC internal SRAM to speed up CIS access in CARDBUS environment.

MAC/Physical

- ⇨ Integrates the whole Physical layer functions of 100BASE-TX and 10BASE-T
- ⇨ Provides Full -duplex operation on both 100Mbps and 10Mbps modes
- ⇨ Provides Auto-negotiation(NWAY) function of full/half duplex operation for both 10 and 100 Mbps
- ⇨ Provides transmit wave-shaper, receive filters, and adaptive equalizer
- ⇨ Provides MLT-3 transceiver with DC restoration for Base-line wander compensation
- ⇨ Provides MAC and Transceiver(TXCVR) loop-back modes for diagnostic
- ⇨ Builds in Stream Cipher Scrambler/ De-scrambler and 4B/5B encoder/decoder
- ⇨ Supports external transmit transformer with turn ratio 1:1
- ⇨ Supports external receive transformer with turn ratio 1:1

LED Display

- ⇨ (1) 3 LEDs displays scheme provided :
  - ◆ 100Mbps(on) or Speed 10(off)
  - ◆ Link(keeps on when link ok) or Activity(will be blinking with 10Hz when receiving or transmitting but not collision)
  - ◆ FD(keeps on when in Full duplex mode) or Collision(will be blinking with 20Hz when colliding)

  (2) 4 LEDs displayed scheme provided :
  - ◆ 100Mbps and Link (keep on when link and 100Mpbs)
  - ◆ 10Mbps and Link (keep on when link and 10Mpbs)
  - ◆ Activity(will be blinking with 10Hz when receiving or transmitting but not collision)
  - ◆ FD(keeps on when in Full duplex mode) or Collision(will be blinking with 20Hz when colliding)

Miscellaneous

- ⇨ Provides 128-pin QFP package for CARDBUS interface

BLOCK DIAGRAM

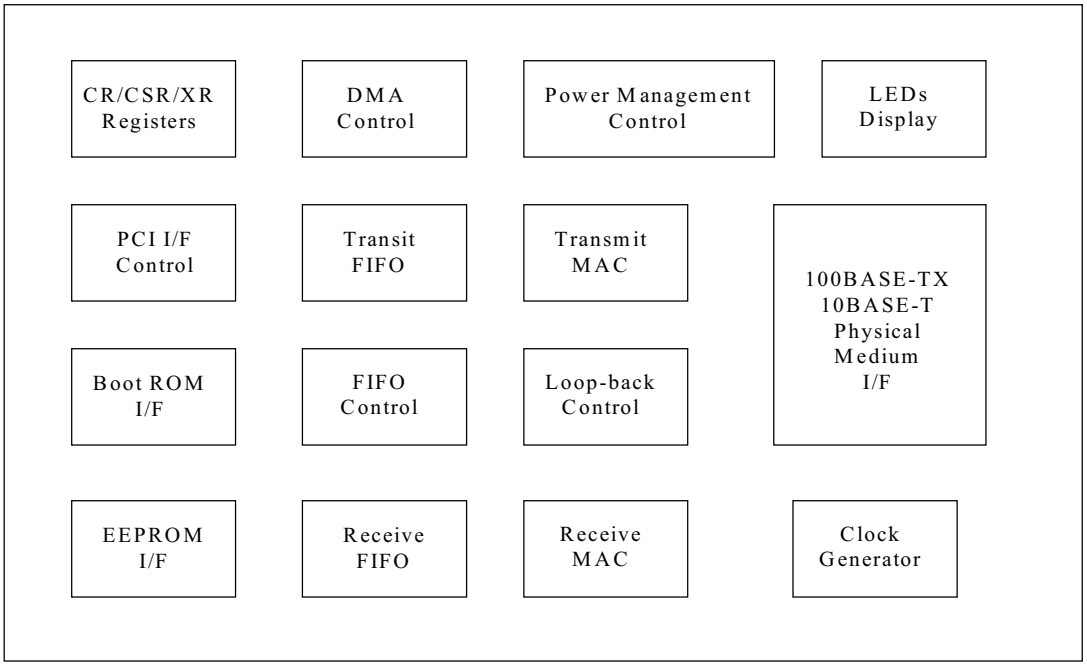
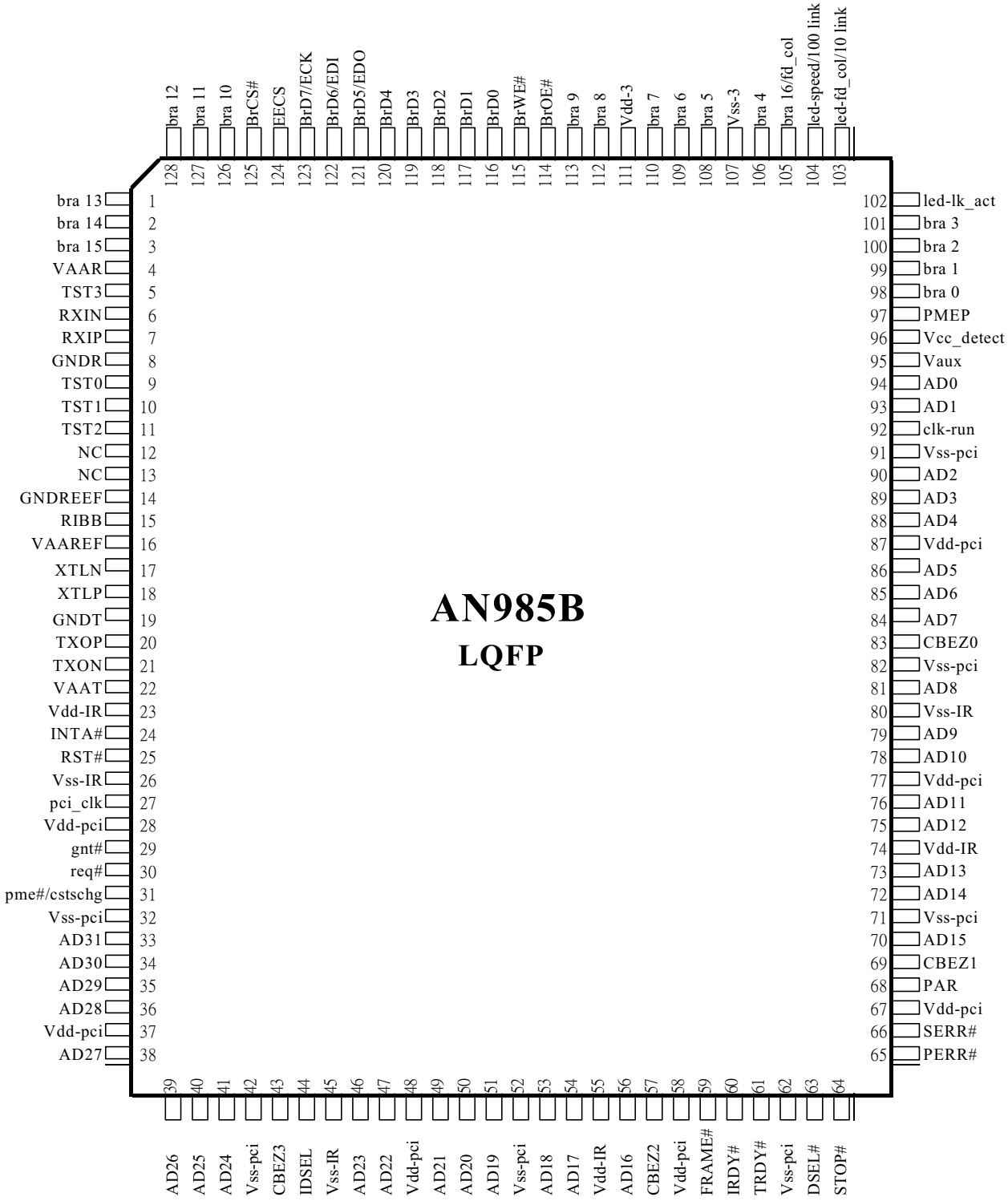


Fig.2 Block Diagram of the AN985B

PIN ASSIGNMENT DIAGRAM



PIN ASSIGNMENT

Pin No.	Name	Type	Description
● **CARDBUS Interface**			
24	INTA#	O/D	CARDBUS interrupt acknowledge. AN985B asserts this signal when one of the
25	RST#	I	CARDBUS signal to initialize the AN985B. The active reset signal should be sustained at least 100μs to guarantee that the AN985B has completed the initializing activity. During the reset period, all the output pins of AN985B will be set to tri-state and all the O/D pins are floated.
27	CLK	I	This CARDBUS clock inputs to AN985B for CARDBUS relative circuits as the synchronized timing base with CARDBUS. The Bus signals are recognized on rising edge of CARDBUS-CLK. In order to let network operating properly, the frequency range of CARDBUS-CLK is limited between 20MHz and 33MHz when network operating.
29	GNT#	I	This signal indicates that the bus request of AN985B have been accepted.
30	REQ#	O	Bus master device want to get bus access right
31	PME# / CSTSCHG	I/O	The Power Management Event signal is an open drain, active low signal for CARDBUS (PME#) When WOL-bit 18 of CSR is set into “1”, means that the AN985B is set into Wake On LAN mode. In this mode, when the AN985B receives a Magic Packet frame from network then the AN985B will active this signal too. In the Wake On LAN mode, when LWS-bit (bit 17) of CSR18 is set into “1” means the LAN-WAKE signal is HP-style signal, otherwise it is IBM-style signal.
33,34 35,36 38,39 40,41 46,47 49,50 51,53 54,56 70,72	AD-31,30 AD-29,28 AD-27,26 AD-25,24 AD-23,22 AD-21,20 AD-19,18 AD-17,16 AD-15,14	I/O	Multiplexed address data pin of CARDBUS Bus

73,75 76,78 79,81 84,85 86,88 89,90 93,94	AD-13,12 AD-11,10 AD-9,8 AD-7, 6 AD-5,4 AD-3,2 AD-1,0		
43 57 69 83	C-BEB3 C-BEB2 C-BEB1 C-BEB0	I/O	Bus command and byte enable
44	IDSEL	I	Initialization Device Select. This signal is asserted when host issues the configuration cycles to the AN985B.
59	FRAME#	I/O	Begin and duration of bus access, driven by master device
60	IRDY#	I/O	Master device is ready to data transaction
61	TRDY#	I/O	Slave device is ready to data transaction
63	DEVSEL#	I/O	Device select, target is driving to indicate the address is decoded
64	STOP#	I/O	Target device request the master device to stop the current transaction
65	PERR#	I/O	Data parity error is detected, driven by the agent receiving data
66	SERR#	O/D	Address parity error
68	PAR	I/O	Parity, even parity (AD[31:0] + C/BE[3:0]), master drives par for address and write data phase, target drives par for read data phase
92	clk-run	I/O O/D	Clock Run for CARDBUS system. In the normal operation situation, Host should assert this signal to indicate AN985B about the normal situation. On the other hand, when Host will deassert this signal when the clock is going down to a nonoperating frequency. When AN985B recognizes the deasserted status of clk-run, then it will assert clk-run to request host to maintain the normal clock operation. When clk-run function is disabled then the AN985B will set clik-run in tri-state.
● **BootROM/EEPROM Interface**			
98~101, 106,108~110, 112,	BrA0 ~16	I/O	ROM data bus Provides up to 128kB EPROM or Flash-ROM application space.

113, 126, 127, 128, 1~3, 105			
116~ 120, 121~ 123,	BrD0~4 BrD5/EDO BrD6/EDI BrD7/ECK	O O/I O/O O/O	BootROM data bus bit (0~7) EDO: Data Output of serial EEPROM, Inputs data to AN985B EDI: Data Input of serial EEPROM, AN985B outputs data to EEPROM ECK: Clock input of serial EEPROM, the AN985B outputs clock signal to EEPROM
124	EECS	O	Chip Select of serial EEPROM
125	BrCS#	O	BootROM Chip Select
114	BrOE#	O	BootROM Read Enable for flash ROM application
115	BrWE#	O	BootROM Write Enable for flash ROM application.
● **Physical Interface**			
18, 17	XTLP, XTLN	I	Crystal inputs. To be connected to a 25MHz crystal.
6,7	RXIN, RXIP	I	The differential receive inputs of 100BASE-TX or 10BASE-T, these pins directly input from Magnetic.
20,21	TXOP, TXON	O	The differential Transmit outputs of 100BASE-TX or 10BASE-T, these pins directly output to Magnetic.
15	RIBB	I	Reference Bias Resistor. To be tied to an external 10.0K (1%) resistor which should be connected to the analog ground at the other end.
9,10,11, 5	TST0, TST1 TST2, TST3	I	Test pin
12,13	NC	O	
● **LED display & Miscellaneous**			
102	Led-Act (Led-lk/act)	O	4Leds mode : LED display for Activity status. This pin will be driven on with 10 Hz blinking frequency when either effective receiving or transmitting is detected. (3Led mode) : link and activity

103	Led-10Lnk (Led-fd/col)	O	4Leds mode : LED display for 10M b/s speed. This pin will be driven on continually when the 10M b/s network operating speed is detected. (3Leds mode) : full duplex / collision
104	Led-100Lnk (Led-speed)	O	4Leds mode : LED display for 100M b/s speed. This pin will be driven on continually when the 100M b/s network operating speed is detected. (3Leds mode) : speed 100(on)/10(off)
105	Led-Fd /Col (bra16)	O	4Leds mode : LED display for Full Duplex or Collision status. This pin will be driven on continually when a full duplex configuration is detected. This pin will be driven on with 20 Hz blinking frequency when a collision status is detected in the half duplex configuration. (3Leds mode) : bra16
95	Vaux	I	When this pin is asserted, it indicates an auxiliary power source is supported ACPI purpose , for detecting the auxiliary power source . This pin should be or-wired connected to 1) 3.3V when 3.3Vaux support , or 2) 5V when 5Vaux support from 3-way switch.
96	Vcc-detect	I	When this pin is asserted, it indicates CARDBUS power source is supported. ACPI purpose , for detecting the main power is remained or not , this pin should be connected to CARDBUS bus power source +5V.
97	PEMP	O	High pulse / low pulse 50ms

- **Digital Power Pins**

26,32,42,45,52,62,71,80,82,91,107,	Vss-pci, Vss-IR, Vss-3
23,28,37,48,55,58,67,74,77,87,111	Vdd-pci Vdd-IR, Vdd-3 Connect to 3.3V

- **Analog Power Pins**

4,16,22	VAAR, VAAREF, VAAT 3.3V
8,14,19	GNDR, GNDREF,GNDT

REGISTERS AND DESCRIPTORS DESCRIPTION

There are three kinds of registers designed for AN985B. They are AN985B configuration registers, CARDBUS control/status registers, and Transceiver control/status registers.

The AN985B configuration registers are used to initialize and configure the AN985B for identifying and querying the AN985B.

The CARDBUS control/status registers are used to communicate between host and AN985B. Host can initialize, control, and read the status of the AN985B through the mapped I/O or memory address space.

Regarding the registers of transceiver portion of AN985B, there are 11 registers with 16bits supported for AN985B. It includes 7 basic registers which are defined according to the clause 22 “Reconciliation Sub-layer and Media Independent Interface” and clause 28 “Physical Layer link signaling for 10 Mb/s and 100 Mb/s Auto-Negotiation on twisted pair” of IEEE802.3u standard. Besides, there are 4 special registers for advance chip controlling and status reading.

The AN985B also provides receive and transmit descriptors for packet buffering and management. These descriptors are described in the following section

AN985B CONFIGURATION REGISTERS

With the configuration registers software driver can initialize and configure AN985B. All of the contents of configuration registers are set to default value when there is any hardware reset occurs. On the other hand, there is no effect to their value when the software reset occurs. To access these configuration registers AN985B provides byte, word, and double word data access length.

AN985B CONFIGURATION REGISTERS LIST

Offset	Index	Name	Descriptions
00h	CR0	LID	Loaded device ID and vendor ID
04h	CR1	CSC	Configuration Status and Command
08h	CR2	CC	Class Code and revision number
0ch	CR3	LT	Latency Timer
10h	CR4	IOBA	IO Base Address
14h	CR5	MBA	Memory Base Address
28h	CR10	CIS	Card Information Structure(for Card bus)
2ch	CR11	SID	Subsystem ID and vendor ID
30h	CR12	BRBA	Boot ROM Base Address (ROM size = 256KB)
34h	CR13	CP	Capability Pointer
3ch	CR15	CINT	Configuration Interrupt
40h	CR16	DS	driver space for special purpose
80h	CR32	SIG	Signature of AN985B
c0h	CR48	PMR0	Power Management Register 0
c4h	CR49	PMR1	Power Management Register 1

■ AN985B CONFIGURATION REGISTERS TABLE

offset	b31 ---------- b16		b15 ---------- b0		
00h	Device ID*		Vendor ID*		
04h	Status		Command		
08h	Base Class Code	Subclass	------	Revision #	Step #
0ch	------	------	Latency timer	cache line size	
10h	Base I/O address				
14h	Base memory address				
18h~ 24h	Reserved				
28h	**ROM-im***	**Address space offset***		**Add-indi***	
2ch	Subsystem ID*		Subsystem vendor ID*		
30h	**Boot ROM base address**				
34h	Reserved			Cap_Ptr	
38h	Reserved				
3ch	Max_Lat*	Min_Gnt*	Interrupt pin	Interrupt line	
40h	Reserved		**Driver Space**	Reserved	
80h	**Signature of AN985B**				
c0h	**PMC**		**Next_Item_Ptr**	**Cap_ID**	
c4h	Reserved		**PMCSR**		

Note: * : automatically recalled from EEPROM when CARDBUS reset is deserted
CIS(28h) is a read-only register
DS(40h), bit15-8, is read/write able register
SIG(80h) is hard wired register, read only.

■ AN985B CONFIGURATION REGISTERS DESCRIPTIONS

CR0(offset = 00h), LID - Loaded Identification number of Device and Vendor

Bit #	Name	Descriptions	Default Val	RW Type
31~16	LDID	Loaded Device ID, the device ID number loaded from serial EEPROM.	From EEPROM	R/O
15~0	LVID	Loaded Vendor ID, the vendor ID number loaded from serial EEPROM.	From EEPROM	R/O

From EEPROM: Loaded from EEPROM

CR1(offset = 04h), CSC - Configuration command and status

Bit #	Name	Descriptions	Default Val	RW Type
31	SPE	Status of Parity Error. 1: means that AN985B detected a parity error. This bit will be set in this condition, even if the parity error response(bit 6 of CR1) is disabled.	0	R/W
30	SES	Status of System Error. 1: means that AN985B asserted the system error pin.	0	R/W
29	SMA	Status of Master Abort. 1: means that AN985B received a master abort and terminated a master transaction.	0	R/W
28	STA	Status of Target Abort. 1: means that AN985B received a target abort and terminated a master transaction.	0	R/W
27	---	reserved.		
26, 25	SDST	Status of Device Select Timing. The timing of the assertion of device select. 01: means a medium assertion of DEVSEL#	01	R/O
24	SDPR	Status of Data Parity Report. 1: when three conditions are met: a. AN985B asserted parity error - PERR# or it detected parity error asserted by other device. b. AN985B is operating as a bus master. c. AN985B's parity error response bit(bit 6 of CR1) is enabled.	0	R/W
23	SFBB	Status of Fast Back-to-Back Always 1, since AN985B has the ability to accept fast back to back transactions.	1	R/O
22~21	---	reserved.		
20	NC	New Capabilities. This bit indicates that whether the AN985B provides a list of extended capabilities, such as	Same as bit 19 of	RO

		CARDBUS power management. 1: the AN985B provides the CARDBUS management function 0: the AN985B doesn't provides New Capabilities.	CSR18	
19~ 9	---	reserved.		
8	CSE	Command of System Error Response 1: enable system error response. AN985B will assert SERR# When it find a parity error on the address phase.	0	R/W
7	---	reserved.		
6	CPE	Command of Parity Error Response 0: disable parity error response. AN985B will ignore any detected parity error and keep on its operating. Default value is 0. 1: enable parity error response. AN985B will assert system error(bit 13 of CSR5) when a parity error is detected.	0	R/W
5~ 3	---	reserved.		
2	CMO	Command of Master Operation Ability 0: disable the bus master ability. 1: enable the CARDBUS bus master ability. Default value is 1 for normal operation.	0	R/W
1	CMSA	Command of Memory Space Access 0: disable the memory space access ability. 1: enable the memory space access ability.	0	R/W
0	CIOSA	Command of I/O Space Access 0: enable the I/O space access ability. 1: disable the I/O space access ability.	0	R/W

R/W: Read and Write able. RO: Read able only.

CR2(offset = 08h), CC - Class Code and Revision Number

Bit #	Name	Descriptions	Default Val	R/W Type
31~24	BCC	Base Class Code. It means AN985B is network controller.	02h	RO
23~16	SC	Subclass Code. It means AN985B is a Fast Ethernet Controller.	00h	RO
15~ 8	---	reserved.		
7 ~ 4	RN	Revision Number, identifies the revision number of	TBD	RO

		AN985B.		
3 ~ 0	SN	Step Number, identifies the AN985B steps within the current revision.	TBD	RO

RO: Read Only. TBD: ???????

CR3(offset = 0ch), LT - Latency Timer

Bit #	Name	Descriptions	Default Val	RW Type
31~16	---	reserved.		
15~ 8	LT	Latency Timer. This value specifies the latency timer of the AN985B in units of CARDBUS bus clock. Once the AN985B asserts FRAME#, the latency timer starts to count. If the latency timer expires and the AN985B still asserted FRAME#, then the AN985B will terminate the data transaction as soon as its GNT# is removed.	0	R/W
7 ~ 0	CLS	Cache Line Size. This value specifies the system cache line size in units of 32-bit double words(DW). The AN985B supports 8, 16, and 32 DW of cache line size. This value is used by the AN985B driver to program the cache alignment bits(bit 14 and 15 of CSR0). The cache alignment bits are used for cache oriented CARDBUS commands, say memory-read-line, memory-read-multiple, and memory-write-and-invalidate.	0	R/W

CR4(offset = 10h), IOBA - I/O Base Address

Bit #	Name	Descriptions	Default Val	RW Type
31~ 8	IOBA	I/O Base Address. This value indicate the base address of CARDBUS control and status register(CSR0~28)	0	R/W
7 ~ 1	---	reserved.		
0	IOSI	I/O Space Indicator. 1: means that the configuration registers map into the I/O space.	1	RO

CR5(offset = 14h), MBA - Memory Base Address

Bit #	Name	Descriptions	Default Val	RW Type
31~ 10	MBA	Memory Base Address. This value indicate the base address of CARDBUS control and status register(CSR0~28)	0	R/W
9 ~ 1	---	reserved.		
0	IOSI	Memory Space Indicator. 1: means that the configuration registers map into the I/O space.	0	RO

CR10(offset = 28h), CIS - Card Information Structure. This register is used to point one of the possible address spaces where the CIS begins. This register is designed for CARDBUS environment. It's data is auto-loaded from the serial EEPROM after power on or hardware reset.

Bit #	Name	Descriptions	Default Val	RW Type
31~28	RI	ROM Image. This ROM image value is applied when the CIS is stored in a boot ROM. This value is loaded from serial EEPROM.	From EEPROM	RO
27~ 3	ASO	Address Space Offset. This value indicate the offset within the address space. The address space is specified by address space indicator(bit 2~0 of CR10).	From EEPROM	RO
2 ~ 0	ASI	Address Space Indicator. This value indicates the location where the CIS address space begins. 7: means that the CIS begins in the boot ROM space. Other than 7: makes all the bits of CIS reset to 0.	From EEPROM	RO

CR11(offset = 2ch), SID - Subsystem ID.

Bit #	Name	Descriptions	Default Val	RW Type
31~16	SID	Subsystem ID. This value is loaded from EEPROM after power on or hardware reset.	From EEPROM	RO
15~ 0	SVID	Subsystem Vendor ID. This value is loaded from EEPROM after power on or hardware reset.	From EEPROM	RO

CR12(offset = 30h), BRBA - Boot ROM Base Address. This register should be initialized before accessing the boot ROM space. (write 32'hffffffff return 32'h fffe0001)

Bit #	Name	Descriptions	Default Val	RW Type
31~17	BRBA	Boot ROM Base Address. This value indicates the address mapping of boot ROM field. Besides, it also defines the boot ROM size. The value of bit 17~10 is set to 0 for AN985B supports up to 128kB of boot ROM.	X: b31~18 0: b17~10	R/W
16 ~ 1	---	reserved	0	
0	BRE	Boot ROM Enable. The AN985B really enables its boot ROM access only if both the memory space access bit(bit 1 of CR1) and this bit are set to 1. 1: enable Boot ROM. (Combines with bit 1 of CR1)	0	R/W

CR13(offset = 34h), CP - Capabilities Pointer.

Bit #	Name	Descriptions	Default Val	RW Type
31~8	---	reserved		
7~0	CP	Capabilities Pointer.	C0h	RO

CR15(offset = 3ch), CI - Configuration Interrupt

Bit #	Name	Descriptions	Default Val	RW Type
31~24	ML	Max_Lat register This value indicates “how often” the AN985B needs to access to the CARDBUS bus in the units of 250ns. This value is loaded from serial EEPROM after power on or hardware reset.	From EEPROM	RO
23~16	MG	Min_Gnt register This value indicates how long the AN985B needs to retain the CARDBUS bus ownership whenever it initiate a transaction, in the units of 250ns. This value is loaded from serial EEPROM after power on or hardware reset.	From EEPROM	RO
15~ 8	IP	Interrupt Pin. This value indicates which of the four interrupt request pins that AN985B is connected. Always 01h: means the AN985B connects to INTA#	01h	RO
7 ~ 0	IL	Interrupt Line. This value indicates which of the system interrupt request lines the INTA# of AN985B is routed to. The BIOS will fill this field when it initializes and configures the system. The AN985B driver can use this value to determine priority and vector information.	X	R/W

CR16(offset = 40h), DS - Driver Space for special purpose.

Bit #	Name	Descriptions	Default Val	RW Type
31~16	---	reserved		
15~8	DS	Driver Space for special purpose. Since this area won’t be cleared in the software reset. The AN985B driver can use this R/W area for special purpose.	X	R/W
7 ~ 0	---	Reserved		

CR32(offset = 80h), SIG - Signature of AN985B

Bit #	Name	Descriptions	Default Val	RW Type
31~16	DID	Device ID, the device ID number of AN985B.	0985h	RO
15~0	VID	Vendor ID, the vendor ID number of ADM Technology Corp.	1317h	RO

CR48(offset = c0h), PMR0, Power Management Register0.

Bit #	Name	Descriptions	Default Val	RW Type
31~27	PMES	PME_Support. The AN985B will assert PME#/CSTSCHG signal while in the D0, D1, D2, D3hot power state. The AN985B supports Wake-up from the above four states.	11111b	RO
26	D2S	D2_Support. The AN985B supports D2 Power Management State.	1	RO

25	D1S	D1_Support. The AN985B supports D1 Power Management State.	1	RO
24~22	AUXC	Aux Current. Thest three bits report the maximum 3.3 Vaux current requirements for AN985B. If bit 31 of PMR0 is '1', the default value is 0101b, means AN985B need 100 mA to support remote wake-up in D3cold power state.	010b	RO
21	DSI	The Device Specific Initialization bit indicates whether special initialization of this function is required before the generic class device driver is able to use it. 0: indicates that the function does not require a device specific initialization sequence following transition to the D0 un-initialized state.	0	RO
20	---	Reserved.	0	RO
19	PMEC	PME Clock. When "1" indicates that the AN985B relies on the presence of the CARDBUS clock for PME#/CSTSCHG operation. While "0" indicates the no CARDBUS clock is required for the AN985B to generate PME#/CSTSCHG.	0	RO
18~16	VER	Version. The value of 010b indicates that the AN985B complies with Revision 1.0a of the CARDBUS Power Management Interface Specification.	010b	RO
15~8	NIP	Next Item Pointer. This value is always 0h, indicates that there is no additional items in the Capabilities List.	00h	RO
7~0	CAPID	Capability Identifier. This value is always 01h, indicates the link list item as being CARDBUS Power Management Registers.	01h	RO

CR49(offset = c4h), PMR1, Power Management Register 1.

Bit #	Name	Descriptions	Default Val	RW Type
31~24	---	Reserved		
23~16	DR	Data register , This register is used to report the state dependent data requested by the data_select field . The value of this register is scaled by the value reported by the data_scale filed	0	RO
15	PMES	PME_Status, This bit is set when the AN985B would normally assert the PME#/CSTSCHG signal for wake-up event, this bit is independent of the state of the PME-En bit. Writing a "1" to this bit will clear it and cause the AN985B to stop asserting a PME#/CSTSCHG (if enabled). Writing a "0" has no effect.	0	R/W*
14,13	DSCAL	Data_Scale, indicates the scaling factor to be used when interpreting the value of the Data register.	2'b00	RO
12~9	DSEL	Data_Select, This four bit field is used to select which	4'b0000	R/W

		data is to be reported through the Data register and Data_Scale field.		
8	PME_En	PME_En, "1" enables the AN985B to assert PME#/CSTSCHG. When "0" disables the PME#/CSTSCHG assertion. Magic packet defult enable : Csr18<18> and csr18<19> set → csr13<9> set , then #pme asserts without impact of PME_En	0	R/W
7~2	---	reserved.	000000b	RO
1,0	PWRS	PowerState, This two bit field is used both to determine the current power state of the AN985B and to set the AN985B into a new power state. The definition of this field is given below. 00b - D0 01b - D1 10b - D2 11b - D3hot This field is auto cleared to D0 when power resumed .	00b	R/W

R/W*: Read and Write 1 clear

Ethernet data register :

Data select	Data scale	Value	Data reported
0	2		D0 power consumption
1	2		D1 power consumption
2	2		D2 power consumption
3	2		D3 power consumption
4	2		D0 power dissipated
5	2		D1 power dissipated
6	2		D2 power dissipated
7	2		D3 power dissipated
8	2		Common function power dissipated
9-15	2		Reserved

■ PCI / CARDBUS CONTROL/STATUS REGISTERS

■ PCI / CARDBUS CONTROL/STATUS REGISTERS LIST

offset from base address of CSR	Index	Name	Descriptions
00h	CSR0	PAR	CARDBUS access register
08h	CSR1	TDR	Transmit demand register
10h	CSR2	RDR	Receive demand register
18h	CSR3	RDB	Receive descriptor base address
20h	CSR4	TDB	Transmit descriptor base address
28h	CSR5	SR	Status register
30h	CSR6	NAR	Network access register
38h	CSR7	IER	Interrupt enable register
40h	CSR8	LPC	Lost packet counter
48h	CSR9	SPR	Serial port register
50h	CSR10	---	Reserved
58h	CSR11	TMR	Timer
60h	CSR12	---	Reserved
68h	CSR13	---	Reserved
70h	CSR14	---	Reserved
78h	CSR15	WTMR	Watchdog timer
80h	CSR16	ACSR5	Status register 2
84h	CSR17	ACSR7	Interrupt enable register 2
88h	CSR18	CR	Command register
8ch	CSR19	CARDBUSC	CARDBUS bus performance counter
90h	CSR20	PMCSR	Power Management Command and Status
94h	CSR21	WTDP	Current transmit descriptor point
98h	CSR22	WRDP	Current receive descriptor point
9ch	CSR23	TXBR	Transmit burst counter/time-out register
a0h	CSR24	FROM	Flash(boot) ROM port
a4h	CSR25	PAR0	Physical address register 0
a8h	CSR26	PAR1	Physical address register 1
ach	CSR27	MAR0	Multicast address hash table register 0
b0h	CSR28	MAR1	Multicast address hash table register 1
100h		FER	Function Event Register
104h		FEMR	Function Event Mask Register
108h		FPSR	Function Present State Register
10ch		FFER	Function Force Event Register

■ CONTROL/STATUS REGISTER DESCRIPTION

CSR0(offset = 00h), PAR - CARDBUS Access Register

Bit #	Name	Descriptions	Default Val	RW Type
31~25	---	Reserved		

24	MWIE	Memory Write and Invalidate Enable. 1: enable AN985B to generate memory write invalidate command. AN985B will generate this command while writing full cache lines. 0: disable AN985B to generate memory write invalidate command and use memory write commands instead.	0	R/W*
23	MRLE	Memory Read Line Enable. 1: enable AN985B to generate memory read line command, while read access instruction reach the cache line boundary. If the read access instruction doesn't reach the cache line boundary then AN985B uses the memory read command instead.	0	R/W*
22	---	Reserved		
21	MRME	Memory Read Multiple Enable. 1: enable AN985B to generate memory read multiple command while reading full cache line. If the memory is not cache aligned, the AN985B uses memory read command instead.	0	R/W*
20~19	---	Reserved		
18,17	TAP	Transmit auto-polling in transmit suspended state, 00: disable auto-polling (default) 01: polling own-bit every 200 us 10: polling own-bit every 800 us 11: polling own-bit every 1600 us	00	R/W*
16	---	Reserved		
15, 14	CAL	Cache alignment, address boundary for data burst, set after reset 00: = PBL 01: min (8 DW , PBL) 10: min (16 DW, PBL) 11: min (32 DW , PBL)	00	R/W*
13 ~ 8	PBL	Programmable Burst Length. This value defines the maximum number of DW to be transferred in one DMA transaction. value: 0 (unlimited), 1, 2, 4, 8, 16(default), 32 DW	010000	R/W*
7	BLE	Big or Little Endian selection. 0: little endian (e.g. INTEL) 1: big endian (only for data buffer)	0	R/W*
6 ~ 2	DSL	Descriptor Skip Length. Defines the gap between two descriptions in the units of DW.	0	R/W*
1	BAR	Bus arbitration 0: receive higher priority 1: transmit higher priority	0	R/W*
0	SWR	Software reset	0	R/W*

		1: reset all internal hardware, except configuration registers. This signal will be cleared by AN985B itself after it completed the reset process.		

R/W* = Before writing the transmit and receive operations should be stopped.

CSR1(offset = 08h), TDR - Transmit demand register

Bit #	Name	Descriptions	Default Val	RW Type
31~ 0	TPDM	Transmit poll demand When written any value in suspended state, trigger read-tx-descriptor process and check the own-bit, if own-bit = 1, then start transmit process	ffffffffh	R/W*

R/W* = Before writing the transmit process should be in the suspended state.

CSR2(offset = 10h), RDR - Receive demand register

Bit #	Name	Descriptions	Default Val	RW Type
31 ~ 0	RPDM	Receive poll demand When written any value in suspended state, trigger the read-rx-descriptor process and check own-bit, if own-bit = 1, then start move data to buffer from FIFO	ffffffffh	R/W*

R/W* = Before writing the receive process should be in the suspended state.

CSR3(offset = 18h), RDB - Receive descriptor base address

Bit #	Name	Descriptions	Default Val	RW Type
31~ 2	SAR	Start address of receive descriptor	xxxxxxx	R/W*
1, 0	RBND	must be 00, DW boundary	00	RO

R/W* = Before writing the receive process should be stopped.

CSR4(offset = 20h), TDB - Transmit descriptor base address

Bit #	Name	Descriptions	Default Val	RW Type
31~ 2	SAT	Start address of transmit descriptor	xxxxxx	R/W*
1, 0	TBND	must be 00, DW boundary	00	RO

R/W* = Before writing the transmit process should be stopped.

CSR5(offset = 28h), SR - Status register

Bit #	Name	Descriptions	Default Val	RW Type
31~ 26	----	reserved		
25~ 23	BET	Bus Error Type. This field is valid only when bit 13 of CSR5(fatal bus error) is set. There is no interrupt generated by this field. 000: parity error, 001: master abort, 010: target abort 011, 1xx: reserved	000	RO
22~ 20	TS	Transmit State. Report the current transmission state only, no interrupt will be generated. 000: stop 001: read descriptor 010: transmitting	000	RO

		011: FIFO fill, read the data from memory and put into FIFO 100: reserved 101: reserved 110: suspended, unavailable transmit descriptor or FIFO overflow 111: write descriptor		
19~17	RS	Receive State. Report current receive state only, no interrupt will be generated. 000: stop 001: read descriptor 010: check this packet and pre-fetch next descriptor 011: wait for receiving data 100: suspended 101: write descriptor 110: flush the current FIFO 111: FIFO drain, move data from receiving FIFO into memory	000	RO
16	NISS	Normal Interrupt Status Summary. It's set if any of below bits of CSR5 asserted.(combines with bit 16 of ACSR5) bit0, transmit completed interrupt bit2, transmit descriptor unavailable bit6, receive descriptor interrupt	0	RO/LH*
15	AISS	Abnormal Interrupt Status Summary. It's set if any of below bits of CSR5 asserted.(combines with bit 15 of ACSR5) bit1, transmit process stopped bit3, transmit jabber timer time-out bit5, transmit under-flow bit7, receive descriptor unavailable bit8, receive processor stopped bit9, receive watchdog time-out bit11, general purpose timer time-out bit13, fatal bus error	0	RO/LH*
14	----	reserved		
13	FBE	Fatal Bus Error. 1: while any of parity error, master abort, or target abort is occurred(see bits 25~23 of CSR5). AN985B will disable all bus access. The way to recover parity error is by setting an software reset.	0	RO/LH*
12	---	reserved		
11	GPTT	General Purpose Timer Time-out, base on CSR11 timer register	0	RO/LH*
10	---	reserved		

9	RWT	Receive Watchdog Time-out, based on CSR15 watchdog timer register	0	RO/LH*
8	RPS	Receive Process Stopped, receive state = stop	0	RO/LH*
7	RDU	Receive Descriptor Unavailable 1: while the next receive descriptor can't be applied by AN985B. The receive process is suspended in this situation. To restart the receive process, the ownership bit of next receive descriptor should be set to AN985B and a receive poll demand command should be issued(or a new recognized frame is received, if the receive poll demand is not issued).	0	RO/LH*
6	RCI	Receive Completed Interrupt 1: while a frame reception is completed.	0	RO/LH*
5	TUF	Transmit Under-Flow 1: while the transmit FIFO had an under-flow condition happened during transmitting. The transmit process will enter the suspended state and report the under-flow errror on bit1 of TDES0.	0	RO/LH*
4	---	Reserved		
3	TJT	Transmit Jabber Time-out 1: while the transmit jabber timer expired. The transmit processor will enter the stop state and the transmit jabber time-out flag of bit 14 of TDES0 will be asserted.	0	RO/LH*
2	TDU	Transmit Descriptor Unavailable 1: while the next transmit descriptor can't be applied by AN985B. The transmission process is suspended in this situation. To restart the transmission process, the ownership bit of next transmit descriptor should be set to AN985B and if the transmit automatic polling is not enabled then a transmit poll demand command should be issued.	0	RO/LH*
1	TPS	Transmit Process Stopped. 1: while transmit state = stop	0	RO/LH*
0	TCI	Transmit Completed Interrupt. 1: means a frame transmission is completed while bit 31 of TDES1 is asserted in the first transmit descriptor of the frame.	0	RO/LH*

LH = High Latching and cleared by writing 1.

CSR6(offset = 30h), NAR - Network access register

Bit #	Name	Descriptions	Default Val	RW Type
31~22	---	Reserved		
21	SF	Store and forward for transmit 0: disable 1: enable, ignore the transmit threshold setting	0	R/W*

20	---	Reserved		
19	SQE	SQE Disable 0: enable SQE function for 10BASE-T operation. The AN985B provides SQE test function for 10BASE-T half duplex operation. 1: disable SQE function.	1	R/W*
18~16	-----	Reserved		
15~14	TR	transmit threshold control 00: 128-byte (100Mbps), 72-byte (10Mbps) 01: 256-byte (100Mbps), 96-byte (10Mbps) 10: 512-byte (100Mbps), 128-byte (10Mbps) 00: 1024-byte (100Mbps), 160-byte (10Mbps)	00	R/W*
13	ST	Stop transmit 0: stop (default) 1: start	0	R/W
12	FC	Force collision mode 0: disable 1: generate collision when transmit (for test in loop-back mode)	0	R/W**
11, 10	OM	Operating Mode 00: normal 01: MAC loop-back 10,11: reserved	00	R/W**
9, 8	---	Reserved		
7	MM	Multicast Mode 1: receive all multicast packets	0	R/W***
6	PR	Promiscuous Mode 1: receive any good packet. 0: receive only the right destination address packets	1	R/W***
5	SBC	Stop Back-off Counter 1: back-off counter stop when carrier is active, and resume when carrier drop. 0: back-off counter is not effected by carrier	0	R/W**
4	---	Reserved		
3	PB	Pass Bad packet 1: receives any packets, if pass address filter, including runt packets, CRC error, truncated packets... For receiving all bad packets, the bit 6 of CSR6 should be set to 1. 0: filters all bad packets	0	R/W***
2	PU	Pass Unicast Mode 1: receive all Unicast packets	0	R/W***
1	SR	Start/Stop Receive	0	R/W

		0: receive processor will enter stop state after the current reception frame completed. This value is effective only when the receive processor is in the running or suspending state. Notice: In "Stop Receive" state, the PAUSE packet and Remote Wake Up packet won't be effected and can be received if the corresponding function is enabled. 1: receive processor will enter running state.		
0	---	Reserved		

W* = only write when the transmit processor stopped.
W = only write when the transmit and receive processor both stopped.**
W* = only write when the receive processor stopped.**

CSR7(offset = 38h), IER - Interrupt Enable Register

Bit #	Name	Descriptions (Refer to CSR5)	Default Val	RW Type
31~17	---	Reserved		
16	NIE	Normal Interrupt Enable 1: enable all the normal interrupt bits(see bit16 of CSR5)	0	R/W
15	AIE	Abnormal Interrupt Enable 1: enable all the abnormal interrupt bits(see bit 15 of CSR5)	0	R/W
14	---	Reserved		
13	FBEIE	Fatal Bus Error Interrupt Enable 1: combine this bit and bit 15 of CSR7 to enable fatal bus error interrupt	0	R/W
12				
11	GPTIE	General Purpose Timer Interrupt Enable 1: combine this bit and bit 15 of CSR7 to enable general purpose timer expired interrupt.	0	R/W
10				
9	RWTIE	Receive Watchdog Time-out Interrupt Enable 1: combine this bit and bit 15 of CSR7 to enable receive watchdog time-out interrupt.	0	R/W
8	RSIE	Receive Stopped Interrupt Enable 1: combine this bit and bit 15 of CSR7 to enable receive stopped interrupt.	0	R/W
7	RUIE	Receive Descriptor Unavailable Interrupt Enable 1: combine this bit and bit 15 of CSR7 to enable receive descriptor unavailable interrupt.	0	R/W
6	RCIE	Receive Completed Interrupt Enable 1: combine this bit and bit 16 of CSR7 to enable receive completed interrupt.	0	R/W
5	TUIE	Transmit Under-flow Interrupt Enable 1: combine this bit and bit 15 of CSR7 to enable	0	R/W

		transmit under-flow interrupt.		
4	---	Reserved		
3	TJTTIE	Transmit Jabber Timer Time-out Interrupt Enable 1: combine this bit and bit 15 of CSR7 to enable transmit jabber timer time-out interrupt.	0	R/W
2	TDUIE	Transmit Descriptor Unavailable Interrupt Enable 1: combine this bit and bit 16 of CSR7 to enable transmit descriptor unavailable interrupt.	0	R/W
1	TPSIE	Transmit Processor Stopped Interrupt Enable 1: combine this bit and bit 15 of CSR7 to enable transmit processor stopped interrupt.	0	R/W
0	TCIE	Transmit Completed Interrupt Enable 1: combine this bit and bit 16 of CSR7 to enable transmit completed interrupt.	0	R/W

CSR8(offset = 40h), LPC - Lost packet counter

Bit #	Name	Descriptions	Default Val	RW Type
31~17	---	Reserved		
16	LPCO	Lost Packet Counter Overflow 1: while lost packet counter overflowed. Cleared after read	0	RO/LH
15~0	LPC	Lost Packet Counter Increment the counter while packet discarded since there was no host receive descriptors available. Cleared after read	0	RO/LH

CSR9(offset = 48h), SPR - Serial port register

Bit #	Name	Descriptions	Default Val	RW Type
31~20	---	Reserved		
19	MDI	MII Management Data Input Specified read data from the external PHY	0	
18	MMC	MII Management Control 0: Write operation to the external PHY 1: Read operation from the external PHY	1	
17	MDO	MII Management Data Output Specified Write Data to the external PHY	0	
16	MDC	MII Management Clock 1: MII Management Clock is a output reference clock to the external PHY	0	
15	---	Reserved		
14	SRC	Serial EEPROM Read Control		
13	SWC	Serial EEPROM Write Control		
12	---	Reserved		
11	SRS	Serial EEPROM Select		
10~4	---	Reserved		

3	SDO	Serial EEPROM data out This bit serially shifts data from the EEPROM to the AN985B.	1	RO
2	SDI	Serial EEPROM data in This bit serially shifts data from the AN985B to the EEPROM.	1	R/W
1	SCLK	Serial EEPROM clock High/Low this bit to provide the clock signal for EEPROM.	1	R/W
0	SCS	Serial EEPROM chip select 1: selects the serial EEPROM chip.	0	R/W

CSR11(offset = 58h), TMR -General-purpose Timer

Bit #	Name	Descriptions	Default Val	RW Type
31~17	---	Reserved		
16	COM	Continuous Operation Mode 1: sets the general-purpose timer in continuous operating mode.	0	R/W
15~0	GTV	General-purpose Timer Value Sets the counter value. This is a count-down counter with the cycle time of 204us.	0	R/W

CSR13(offset = 68h), WCSR –Wake-up Control/Status Register

Bit #	Name	Descriptions	Default Val	RW Type
31	---	Reserved		
30	CRCT	CRC-16 Type 0: Initial contents = 0000h 1: Initial contents = FFFFh	0	R/W
29	WP1E	Wake-up Pattern One Matched Enable.	0	R/W
28	WP2E	Wake-up Pattern Two Matched Enable.	0	R/W
27	WP3E	Wake-up Pattern Three Matched Enable.	0	R/W
26	WP4E	Wake-up Pattern Four Matched Enable.	0	R/W
25	WP5E	Wake-up Pattern Five Matched Enable.	0	R/W
24-18	---	Reserved		
17	LinkOFF	Link Off Detect Enable. The AN985B will set the LSC bit after it has detected that link status is from ON to OFF.	0	R/W
16	LinkON	Link On Detect Enable. The AN985B will set the LSC bit after it has detected that link status is from OFF to	0	R/W

		ON.		
15-11	---	Reserved	00001	
10	WFRE	Wake-up Frame Received Enable. The AN985B will include the “Wake-up Frame Received” event into wake-up events. If this bit is set, AN985B will assert PMES bit of PMR1 after AN985B has received a matched wake-up frame.	0	R/W
9	MPRE	Magic Packet Received Enable. The AN985B will include the “Magic Packet Received” event into wake-up events. If this bit is set, AN985B will assert PMES bit of PMR1 after AN985B has received a Magic packet.	0	R/W
8	LSCE	Link Status Changed Enable. The AN985B will include the “Link Status Changed” event into wake-up events. If this bit is set, AN985B will assert PMES bit of PMR1 after AN985B has detected a link status changed event.	0	R/W
7-3	---	Reserved		
2	WFR	Wake-up Frame Received, 1: Indicates AN985B has received a wake-up frame. It is cleared by write 1 or upon power-up reset. It is not affected by a hardware or software reset.	X	R/W1C*
1	MPR	Magic Packet Received, 1: Indicates AN985B has received a magic packet. It is cleared by write 1 or upon power-up reset. It is not affected by a hardware or software reset.	X	R/W1C*
0	LSC	Link Status Changed, 1: Indicates AN985B has detected a link status change event. It is cleared by write 1 or upon power-up reset. It is not affected by a hardware or software reset.	X	R/W1C*

R/W1C*, Read Only and Write one cleared.

CSR14(offset = 70h), WPDR –Wake-up Pattern Data Register

All six wake-up patterns filtering information are programmed through WPDR register. The filtering information is as follows,

Offset	31 16	15 8	7 0
0000h	Wake-up pattern 1 mask bits 31:0		
0004h	Wake-up pattern 1 mask bits 63:32		
0008h	Wake-up pattern 1 mask bits 95:64		
000ch	Wake-up pattern 1 mask bits 127:96		
0010h	CRC16 of pattern 1	Reserved	Wake-up pattern 1 offset

0014h	Wake-up pattern 2 mask bits 31:0		
0018h	Wake-up pattern 2 mask bits 63:32		
001ch	Wake-up pattern 2 mask bits 95:64		
0020h	Wake-up pattern 2 mask bits 127:96		
0024h	CRC16 of pattern 2	Reserved	Wake-up pattern 2 offset
0028h	Wake-up pattern 3 mask bits 31:0		
002ch	Wake-up pattern 3 mask bits 63:32		
0030h	Wake-up pattern 3 mask bits 95:64		
0034h	Wake-up pattern 3 mask bits 127:96		
0038h	CRC16 of pattern 3	Reserved	Wake-up pattern 3 offset
003ch	Wake-up pattern 4 mask bits 31:0		
0040h	Wake-up pattern 4 mask bits 63:32		
0044h	Wake-up pattern 4 mask bits 95:64		
0048h	Wake-up pattern 4 mask bits 127:96		
004ch	CRC16 of pattern 4	Reserved	Wake-up pattern 4 offset
0050h	Wake-up pattern 5 mask bits 31:0		
0054h	Wake-up pattern 5 mask bits 63:32		
0058h	Wake-up pattern 5 mask bits 95:64		
005ch	Wake-up pattern 5 mask bits 127:96		
0060h	CRC16 of pattern 5	Reserved	Wake-up pattern 5 offset

1. CRC-16 polynomial: Still pending
2. Offset value is from 0-255 (8-bit width).
3. To load the whole wake-up frame filtering information, consecutive 22 long words write operation to CSR14 should be done.

CSR15(offset = 78h), WTMR - Watchdog timer

Bit #	Name	Descriptions	Default Val	RW Type
31	Clock_save	1: clock stuck at 1 when clock save mode enable 0: clock stuck at 0 when clock save mode enable	0	RO/EE 16h[3]
30	CARDBUS_Save	1 : CARDBUS clock save mode enable	0	RO/EE 16h[2]
29	RX_save	1: RXCLK save mode enable	0	RO/EE 16h[1]
28	RX_reve	1: RXCLK reverse mode for HOME PHY mode	0	RO/EE/

	rse			16h[0]
27~6		Reserved		
5	RWR	Receive Watchdog Release, the time of release watchdog timer from last carrier deserted. 0: 24 bit-time 1: 48 bit-time	0	R/W
4	RWD	Receive Watchdog Disable 0: If the receiving packet's length is longer than 2560 bytes, the watchdog timer will be expired. 1: disable the receive watchdog.	0	R/W
3	---	Reserved		
2	JCLK	Jabber clock 0: cut off transmission after 2.6 ms (100Mbps) or 26 ms (10Mbps). 1: cut off transmission after 2560 byte-time.	0	R/W
1	NJ	Non-Jabber 0: if jabber expired, re-enable transmit function after 42 ms (100Mbps) or 420ms (10Mbps) 1: immediately re-enable the transmit function after jabber expired	0	R/W
0	JBD	Jabber disable 1: disable transmit jabber function	0	R/W

CSR16(offset = 80h), ACSR5 - Assistant CSR5(Status register 2)

Bit #	Name	Descriptions	Default Val	RW Type
31	TEIS	Transmit Early Interrupt status Transmit early interrupt status is set to 1 when Transmit early interrupt function is enabled(set bit 31 of CSR17 = 1) and the transmitted packet is moved completed from descriptors to TX-FIFO buffer. This bit is cleared by written with 1.	0	RO/LH*
30	REIS	Receive Early Interrupt Status. Receive early interrupt status is set to 1 when Receive early interrupt function is enabled(set bit 30 of CSR17 = 1) and the received packet is fill up its first receive descriptor. This bit is cleared by written with 1.	0	RO/LH*
29	LCS	Link change status	0	RO/LH*
28	TDIS	Transmit Deferred Interrupt Status.	0	RO/LH*
27	---	Reserved		
26	PFR	PAUSE Frame Received Interrupt Status 1: indicates a PAUSE frame received when the PAUSE function is enabled.	0	RO/LH*
25~17	---	Reserved		
16	ANISS	Added normal interrupt status summary.	0	RO/LH*

		1: any of the added normal interrupt happened.		
15	AAISS	Added Abnormal Interrupt Status Summary. 1: any of added abnormal interrupt happened.	0	RO/LH*
14~0		These bits are the same as the status register of CSR5. You can access those status bits through either CSR5 or CSR16.		RO/LH*

LH* = High Latching and cleared by writing 1.

CSR17(offset = 84h), ACSR7- Assistant CSR7(Interrupt enable register 2)

Bit #	Name	Descriptions	Default Val	RW Type
31	TEIE	Transmit Early Interrupt Enable	0	R/W
30	REIE	Receive Early Interrupt Enable	0	R/W
29	LCIE	Link Change Interrupt enable	0	R/W
28	TDIE	Transmit Deferred Interrupt Enable	0	R/W
27	---	Reserved		
26	PFRIE	PAUSE Frame Received Interrupt Enable	0	R/W
25~17	---	Reserved		
16	ANISE	Added Normal Interrupt Summary Enable. 1: adds the interrupts of bit 30 and 31 of ACSR7 to the normal interrupt summary(bit 16 of CSR5).	0	R/W
15	AAIE	Added Abnormal Interrupt Summary Enable. 1: adds the interrupt of bit 26, 28 and 29 of ACSR7 to the abnormal interrupt summary.	0	R/W
14~0		These bits are the same as the interrupt enable register of CSR7. You can access those interrupt enable bits through either CSR7 or CSR16.		R/W

CSR18(offset = 88h), CR - Command Register, bit31 to bit16 automatically recall from EEPROM

Bit #	Name	Descriptions	Default Val	RW Type
31	D3CS	D3cold support , mapped to CR48<31>	1 from EEPROM	R/W
30-28	AUXCL	Should be 0	000b from EEPROM	R/W
27	pmepsel	1 : negtive pulse ; 0 : positive pulse	0 from eeprom	R/W
26	Pmep_en	0:disable (for old board); 1: enable	0 from eeprom	
25	Pci_pad	1 : apply pci pad in cardbus mode (for twinhead notebook)	0 from	R/W

		0 : apply cardbus pad in cardbus mode no effect in pci mode	eeprom	
24	pmes_sticky	1 : pmez sticky : Vcc_detect has no impact to pmez disasserts 0 : pmez will be disasserted by power up after wakeup event trigger	0 from eeprom	R/W
23	4_3LED	0 : 3_LED scheme 1: 4_LED scheme	0 from EEPROM	R/W
22, 21	RFS	Receive FIFO size control 11: 1K 10: 2K 01,00: reserved	10 from EEPROM	R/W
20	CRD	Clock Run(clk-run pin) disable 1: disables the function of clock run supports to CARDBUS.	0 from EEPROM	R/W
19	PM	Power Management, enables the AN985B whether to activate the Power Management abilities. When this bit is set into “0” the AN985B will set the Cap_Ptr register to zero, indicating no CARDBUS compliant power management capabilities. The value of this bit will be mapped to NC-bit 20 of CR1. In CARDBUS Power Management mode, the Wake-up events include “Wake-up Frame Received”, “Magic Packet Received” and “Link Status Changed” depends on the CSR13 settings	0 from EEPROM	RO
18	APM	APM mode , this bit is effective when PM (csr18[19]) =1	0 from EEPROM	R/W
17	LWS	Should be 0	0 from EEPROM	R/W
16~9	----	reserved		
8	pmepshort	PMEP pulse length select 0:long pulse 50ms 1:short pulse 100us for test purpose	0	R/W
7	D3_APM	D3_cold APM_mode_en PMEZ can be asserted without the impact of PME_EN.	0	R/W
6	RWP	Reset Wake-up Pattern Data Register Pointer 0: Normal 1: Reset	0	R/W
5	PAUSE	PAUSE function control to disable or enable the PAUSE function for flow control. The default value of PAUSE is decided by the result of Auto-Negotiation. Driver can force to enable or disable it after the Auto-Negotiation	0	R/W

		completed. 0: PAUSE function is disabled. 1: PAUSE function is enabled		
4	RTE	Receive Threshold Enable. 1: the receive FIFO threshold is enabled. 0: disable the receive FIFO threshold selection in bit 3~2 of this register, the receive threshold is set to 64-byte.	0	R/W
3~2	DRT	Drain Receive Threshold 00: 32 bytes (8 DW) 01: 64 bytes (16 DW) 10: store-and -forward 11: reserved	01	R/W
1	SINT	Software interrupt.	0	R/W
0	ATUR	1: enable automatically transmit-underrun recovery.	0	R/W

CSR19(offset = 8ch) - CARDBUSC, CARDBUS bus performance counter

Bit #	Name	Descriptions	Default Val	RW Type
31~16	CLKCNT	The number of CARDBUS clock from read request asserted to access completed. This CARDBUS clock number is accumulated all the read command cycles from last CSR19 read to current CSR19 read.	0	RO*
15~8	---	reserved		
7~0	DWCNT	The number of double word accessed by the last bus master. This double word number is accumulated all the bus master data transactions from last CSR19 read to current CSR19 read.	0	RO*

RO* = Read only and cleared by reading.

CSR20(offset = 90h) - PMCSR, Power Management Command and Status.(The same register value mapping to CR49-PMR1.)

Bit #	Name	Descriptions	Default Val	RW Type
31~16	---	reserved		
15	PMES	PME_Status, This bit is set when the AN985B would normally assert the PME# signal for wakeup event, this bit is independent of the state of the PME-En bit. Writing a “1” to this bit will clear it and cause the AN985B to stop asserting a PME#(if enabled). Writing a “0” has no effect. Since the AN985B doesn’t supports PME# from D3cold, this bit is defaulted to “0”.	0	RO
14,13	DSCAL	Data_Scale, indicates the scaling factor to be used when interpreting the value of the Data register. This	00b	RO

		field is required for any function that implements the Data register. Otherwise, it's optional. The AN985B doesn't support Data register and Data_Scale.		
12~9	DSEL	Data_Select, This four bit field is used to select which data is to be reported through the Data register and Data_Scale field. This field is required for any function that implements the Data register. The AN985B doesn't support Data_select.	0000b	RO
8	PME_En	PME_En, "1" enables the AN985B to assert PME#. When "0" disables the PME# assertion. This bit defaults to "0" if the function does not support PME# generation from D3cold.	0	RO
7~2	---	reserved.	000000b	RO
1,0	PWRS	PowerState, This two bit field is used both to determine the current power state of the AN985B and to set the AN985B into a new power state. The definition of this field is given below. 00b - D0 01b - D1 10b - D2 11b - D3hot If software attempts to write an unsupported, optional state to this field, the write operation must complete normally on the bus, however the data is discarded an no state change occurs.	00b	RO

CSR21(offset = 94h) - WTDP, The current working transmit descriptor pointer

Bit #	Name	Descriptions	Default Val	RW Type
31~0	WTDP	The current working transmit descriptor pointer for driver's double checking or other special purpose.	XXXX	RO

CSR22(offset = 98h) - WRDP, The current working receive descriptor pointer

Bit #	Name	Descriptions	Default Val	RW Type
31~0	WRDP	The current working receive descriptor pointer for driver's double checking or other special purpose.	XXXX	RO

CSR23(offset = 9ch) - TXBR, transmit burst count / time-out

Bit #	Name	Descriptions	Default Val	RW Type
31~21	---	reserved		
20~16	TBCNT	Transmit Burst Count	0	R/W

		After this number of consecutive successful transmit, transmit completed interrupt will be generated. Continuously do this function if no reset.		
11~0	TTO	Transmit Time-Out = (deferred time + back-off time). When the TDIE(bit28 of ACSR7) is set, the timer is decreased in unit of 2.56us(100M) or 25.6us(10M). If the timer expires before another packet transmit begin, then the TDIE interrupt will be generated.	0	R/W

CSR24(offset = a0h) - FROM, Flash ROM(also the boot ROM) port

Bit #	Name	Descriptions	Default Val	RW Type
31	Bra16_on	This bit is no effect when 3_LED scheme applied 1: no effect to bra[16] 0: bra[16] = fd/col LED path driver need to program this bit when 4_LED applied especially when boot rom read	1	R/W
30~28	---	reserved		
27	REN	read enable, clear if read data is ready in DATA, bit7-0 of FROM.	0	R/W
26	WEN	Write enable, cleared if write completed	0	R/W
25~8	ADDR	Flash ROM address	0	R/W
7~0	DATA	Read/Write data of flash ROM	0	R/W

CSR25(offset = a4h) - PAR0, physical address register 0, automatically recall from EEPROM

Bit #	Name	Descriptions	Default Val	RW Type
31~24	PAB3	physical address byte 3	XX	R/W
23~16	PAB2	physical address byte 2	XX	R/W
15~8	PAB1	physical address byte 1	XX	R/W
7~0	PAB0	physical address byte 0	XX	R/W

CSR26(offset = a8h) - PAR1, physical address register 1, automatically recall from EEPROM

Bit #	Name	Descriptions	Default Val	RW Type
31~24	---	reserved		
23~16	---	reserved		
15~8	PAB5	physical address byte 5	XX	R/W
7~0	PAB4	physical address byte 4	XX	R/W

for example, physical address = 00-00-e8-11-22-33

PAR0= 11 e8 00 00

PAR1= xx xx 33 22

PAR0 and PAR1 are readable, but can be written only if the receive state is in stopped(CSR5 bit19-17=000).

CSR27(offset = ach) - MAR0, multicast address register 0

Bit #	Name	Descriptions	Default Val	RW Type
31~24	MAB3	multicast address byte 3 (hash table 31:24)	XX	R/W
23~16	MAB2	multicast address byte 2 (hash table 23:16)	XX	R/W
15~8	MAB1	multicast address byte 1 (hash table 15:8)	XX	R/W
7~0	MAB0	multicast address byte 0 (hash table 7:0)	XX	R/W

CSR28(offset = b0h) - MAR1, multicast address register 1

Bit #	Name	Descriptions	Default Val	RW Type
31~24	MAB7	multicast address byte 7 (hash table 63:56)	XX	R/W
23~16	MAB6	multicast address byte 6 (hash table 55:48)	XX	R/W
15~8	MAB5	multicast address byte 5 (hash table 47:40)	XX	R/W
7~0	MAB4	multicast address byte 4 (hash table 39:32)	XX	R/W

MAR0 and MAR1 are readable, but can be written only if the receive state is in stopped(CSR5 bit19-17=000).

CSR_UAR0 (offset = b4h) - UAR0, unicast address register 0

Bit #	Name	Descriptions	Default Val	RW Type
31~24	UAB3	Unicast address byte 3 (hash table 31:24)	0	R/W
23~16	UAB2	Unicast address byte 2 (hash table 23:16)	0	R/W
15~8	UAB1	Unicast address byte 1 (hash table 15:8)	0	R/W
7~0	UAB0	Unicast address byte 0 (hash table 7:0)	0	R/W

CSR_UAR1(offset = b8h) - UAR1, unicast address register 1

Bit #	Name	Descriptions	Default Val	RW Type
31~24	UAB7	Unicast address byte 7 (hash table 63:56)	0	R/W
23~16	UAB6	Unicast address byte 6 (hash table 55:48)	0	R/W
15~8	UAB5	Unicast address byte 5 (hash table 47:40)	0	R/W
7~0	UAB4	Unicast address byte 4 (hash table 39:32)	0	R/W

CSR_Test (offset = fch)

Bit #	Name	Descriptions	Default Val	RW Type
31	speed	1: phy is in 100M mode 0: phy is in 10M mode	o	RO

30	duplex	1: full 0: helf	0	RO
29	Link	Link status 1: link OK 0: link down	0	RO
28				
27	ET	0: 9346 , 1:9366	0	RO
26	E2prom_Soft_load	Write 1 to reload e2prom	0	R/W
25~3	---	reserved		
2~0	chipmode	3'b111 : normal mode 3'b110 : monitor mode 3'b100 : HOME PNA mode 3'b001 : phy only mode 3'b101: HP94000tester mode (vaux ,vcc_detect will be internal forced to 1'b1 , and muxed with poweron_reset input and ssram_rdy)	3'b111	R/W

Function Event Register (Memory base offset 100h)

Bit #	Name	Descriptions	Default Val	RW Type
31~16	Reserved	Bits [31:16] are reserved in the CARDBUS Specification		
15	INTR_EVENT	This bit os used for as the interrupt bit. It is set when the Ethernet interrupt source is set, regardless of the mask value. It is cleared when the OS writes 1b to this field and the interrupt source has been serviced. Writing 0b to this field has no effect.	0	RLH*/W1C
14~5	Reserved	Bits [14:5] are reserved in the CARDBUS Specification		
4	GWAKE_EVENT	This bit is used for general wake-up. It is set when the Ehternet wake-up source is set, regardless of the mask value. Writing 1b to this field clears this bit and the PME Status bit in the PMCSR. Writing 0b to this field has no effect. Note that writing 1b to the PME Status bit in the PMCSR has the same effect.	0	R/W1C
3~0	Reserved	Bits [3:0] are reserved in the CARDBUS Specification		

Function Event Mask Register (Memory base offset 104h)

Bit #	Name	Descriptions	Default Val	RW Type

31~16	Reserved	Bits [31:16] are reserved in the CARDBUS Specification		
15	INTR_EN	The bit is the interrupt mask. When this bit equals 0b, it masks the Ethernet function INTA# line but has no effect on the Function Event register. The interrupt mask bit affects the INTA# masking.	1	R/W
14	WKUP_EN	This bit is the wake-up mask. When this bit equals 0b, it masks the Ethernet function CSTSCHG signal but has no effect on the Function Event register. This bit is dependent on bit 4 of this register.	0	R/W
13~5	Reserved	Bits [13:5] are reserved in the CARDBUS Specification		
4	GWAKE_EN	This bit is the general wake-up mask. When this bit equals 0b, it masks the Ethernet function wake-up events towards the CSTSCHG signal. It has no effect on the Function Event register. The AN985B can assert the CSTSCHG signal in the following configuration of masked bits: wake-up bit AND general wake-up bit, or PME Enable bit in the PMCSR register only.	0	R/W
3~0	Reserved	Bits [3:0] are reserved in the CARDBUS Specification		

Function Present State Register (Memory base offset 108h)

Bit #	Name	Descriptions	Default Val	RW Type
31~16	Reserved	Bits [31:16] are reserved in the CARDBUS Specification		
15	INTR_STATUS	This bit is used for interrupts. It reflects the current state of the Ethernet source of the interrupt regardless of the mask value. It is set when the Ethernet function has a pending interrupt and cleared when the software driver acknowledges all active interrupts through the SCB Command Word.	0	RO
14~5	Reserved	Bits [14:5] are reserved in the CARDBUS Specification		
4	WAKEUP_STATUS	This bit is used for general wake-up. It reflects the current state of the Ethernet source of CSTSCHG. It is a logical OR result of the gated three most significant bits in the PMDR: Link Status change bit is gated by the Link Status Change Wake Enable bit in the Configuration command. The Magic Packet bit is gated by the Magic Packet Wake-up disable bit in the Configuration command. The Interesting Packet bit is gated by the programmable filter command.	0	RO
3~0	Reserved	Bits [3:0] are reserved in the CARDBUS Specification		

Function Force Event Register (Memory base offset 10Ch)

Bit #	Name	Descriptions	Default Val	RW Type
31~16	Reserved	Bits [31:16] are reserved in the CARDBUS Specification		
15	INTA_FORCE	This bit is used for interrupts. Writing 1b in this field will set the interrupt bit in the Function Event register. If the INTA# pin is not masked, then it will also be activate. Writing 0b has no effect.	0	W
14~5	Reserved	Bits [14:5] are reserved in the CARDBUS Specification		
4	GWAKE_FORCE	This bit is used for general wake-up. Writing 1b in this field will set the CSTSCHG bit in the Function Event register. If the CSTSCHG pin is not masked, then it will also be activated. Writing 0b has no effect.	0	W
3~0	Reserved	Bits [3:0] are reserved in the CARDBUS Specification		

■ PHY REGISTER TABLE

Register 0 (MII Control)

BIT	NAME	DESCRIPTION	Read/Write	DEFAULT
15	Reset	1 = PHY Reset 0 = normal operation	R/W, SC	0
14	Loopback	1 = enable loopback 0 = disable loopback	R/W	0
13	Speed selection	1 = 100Mbps/s 0 = 10 Mb/s	R/W	Pin - see note
12	Autonegotiation enable	1 = enable autoneg 0 = disable autoneg	R/W	Pin – see note
11	Power down	1 = Power Down 0 = normal operation	R/W	0
10	Isolate	1 = isolate PHY from MII 0 = normal operation	R/W	0
9	Restart autonegotiation	1 = Restart Autoneg	R/W, SC	0
8	Duplex mode	1 = full, 0 = half	R/W	Pin – see note
7	Collision test	Not implemented	RO	0 - see note
6:0	Reserved		RO	0000000

SC Self Clearing

Reset Reset this port only. This will cause the following:

1. Restart the autonegotiation process.
2. Reset the registers to their default values. Note that this does not affect registers 20, 22, 30 or 31. These registers are not reset by this bit to allow test configurations to be written and then not affected by resetting the port.

Note: No reset is performed to analogue sections of the port. There is also no physical reset to any internal clock synthesisers or the local clock recovery oscillator which will continue to run throughout the reset period. However since the port is restarted and autoneg re-run the process of locking the frequency of the local oscillator (slave) to the reference oscillator (master) will be repeated as it is at the start of any link initialisation process.

Loopback Loop back of transmit data to receive via a path as close to the wire as possible. When set inhibits actual transmission on the wire.

Speed selection Forces speed of Phy only when autonegotiation is disabled. The default state of this bit will be determined by a power-up configuration pin in this case. Otherwise it defaults to 1. See Annex A.

Auto-neg enable Defaults to pin programmed value. When cleared allows forcing of speed and duplex settings. When set (after being cleared) causes re-start of autoneg process. Pin programming at power-up allows it to come up disabled and for software to write the desired capability before allowing the first negotiation to commence. See Annex A.

Restart Negotiation only has effect when autonegotiating. Restarts state machine.

Power down Has no effect in this device. Test mode power down modes may be implemented in other specific modules.

Isolate Puts RMII receive signals into high impedance state and ignores transmit signals.

Duplex mode When bit12 is cleared (i.e. autoneg disabled), this bit forces full duplex (bit = 1) or half duplex (bit = 0).

Collision test Always 0 because collision signal is not implemented.

Register 1 (Status):

BIT	NAME	DESCRIPTION	Read/Write	Default
15	100 BASE T4	Not supported	RO	0
14	100BASE-X Full Duplex	1 = PHY is 100BASE-X full duplex capable 0 = PHY is not 100BASE-X full duplex capable	RO	1 (see Annex A)
13	100BASE-X Half Duplex	1 = PHY is 100BASE-X half duplex capable 0 = PHY is not 100BASE-X half duplex capable	RO	1 (see Annex A)
12	10Mbps/s Full Duplex	1 = PHY is 10Mbps/s Full duplex capable 0 = PHY is not 10Mbps/s Full duplex capable	RO	1 (see Annex A)
11	10 Mb/s Half Duplex	1 = PHY is 10Mbps/s Half duplex capable 0 = PHY is not 10Mbps/s Half duplex capable	RO	1 (see Annex A)
10	100BASE-T2 full duplex	Not supported	RO	0
9	100BASE-T2 half duplex	Not supported	RO	0
8-7	Reserved		RO	00
6	MF Preamble Suppression	1 = PHY can accept management frames with preamble suppression 0 = PHY cannot accept management frames with preamble suppression	RO	1
5	Autoneg Complete	1 = autoneg completed, 0 = autoneg incomplete	RO	0
4	Remote Fault	1 = remote fault detected, 0 = no remote fault detected	RO, LH	0
3	Autoneg Ability	1 = PHY can auto-negotiate, 0 = PHY cannot auto-negotiate	RO	1
2	Link Status	1 = link is up, 0 = link is down	RO, LL	0
1	Jabber Detect	1 = jabber condition detected	RO, LH	0(see note)
0	Extended Capability	1 = extended register capabilities, 0 = basic register set capabilities only	RO	1

LL	Latch Low
LH	Latch High
Jabber detect	Only used in 10Base-T mode. Reads as 0 in 100Base-TX mode.

Register 2 and 3

Each PHY has a unique identifier, which is assigned to the device.
The identifier contains a total of 32 bits, which consists of the following: 22 bits of a 24bit organisationally unique identifier (OUI) for the manufacturer (3Com); a 6-bit manufacturer's model number; a 4-bit manufacturer's revision number. For an explanation of how the OUI maps to the register, please refer to IEEE 802-1990 clause 5.1
There is physically only one of each of these registers for all six network (MDI) ports. When

reading this register the port number is ignored.

Register 2

BIT	NAME	DESCRIPTION	READ/WRITE	DEFAULT
15:0	PHY_ID[31-16]	3Com OUI (bits 3-18)	RO	001D(Hex)

Register 3

BIT	NAME	DESCRIPTION	READ/WRITE	DEFAULT
15:10	PHY_ID[15-10]	3Com OUI (bits 19-24)	RO	001001(bin)
9:4	PHY_ID[9-4]	Manufacturer's Model Number (bits 5-0)	RO	000001(bin)
3:0	PHY_ID[3-0]	Revision Number (bits 3-0); Register 3, bit 0 is LS bit of PHY Identifier	RO	0001(bin)

This uses the OUI of ADMtek, device type of 1 and rev 0.

Register 4

BIT	NAME	DESCRIPTION	READ/WRITE	DEFAULT
15	Next Page	1 = Device set to use Next Page, 0 = Device not set to use Next Page	R/W	0
14	Reserved		RO	0
13	Remote Fault	1 = Local remote fault sent to link partner 0 = no fault detected	R/W	0
12:11	Not implemented	Technology ability bits A7-A6	RO	00
10	Pause	Technology ability bit A5	R/W	0
9	Not implemented	Technology ability bit A4	RO	0
8	100BASE-TX full duplex	Technology ability bit A3 1 = Unit is capable of Full Duplex 0 = Unit is not capable of Full Duplex	R/W	0 (see Annex A)
7	100BASE-TX half duplex	Technology ability bit A2 1 = Unit is capable of Half Duplex 0 = Unit is not capable of Half Duplex 100BASE-TX	R/W	0 (see Annex A)
6	10BASE-T full duplex	Technology ability bit A1 1 = Unit is capable of Full Duplex 10BASE-T 0 = Unit is not capable of Full Duplex 10BASE-T	R/W	0 (see Annex A)
5	10BASE-T half duplex	Technology ability bit A0 1 = Unit is capable of Half Duplex 10BASE-T 0 = Unit is not capable of Half Duplex 10BASE-T	R/W	0 (see Annex A)
4:0	Selector Field	Identifies type of message being sent. Currently only one value is defined.	RO	00001

Register 5

The register is used to view the advertised capabilities of the link partner once autonegotiation is complete. The contents of this register should not be relied upon unless register 1 bit 5 is set (autoneg complete). After negotiation this register should contain a copy of the link partner's register 4. All bits are therefore defined in the same way as for register 4.
All bits are read only.
This register is used for Base Page code word only.

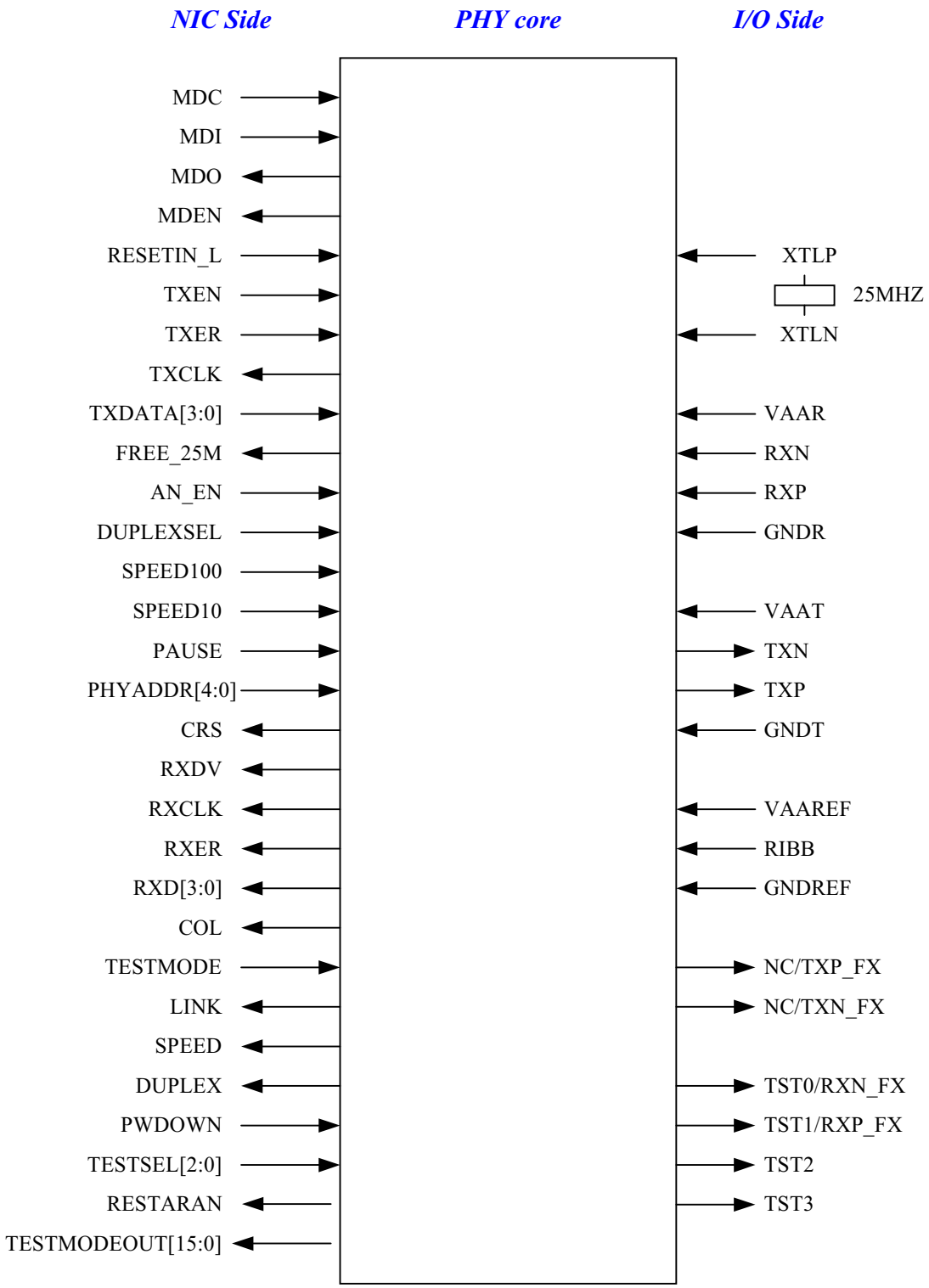
Base Page Register Format

BIT	NAME	DESCRIPTION	READ/WRITE	DEFAULT
15	Next Page	1 = Link Partner is requesting Next Page function 0 = Base Page is requested	RO	0
14	Acknowledge	Link Partner acknowledgement bit	RO	0
13	Remote Fault	Link Partner is indicating a fault	RO	0
12:5	Technology Ability	Link Partner technology ability field.	RO	00(hex)
4:0	Selector Field	Link Partner selector field	RO	00000

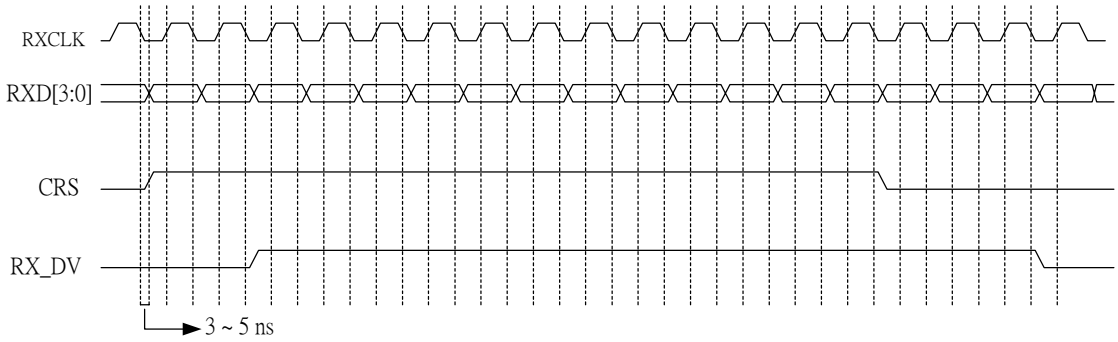
Register 6

BIT	NAME	DESCRIPTION	READ/WRITE	DEFAULT
15:5	Reserved		RO	000(hex)
4	Parallel Detection Fault	1 = Local Device Parallel Detection Fault 0 = No fault detected	RO, LH	0
3	Link Partner Next Page Able	1 = Link Partner is Next Page Able 0 = Link Partner is not Next Page Able	RO	0
2	Next Page Able	1 = Local device is Next Page Able 0 = Local device is not Next Page Able	RO	1
1	Page Received	1 = A New Page has been received 0 = A New Page has not been received	RO, LH	0
0	Link Partner Autonegotiation Able	1 = Link Partner is Autonegotiation able 0 = Link Partner is not Autonegotiation able	RO	0

LH Latch High


NIC Side
PHY core
I/O Side
MDC
MDI
MDO
MDEN
RESETIN_L
TXEN
TXER
TXCLK
TXDATA[3:0]
FREE_25M
AN_EN
DUPLEXSEL
SPEED100
SPEED10
PAUSE
PHYADDR[4:0]
CRS
RXDV
RXCLK
RXER
RXD[3:0]
COL
TESTMODE
LINK
SPEED
DUPLEX
PWDOWN
TESTSEL[2:0]
RESTARAN
TESTMODEOUT[15:0]
XTLP
25MHZ
XTLN
VAAR
RXN
RXP
GNDR
VAAT
TXN
TXP
GNDT
VAAREF
RIBB
GNDREF
NC/TXP_FX
NC/TXN_FX
TST0/RXN_FX
TST1/RXP_FX
TST2
TST3

■ TIMING:



■ DESCRIPTORS AND BUFFER MANAGEMENT

The AN985B provides receive and transmit descriptors for packet buffering and management.

■ RECEIVE DESCRIPTOR

□ Receive Descriptor Table

	31					0
RDES0	Own	Status				
RDES1		---	Control	Buffer2 byte-count		Buffer1 byte-count
RDES2	Buffer1 address (DW boundary)					
RDES3	Buffer2 address (DW boundary)					

Descriptors and receive buffers addresses must be long-word alignment

□ Receive Descriptor Descriptions

RDES0

Bit #	Name	Descriptions
31	OWN	Own bit 1: indicate the new receiving data can be put into this descriptor 0: Host does not move the receiving data out yet.

30-16	FL	Frame length, including CRC. This field is valid only in last descriptor
15	ES	Error summary, OR of the following bit 0: overflow 1: CRC error 6: late collision 7: frame too long 11: runt packet 14: descriptor error This field is valid only in last descriptor.
14	DE	Descriptor error. This bit is valid only in last descriptor 1: the current receiving packet is not able to put into the current valid descriptor. This packet is truncated.
13-12	DT	Data type. 00: normal 01: MAC loop-back 10: Transceiver loop-back 11: remote loop-back These bits are valid only in last descriptor
11	RF	Runt frame (packet length < 64 bytes). This bit is valid only in last descriptor
10	MF	Multicast frame. This bit is valid only in last descriptor
9	FS	First descriptor.
8	LS	Last descriptor.
7	TL	Too long packet (packet length > 1518 bytes). This bit is valid only in last descriptor
6	CS	Late collision. Set when collision is active after 64 bytes. This bit is valid only in last descriptor
5	FT	Frame type. This bit is valid only in last descriptor. 1: Ethernet type 0: 802.3 type
4	RW	Receive watchdog (refer to CSR15, bit 4). This bit is valid only in last descriptor.
3	reserved	Default = 0
2	DB	Dribble bit. This bit is valid only in last descriptor Packet length is not integer multiple of 8-bit.
1	CE	CRC error. This bit is valid only in last descriptor
0	OF	Overflow. This bit is valid only in last descriptor

RDES1

Bit #	Name	Descriptions
31~26	---	reserved
25	RER	Receive end of ring indicates this descriptor is last, return to base address of descriptor
24	RCH	Second address chain Use for chain structure. Indicates the buffer2 address is the next descriptor address. Ring mode takes precedence over chained mode
23~22	---	reserved
21~11	RBS2	Buffer 2 size (DW boundary)
10~ 0	RBS1	Buffer 1 size (DW boundary)

RDES2

Bit #	Name	Descriptions
31~0	RBA1	Receive Buffer Address 1. This buffer address should be double word aligned.

RDES3

Bit #	Name	Descriptions
31~0	RBA2	Receive Buffer Address 2. This buffer address should be double word aligned.

■ TRANSMIT DESCRIPTOR

□ Transmit Descriptor Table

	31			0
TDES0	Own	Status		
TDES1	Control	Buffer2 byte-count	Buffer1 byte-count	
TDES2	Buffer1 address			
TDES3	Buffer2 address			

Descriptor addresses must be longword alignment

□ Transmit Descriptor Descriptions

TDES0

Bit #	Name	Descriptions
31	OWN	Own bit 1: Indicate this descriptor is ready to transmit 0: Old data not for transmission
30-24	---	Reserved
23-22	UR	Under-run count
21-16	---	Reserved
15	ES	Error summary, OR of the following bit 1: under-run error 8: excessive collision 9: late collision 10: no carrier 11: loss carrier 14: jabber time-out
14	TO	Transmit jabber time-out
13-12	-----	Reserved
11	LO	Loss carrier
10	NC	No carrier
9	LC	Late collision
8	EC	Excessive collision
7	HF	Heartbeat fail
6-3	CC	Collision count
2	-----	Reserved
1	UF	Under-run error
0	DE	Deferred

TDES1

Bit #	Name	Descriptions
31	IC	Interrupt completed
30	LS	Last descriptor
29	FS	First descriptor
28,27	---	Reserved
26	AC	Disable add CRC function
25	TER	End of Ring

24	TCH	2nd address chain Indicate the buffer2 address is the next descriptor address
23	DPD	Disable padding function
22	---	Reserved
21-11	TBS2	Buffer 2 size
10-0	TBS1	Buffer 1 size

TDES2

Bit #	Name	Descriptions
31~0	BA1	Buffer Address 1. Without any limitation on the transmission buffer address.

TDES3

Bit #	Name	Descriptions
31~0	BA2	Buffer Address 2. Without any limitation on the transmission buffer address.

FUNCTIONAL DESCRIPTIONS

■ NETWORK PACKET BUFFER MANAGEMENT

■ DESCRIPTOR STRUCTURE TYPES

For networking operation, the AN985B transmits the data packet from transmit buffers in host memory to AN985B's transmit FIFO and receives the data packet from AN985B's receive FIFO to receive buffers in host memory. The descriptors that the AN985B supports to build in host memory are used as the pointers of these transmit and receive buffers.

There are two structure types for the descriptor, **Ring and Chain**, supported by the AN985B and are shown as below. The type selections are controlled by the bit24 of RDES1 and the bit24 of TDES1.

The transmitting and receiving buffers are physically built in host memory. Any buffer can contain either a whole packet or just part of a packet. But it can't contain more than one packet.

□ Ring structure:

There are two buffers per descriptor in the ring structure. Support receive early interrupt.

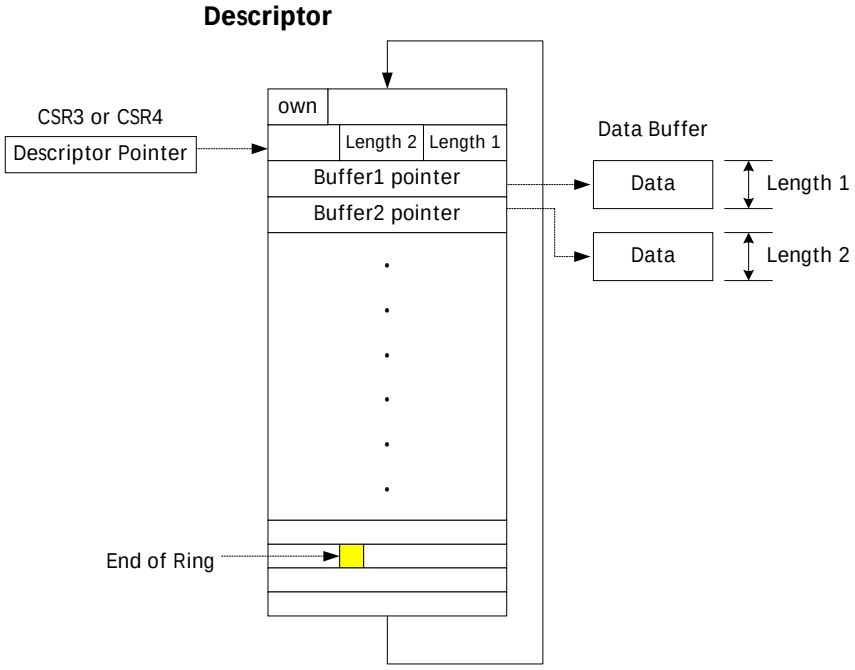


Fig.3 Ring structure of frame buffer

□ Chain structure

There is only one buffer per descriptor in chain structure.

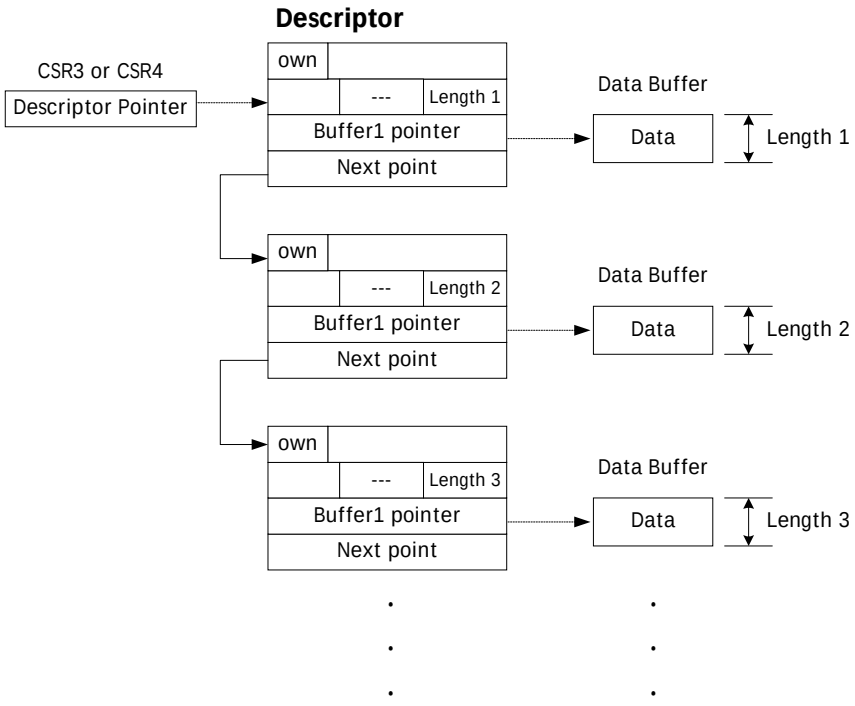


Fig.4 Chain structure of frame buffer

■ THE POINT OF DESCRIPTOR MANAGEMENT

OWN bit = 1, ready for network side access

OWN bit = 0, ready for host side access

□ Transmit Descriptor Pointers

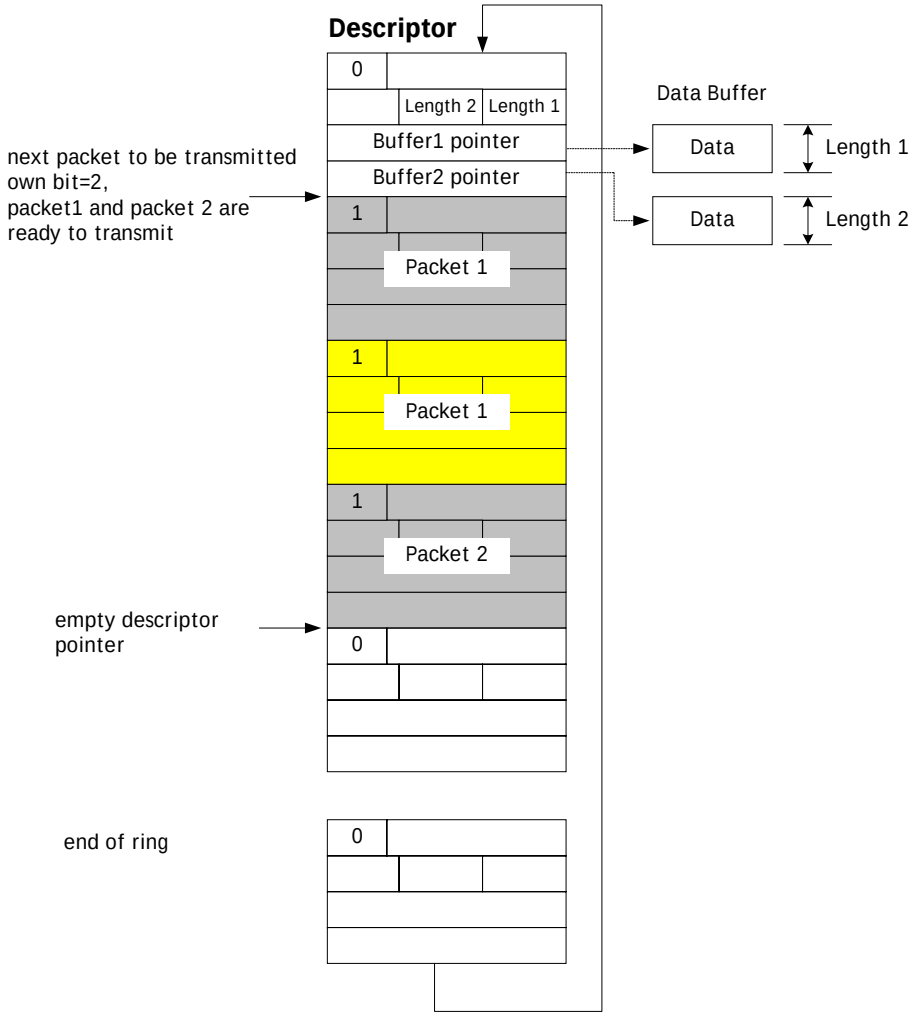


Fig.5 Transmit pointers for descriptor management

□ Receive Descriptor Pointers

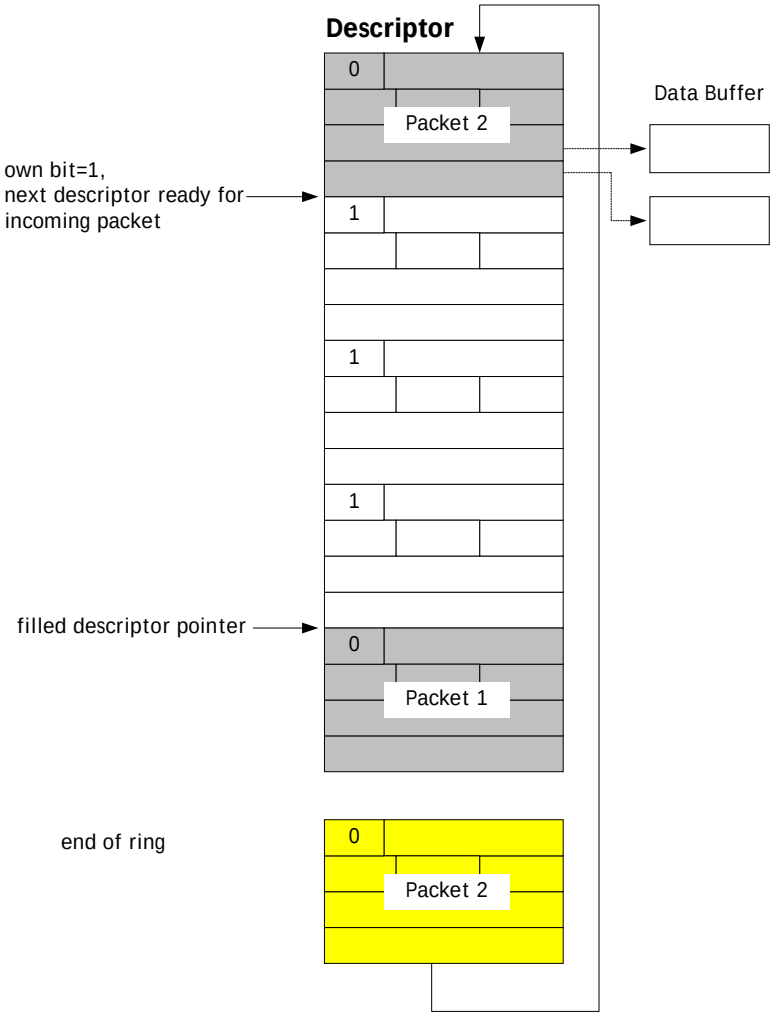
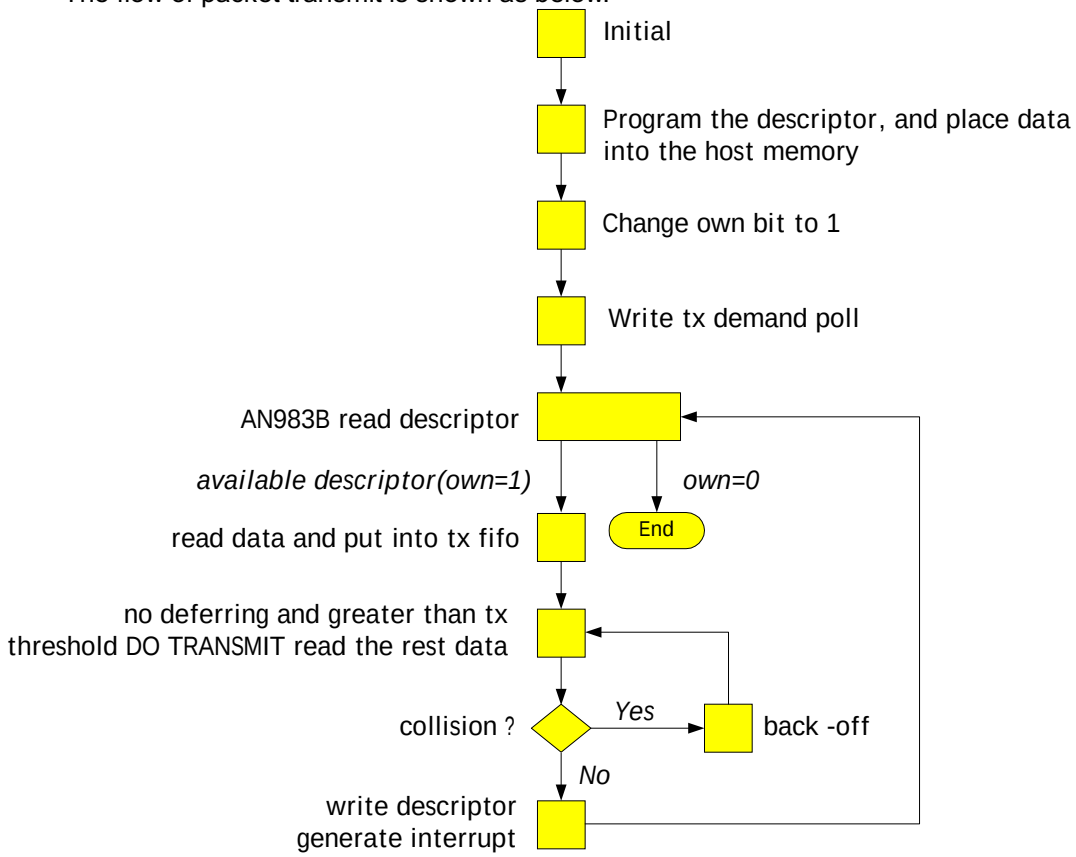


Fig.6 Receive pointers for descriptor management

TRANSMIT SCHEME AND TRANSMIT EARLY INTERRUPT

TRANSMIT FLOW

The flow of packet transmit is shown as below.



TRANSMIT PRE-FETCH DATA FLOW

>> Transmit FIFO size=2K-byte

>> Two packets in the FIFO at the same time

>> Meet the transmit min. back-to-back

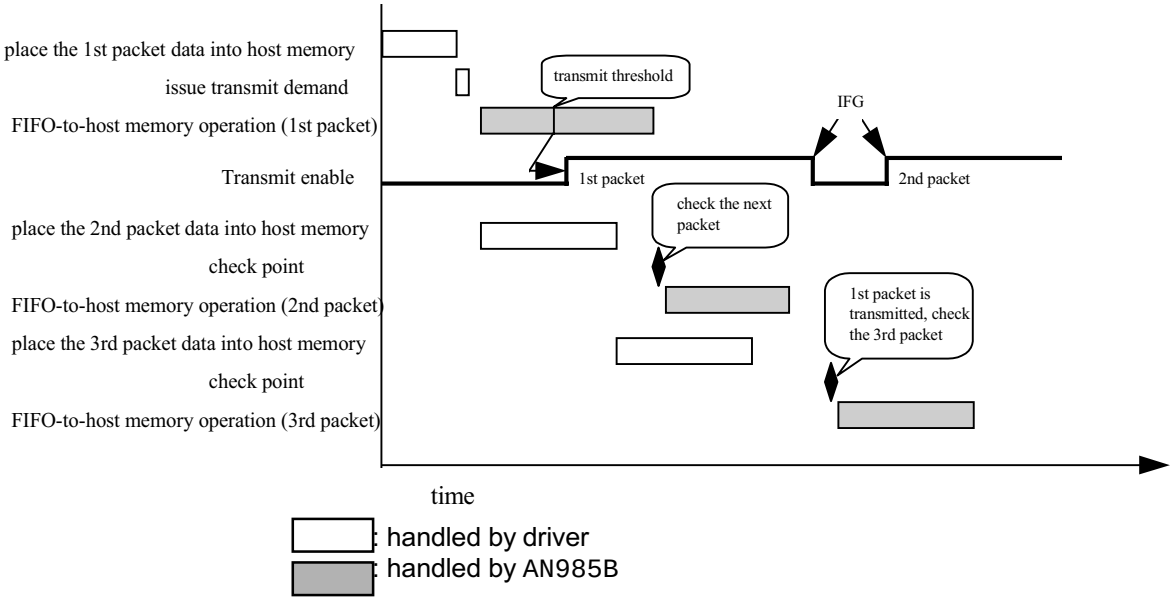


Fig.7 Transmit data flow of pre-fetch data

■ TRANSMIT EARLY INTERRUPT SCHEME

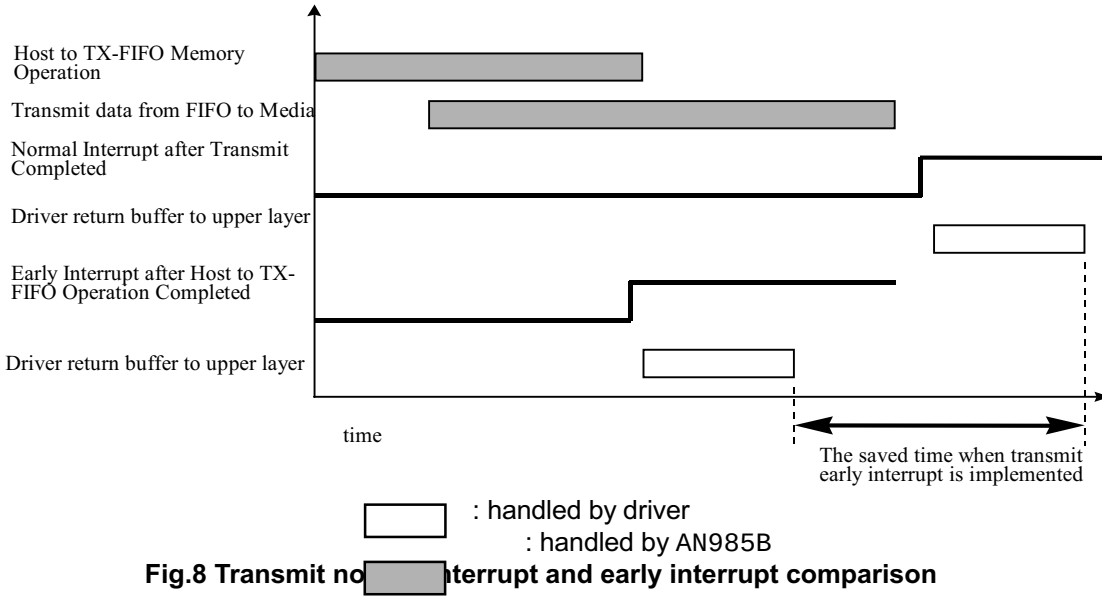


Fig.8 Transmit no terrupt and early interrupt comparison

■ RECEIVE SCHEME AND RECEIVE EARLY INTERRUPT SCHEME

The following figure shows the difference of timing without early interrupt and with early interrupt.

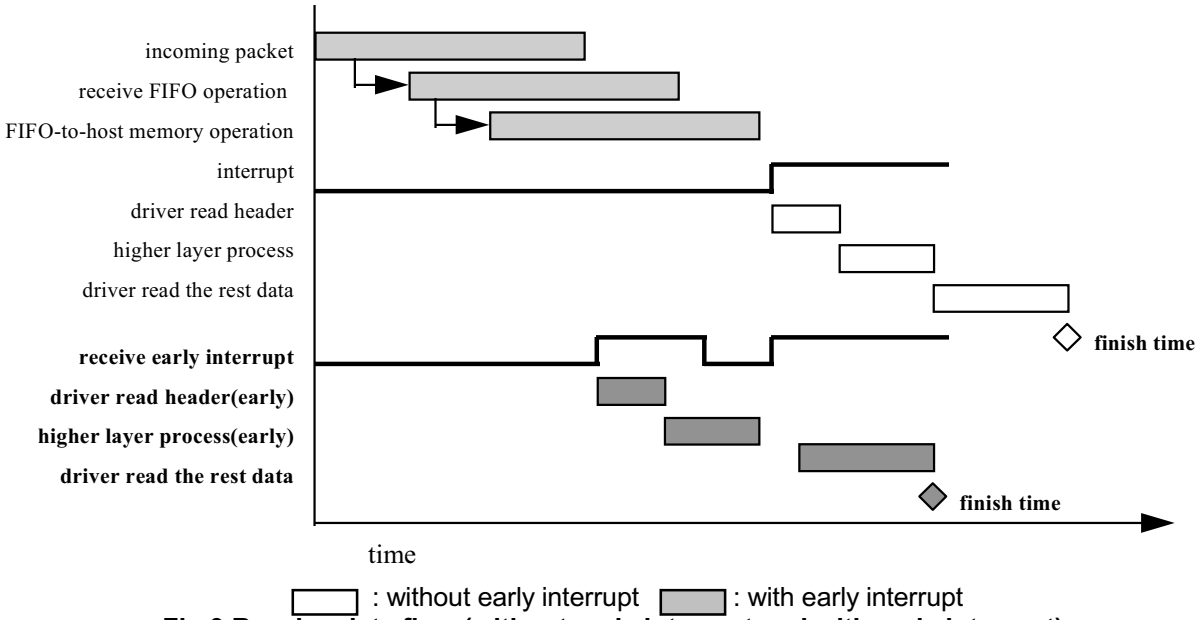


Fig.9 Receive data flow (without early interrupt and with early interrupt)

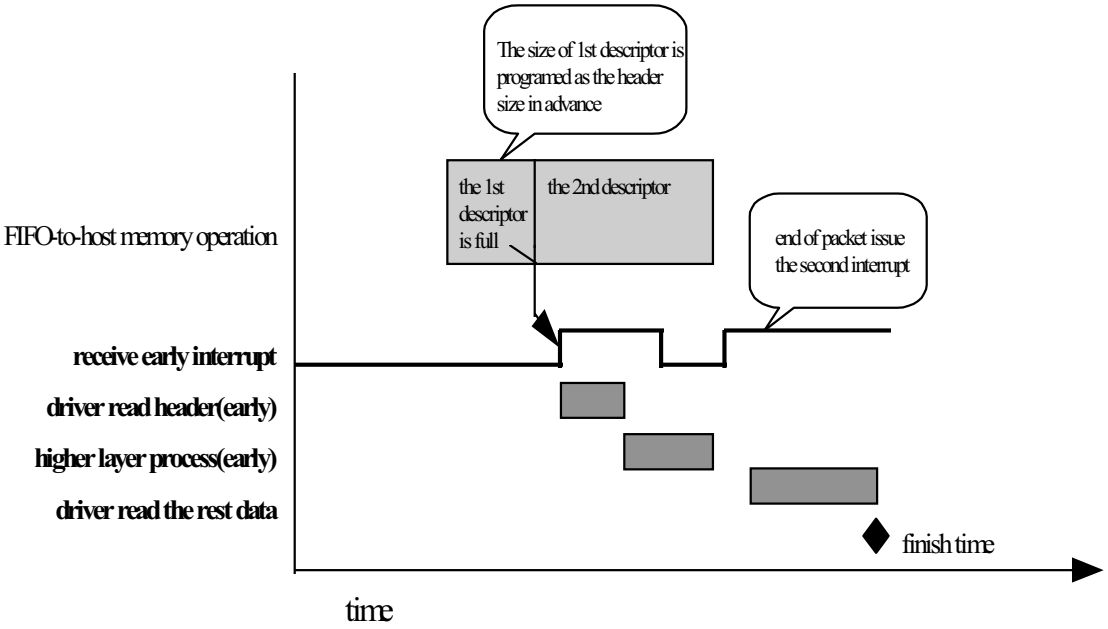


Fig.10 Detailed Receive Early interrupt flow

■ NETWORK OPERATION

■ MAC OPERATION

In the MAC (Media Access Control) portion of AN985B, it incorporates the essential protocol requirements for operating as an IEEE802.3 and Ethernet compliant node.

□ Format

Field	Description
Preamble	A 7-byte field of (10101010b)
Start Frame Delimiter	A 1-byte field of (10101011b)
Destination Address	A 6-byte field
Source Address	A 6-byte field
Length/Type	A 2-byte field indicated the frame is in IEEE802.3 format or Ethernet format. IEEE802.3 format: 0000H ~ 05DCH for Length field Ethernet format: 05DD ~ FFFFH for Type field
Data	*46 ~ 1500 bytes of data information
CRC	A 32-bit cyclic redundant code for error detection

*Note: If padding is disabled(TDES1 bit23), the data field may be shorter than 46 bytes.

□ Transmit Data Encapsulation

The differences between the encapsulation and a MAC frame while operating in the 100BASE-TX mode are listed as follow:

1. The first byte of the preamble is replaced by the JK code according to the IEE802.3u, clause 24.

2. After the CRC field of the MAC frame, the AN985B insert the TR code according to the IEE802.3u, clause 24.

□ Receive Data Decapsulation

When operate in 100BASE-TX mode the AN985B detects a JK code for a preamble as well as a TR code for the packet end. If a JK code is not detected, the AN985B will abort this frame receiving and wait for a new JK code detection. If a TR code is not detected, the AN985B will report a CRC error.

□ Deferring

The Inter-Frame Gap (IFG) time is divided into two parts:

1. IFG1 time (64-bit time): If a carrier is detected on the medium during this time, the AN985B will reset the IFG1 time counter and restart to monitor the channel for an idle again.

2. IFG2 time (32-bit time): After counting the IFG2 time the AN985B will access the channel even though a carrier has been sensed on the network.

□ Collision Handling

The scheduling of re-transmissions are determined by a controlled randomization process called “truncated binary exponential back-off”. At the end of enforcing a collision (jamming), the AN985B delays before attempting to re-transmit the packet. The delay is an integer multiple of slot time. The number of slot times to delay before the nth re-transmission attempt is chosen as a uniform distributed integer r in the range:

$$0 \leqq r < 2^k \quad \text{where} \quad k = \min(n, 10)$$

■ TRANSCEIVER OPERATION

In the transceiver portion of the AN985B, it integrates the IEEE802.3u compliant functions of PCS(physical coding sub-layer), PMA(physical medium attachment) sub-layer, and PMD(physical medium dependent) sub-layer for 100BASE-TX, and the IEEE802.3 compliant functions of Manchester encoding/decoding and transceiver for 10BASE-T. All the functions and operation schemes are described in the following sections.

□ 100BASE-TX Transmit Operation

Regarding the 100BASE-TX transmission, the transceiver provides the transmission functions of PCS, PMA, and PMD for encoding of MII data nibbles to five-bit code-groups (4B/5B), scrambling, serialization of scrambled code-groups, converting the serial NRZ code into NRZI code, converting the NRZI code into MLT3 code, and then driving the MLT3 code into the category 5 Unshielded Twisted Pair cable through an isolation transformer with the turns ratio of 1: 1.

- **Data code-groups Encoder:** In normal MII mode application, the transceiver receives nibble type 4B data via the TxD0~3 inputs of the MII. These inputs are sampled by the transceiver on the rising edge of Tx-clk and passed to the 4B/5B encoder to generate the 5B code-group used by 100BASE-TX.

- **Idle code-groups:** In order to establish and maintain the clock synchronization, the transceiver need to keep transmitting signals to medium. The transceiver will generate Idle code-groups for transmission when there is no real data want to be sent by MAC.

- **Start-of-Stream Delimiter-SSD (/J/K/):** In a transmission stream, the first 16 nibbles are MAC preamble. In order to let partner delineate the boundary of a data transmission sequence and to authenticate carrier events, the transceiver will replace the first 2 nibbles of the MAC preamble with /J/K/ code-groups.

- **End-of-Stream Delimiter-ESD (/T/R/):** In order to indicate the termination of the normal data transmissions, the transceiver will insert 2 nibbles of /T/R/ code-group after the last nibble of FCS.

- **Scrambling:** All the encoded data(including the idle, SSD, and ESD code-groups) is passed to data scrambler to reduce the EMI and spread the power spectrum using a 10-bit scrambler seed loaded at the beginning.

- **Data conversion of Parallel to Serial, NRZ to NRZI, NRZI to MLT3:** After scrambled, the transmission data with 5B type in 25MHz will be converted to serial bit stream in 125HMz by the parallel to serial function. After serialized, the transmission serial bit stream will be further converted from NRZ to NRZI format. This NRZI conversion function can be bypassed, if the bit 7 of XR10 register is cleared as 0. After NRZI converted, the NRZI bit stream is passed through MLT3 encoder to generate the TP-PMD specified MLT3 code. With this MLT3 code, it lowers the frequency and reduces the energy of the transmission signal in the UTP cable and also makes the system easily to meet the FCC specification of EMI.

- **Wave-Shaper and Media Signal Driver:** In order to reduce the energy of the harmonic frequency of transmission signals, the transceiver provides the wave-shaper prior the line driver to smooth but keep symmetric the rising/falling edge of transmission signals. The wave-shaped signals include the 100BASE-TX and 10BASE-T both are passed to the same media signal driver. This design can simplify the external magnetic connection with single one.

□ 100BASE-TX Receiving Operation

Regarding the 100BASE-TX receiving operation, the transceiver provides the receiving functions of PMD, PMA, and PCS for receiving incoming data signals through category 5 UTP cable and an isolation transformer with turns ratio of 1: 1. It includes the adaptive equalizer and baseline wander, data conversions of MLT3 to NRZI, NRZI to NRZ and serial to parallel, the PLL for clock and data recovery, the de-scrambler, and the decoder of 5B/4B.

- **Adaptive Equalizer and Baseline Wander:** Since the high speed signals over the unshielded (or shielded) twisted Pair cable will induce the amplitude attenuation and phase shifting. Furthermore, these effects are depends on the signal frequency, cable type, cable length and the connectors of the cabling. So a reliable adaptive equalizer and baseline wander to compensate all the amplitude attenuation and phase shifting are necessary. In the transceiver, it provides the robust circuits to

perform these functions.

- **MLT3 to NRZI Decoder and PLL for Data Recovery:** After receiving the proper MLT3 signals, the transceiver converts the MLT3 to NRZI code for further processing. After adaptive equalizer, baseline wander, and MLT3 to NRZI decoder, the compensated signals with NRZI type in 125MHz are passed to the Phase Lock Loop circuits to extract out the original data and the synchronous clock.

- **Data Conversions of NRZI to NRZ and Serial to Parallel:** After data recovered, the signals will be passed to the NRZI to NRZ converter to generate the 125MHz serial bit stream. This serial bit stream will be packed to parallel 5B type for further processing. The NRZI to NRZ conversion can be bypassed, if the bit 7 of XR10 register is cleared as 0.

- **De-scrambling and Decoding of 5B/4B:** The parallel 5B type data is passed to de-scrambler and 5B/4B decoder to return their original MII nibble type data.

- **Carrier sensing:** Carrier Sense(CRS) signal is asserted when the transceiver detects any 2 non-contiguous zeros within any 10bit boundary of the receiving bit stream. CRS is de-asserted when ESD code-group or Idle code-group is detected. In half duplex mode, CRS is asserted during packet transmission or receive. But in full duplex mode, CRS is asserted only during packet reception.

□ 10BASE-T Transmission Operation

It includes the parallel to serial converter, Manchester Encoder, Link test function, Jabber function and the transmit wave-shaper and line driver described in the section of "Wave-Shaper and Media Signal Driver" of "100BASE-T Transmission Operation". It also provides Collision detection and SQE test for half duplex application.

□ 10BASE-T Receive Operation

It includes the carrier sense function, receiving filter, PLL for clock and data recovering, Manchester decoder, and serial to parallel converter.

□ Loop-back Operation of transceiver

The transceiver provides internal loop-back(also called transceiver loop-back) operation for both the 100BASE-TX and 10BASE-T operations. The loop-back operation can be enabled by setting bit 14 of XR0 register to 1. In this loop-back operation, the TX± and RX± lines are isolated from the media. The transceiver also provides remote loop-back operation for 100BASE-TX operation. The remote loop-back operation can be enabled by setting bit 9 of XR10 register to 1.

In the 100BASE-TX internal loop-back operation, the data comes from the transmit output of NRZ to NRZI converter then loop-back to the receive path into the input of NRZI to NRZ

converter.

In the 100BASE-TX remote loop-back operation, the data is received from RX± pins through receive path to the output of data and clock recover and then loop-back to the input of NRZI to MLT3 converter of transmit path then transmit out to the medium via the transmit line drivers.

In the 10BASE-T loop-back operation, the data is through transmit path and loop-back from the output of the Manchester encoder into the input of Phase Lock Loop circuit of receive path.

□ Full Duplex and Half Duplex Operation of Transceiver

The transceiver can operate for either full duplex or half duplex network application. In full duplex, both transmit and receive can be operated simultaneously. Under full duplex mode, collision (COL) signal is ignored and carrier sense (CRS) signal is asserted only when the transceiver is receiving.

In half duplex mode, either transmit or receive can be operated at one time. Under half duplex mode, collision signal is asserted when transmit and receive signals collided and carrier sense asserted during transmission and reception.

□ Auto-Negotiation Operation

The Auto-Negotiation function is designed to provide the means to exchange information between the transceiver and the network partner to automatically configure both to take maximum advantage of their abilities, and both are setup accordingly. The Auto-Negotiation function can be controlled through bit 12 of XR0 register.

The Auto-Negotiation exchanges information with the network partner using the Fast Link Pulses(FLPs) - a burst of link pulses. There are 16 bits of signaling information contained in the burst pulses to advertise all remote partner's capabilities which are determined by the register of XR4. According to this information they find out their highest common capability by following the priority sequence as below:

1. 100BASE-TX full duplex

2. 100BASE-TX half duplex

3. 10BASE-T full duplex

4. 10BASE-T half duplex

During power-up or reset, if Auto-Negotiation is found enabled then FLPs will be transmitted and the Auto-Negotiation function will process. Otherwise, the Auto-Negotiation will not occur until the bit 12 of XR0 register is set to 1. When the Auto-Negotiation is disabled, then the Network Speed and Duplex Mode are selected by programming XR0 register.

□ Power Down Operation

To reduce the power consumption the transceiver is designed with power down feature which can save the power consumption significantly. Since the power supply of the 100BASE-TX and 10BASE-T circuits are separated, the transceiver can turn off the circuit of either the 100BASE-TX or 10BASE-T when the other one of them is operating.

■ FLOW CONTROL IN FULL DUPLEX APPLICATION

The PAUSE function operation is used to inhibit transmission of data frames for a specified period of time. The AN985B supports full duplex protocol of IEEE802.3x. To support PAUSE function, the AN985B implements the MAC Control Sub-layer functions to decode the MAC Control frames received from MAC control clients and execute the relative requests accordingly. When the Full Duplex mode and PAUSE function are selected after Auto-Negotiation completed (refer the register of XCVR configuration information of XR8), then the AN985B enables the PAUSE function for flow control of full duplex application. In this section we will describe how the AN985B implements the PAUSE function.

□ MAC Control Frame and PAUSE Frame

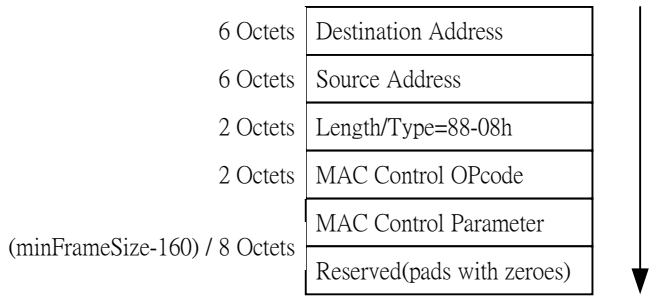


Fig.11 MAC Control Frame Format

The MAC Control frame is distinguished from other MAC frames only by their Length/Type field identifier. The MAC Control Opcode defined in MAC Control Frame format for PAUSE function is 0001h. Besides, the PAUSE time is specified in the MAC Control Parameters field with 2 Octets, unsigned integer, in the units of Slot-Times. The range of possible PAUSE time is 0 to 65535 Slot-Times.

So, a valid PAUSE frame issued by a MAC control client(could be a switch or a bridge) will contains:

- The destination address is set equal to the globally assigned 48 bit mulitcast address 01-80-C2-00-00-01, or equal to the unicast address which the MAC control client wishes to inhibit its transmission of data frames.
- Filled the MAC Control Opcode field with 0001h.
- 2 Octets of PAUSE time specified in the MAC Control parameter field to indicate the length of time for which the destination is wished to inhibit data frame transmission.

□ Receive Operation for PAUSE function

Upon reception of a valid MAC Control frame, the AN985B will start a timer for the length of time specified by the MAC Control Parameters field. When the timer value reaches zero then the AN985B ends PAUSE state. However, a PAUSE frame should not affect the transmission of a frame that has been submitted to the MAC(started Transmit out of the MAC and can't be interrupted). On the other hand, the AN985B shall not begin to transmit a frame more than one Slot-Times after received a valid PAUSE frame with a non-zero PAUSE time. If the AN985B receives a PAUSE frame with a zero PAUSE time value, then the AN985B ends the PAUSE state immediately.

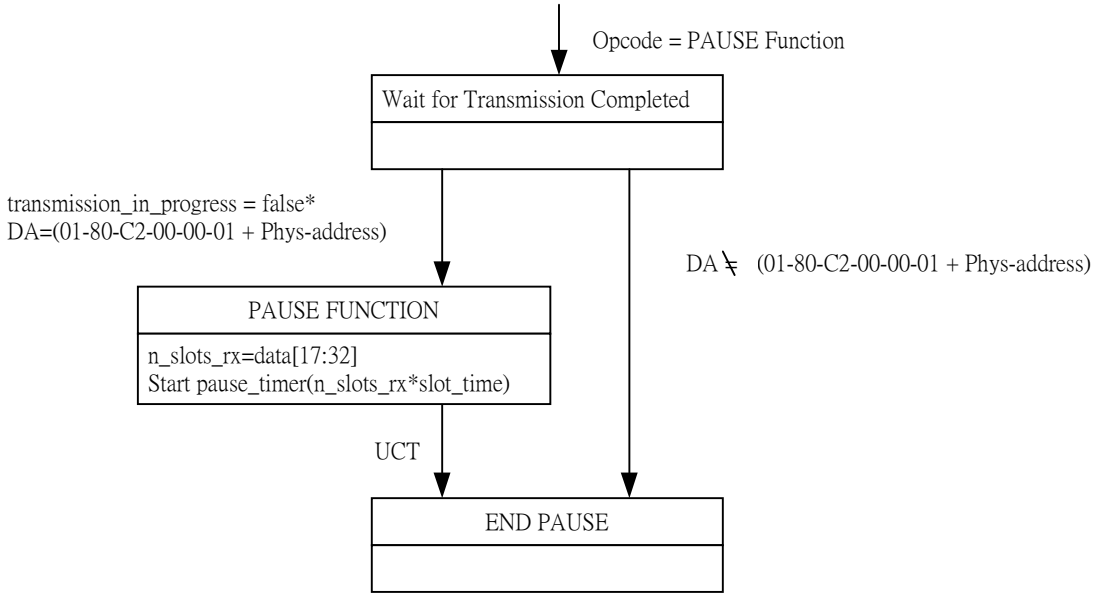


Fig.12 PAUSE operation receive state diagram

■ LED DISPLAY OPERATION

The AN985B provides two LED schemes one is three-LED which provides display pins for Link test status/Activity status, Speed mode, and Full duplex/Collision status. These pins can directly drive LED device, the other is four-LED scheme which provides link100, link10, act, fd/col. The detail descriptions about the operation are described in the Pin Description

section.

RESET OPERATION

RESET WHOLE CHIP

There are two ways to reset the AN985B. First, hardware reset, the AN985B can be reset via RST# pin. For ensuring proper reset operation, at least 100μs active Reset input signal is required. Second, software reset, when bit 0 of CSR0 register is set to 1, the AN985B will reset entire circuits and register to default value then clear the bit 0 of CSR0 to 0.

■ RESET TRANSCEIVER ONLY

When bit 15 of XR0 register is set to 1, the transceiver will reset entire circuits and register contains to default value then clear the bit 15 of XR0 to 0.

■ WAKE ON LAN FUNCTION

The AN985B can assert a signal to wake up the system when it received a Magic Packet from the network. The Wake on LAN operation is described as follow.

■ THE MAGIC PACKET FORMAT:

- Valid destination address that can pass the address filter of the AN985B
- The payload of frame must include at least 6 contiguous 'FF' followed immediately by 16 repetitions of IEEE address.
- The frame can contain multiple 'six FF + sixteen IEEE address' pattern.
- CRC OK

■ THE WAKE ON LAN OPERATION

The Wake on LAN enable function is controlled by bit 18 of CSR18, it is loaded from EEPROM after reset or programmed by driver to enable Wake on LAN function. If the bit 18 of CSR18 is set and the AN985B receive a Magic Packet, it will assert the PME# signal (drive to low) to indicate receiving a wake up frame as well as to set the PME status bit (the bit 15 of CSR20).

■ ACPI POWER MANAGEMENT FUNCTION

The AN985B has a built-in capability for Power Management (PM) which controlled by the host system

The AN985B will provide:

- Compatibility with Device Class Power Management Reference Specification
- Network Device Class, Draft proposal v0.9, October 1996
- Compatibility with ACPI, Rev 1.0, December 22, 1996
- Compatibility with CARDBUS Bus Power Management Interface Specification, Rev 1.0, January 6, 1997
- Compatibility with AMD Magic Packet™ Technology.
- Compatibility with CARDBUS CLKRUN scheme.

■ POWER STATES

□ DO (Fully On)

In this state the AN985B operates as full functionality and consumes its normal power. While in the D0 state, if the CARDBUS clock is lower than 16MHz, the AN985B may not receive or transmit frames properly.

□ D1

In this state the AN985B doesn't response to any accesses except configuration space and full function context in place. The only network operation the AN985B can initiate is a wake-up event.

□ D2

In this state the AN985B only respond to access configuration space and full function context in place. The AN985B can't transmit or receive even the wake-up frame.

□ $D3_{cold}$ (Power Removed)

In this state all function context is lost. When power is restored, the function will return to D0.

□ $D3_{hot}$ (Software Visible D3)

When the AN985B is brought back to D0 from $D3_{hot}$ the software must perform a full initialization.

The AN985B in the $D3_{hot}$ state respond to configurations cycles as long as power and clock are supplied. This requires the device to perform an internal reset and return to a power-up reset condition without the RST# pin asserted.

Device State	CARDBUS Bus State	Function Context	Clock	Power	Supported Actions to Function	Supported Actions from Function
D0	B0	Full function context in place	Full speed	Full power	Any CARDBUS transaction	Any CARDBUS transaction or interrupt
D1	B0, B1	Configuration maintained. No Tx and Rx except wake-up	Stopped to Full speed		CARDBUS configuration access	Only wake-up events

		events				
D2	B0, B1, B2	Configuration maintained. No Tx and Rx	Stopped to Full speed		CARDBUS configuration access(B0, B1)	
D3hot	B0, B1, B2	Configuration lost, full initialization required upon return to D0	Stopped to Full speed		CARDBUS configuration access(B0, B1)	
D3cold	B3	All configuration lost. Power-on defaults in place on return to D0	No clock	No power	Power-on reset	

Table 1 Power state

ELECTRICAL SPECIFICATIONS AND TIMINGS

■ ABSOLUTE MAXIMUM RATINGS

Supply Voltage(Vcc)	-0.5V to 3.6V
Input Voltage	-0.5V to VCC+0.5 V
Output Voltage	-0.5V to VCC+0.5 V
Storage Temperature	-65°C to 150°C
Ambient Temperature	0°C to 70°C
ESD Protection	2000V

■ DC SPECIFICATIONS

General DC Specifications

Parameter	Description	Condition	Min	Typical	Max	Units
Vcc	Supply Voltage		3.0		3.6	V
Icc	Power Supply				1	A

CARDBUS Interface DC Specfications

Parameter	Description	Condition	Min	Typical	Max	Units
Vilp	Input LOW Voltage		-0.5		0.325vcc	V
Vihp	Input HIGH Voltage		0.475vcc		Vcc+0.5	V
Iilp	Input Leakage Current	0<Vin <Vcc			+-10	uA
Volp	Output LOW Voltage	Iout=700uA			0.1Vcc	V
Vohp	Output HIGH Voltage	Iout=-150uA	0.9Vcc			V
Cinp	Input Pin Capacitance		5		17	pF
Cclkp	CLK Pin Capacitance		10		22	pF

Flash/EEPROM Interface DC Specifications

Parameter	Description	Condition	Min	Typical	Max	Units
Vilf	Input LOW Voltage		0		Vcc x 0.3	V
Vihf	Input HIGH Voltage		Vcc x 0.7		Vcc + 1	V
Iif	Input Leakage Current				?	uA
Volf	Output LOW Voltage				0.2	V
Vohf	Output HIGH Voltage		Vcc – 0.2			V
Cinf	Input Pin Capacitance				?	pF

■ AC SPECIFICATIONS

CARDBUS Signaling AC Specifications for 3.3V

Parameter	Description	Condition	Min	Typical	Max	Units
Ioh(AC)	Switching Current High			4		mA
Iol(AC)	Switching Current Low			6		mA
	Slew Rate		0.25		1	V/ns

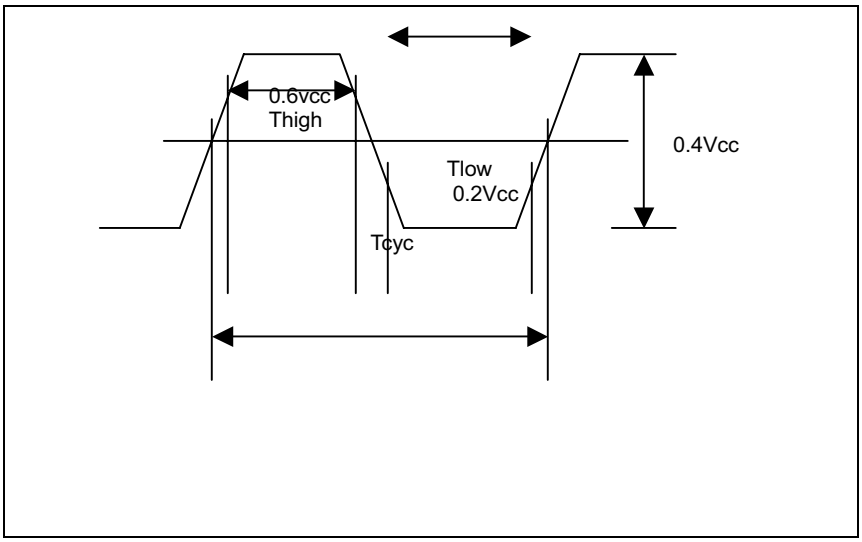
Icl	Low Clamp Current					mA
Tr	Unloaded Output Rise Time	0.2vcc~0.6vcc	1		4	V/ns
Tf	Unloaded Output Fall Time	0.6vcc~0.2vcc	1		4	V/ns

■ TIMING SPECIFICATIONS

CARDBUS Clock Specifications

Parameter	Description	Condition	Min	Typical	Max	Units
Tcyc	Clock Cycle Time		30			ns
Thigh	Clock High Time		12			ns
Tlow	Clock Low Time		12			ns
	Clock Slew Rate		1		4	V/ns

Figure 13 CARDBUS Clock Waveform

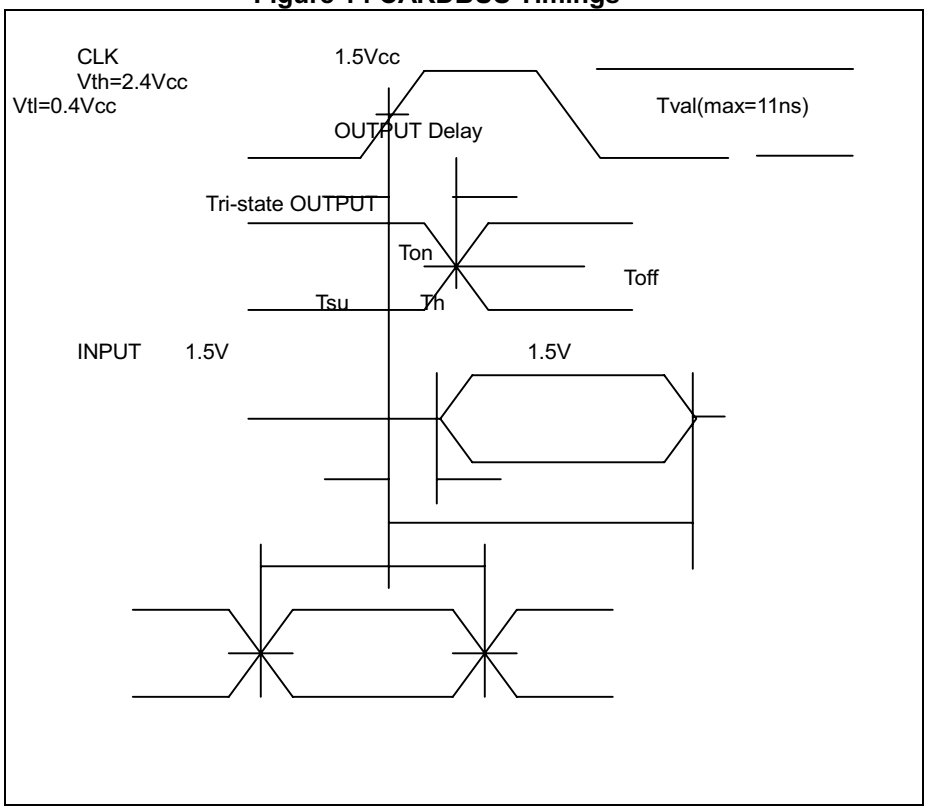


CARDBUS Timings

Parameter	Description	Condition	Min	Typical	Max	Units
Tval	access time – bused signals		2		11	ns
Tval(ptp)	access time –point to point		2		12	ns
Ton	Float to Active Delay		2			ns
Toff	Active to Float Delay				28	ns
Tsu	Input Set up Time to Clock – bused signals		7			ns
Tsu(ptp)	Input Set up Time to Clock - point to point		10,12			ns
Th	Input Hold Time from Clock		0			ns
Trst	Reset Active Time after Power Stable		1			ms
Trst-clk	Reset Active Time after CLK Stable		100			us
Trst-off	Reset Active to Output				40	ns

	Float delay					

Figure 14 CARDBUS Timings



Flash Interface Timings

Parameter	Description	Condition	Min	Typical	Max	Units
Trc	Read cycle time		90			ns
Tce	Chip enable access time				90	ns
Taa	Address access time				90	ns
Toe	Output enable access time				45	ns
Tclz	#CE low to active output		0			ns
Tolz	#OE low to active output		0			ns
Tchz	#CE high to active output				45	ns
Tohz	#OE high to active output				45	ns
Toh	Output hold from address change		0			ns
Twc	Write cycle time				10	ms
Tas	Address setup time		0			ns
Tah	Address hold time		50			ns
Tcs	#WE and #CE setup time		0			ns
Tch	#WE and #CE hold time		0			ns
Toes	#OE high setup time		10			ns
Toeh	#OE high hold time		10			ns
Tcp	#CE pulse width		70			ns
Twp	#WE pulse width		70			ns

Twph	#WE high width		150			ns
Tds	Data setup time		50			ns
Tdh	Data hold time		10			ns
Tblc	Byte load cycle time		0.22		200	us
Tblco	Byte laod cycle time out		300			us

Figure 15 Flash write timings

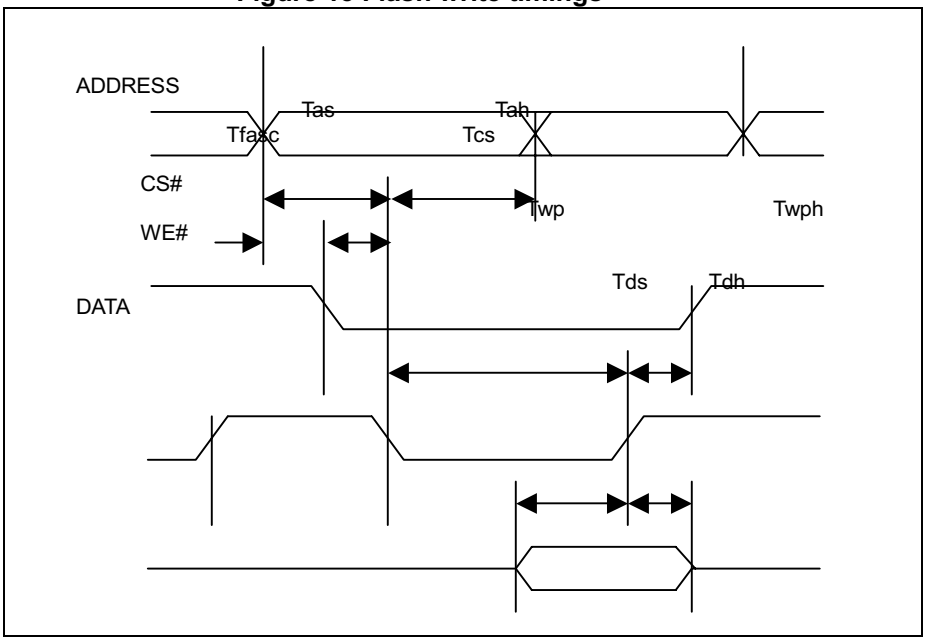
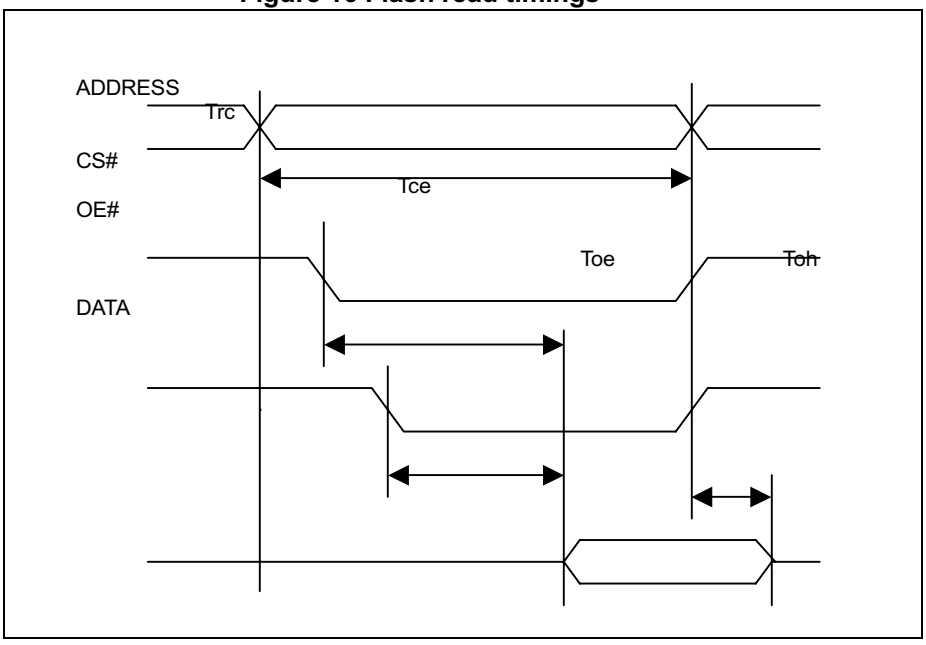


Figure 16 Flash read timings

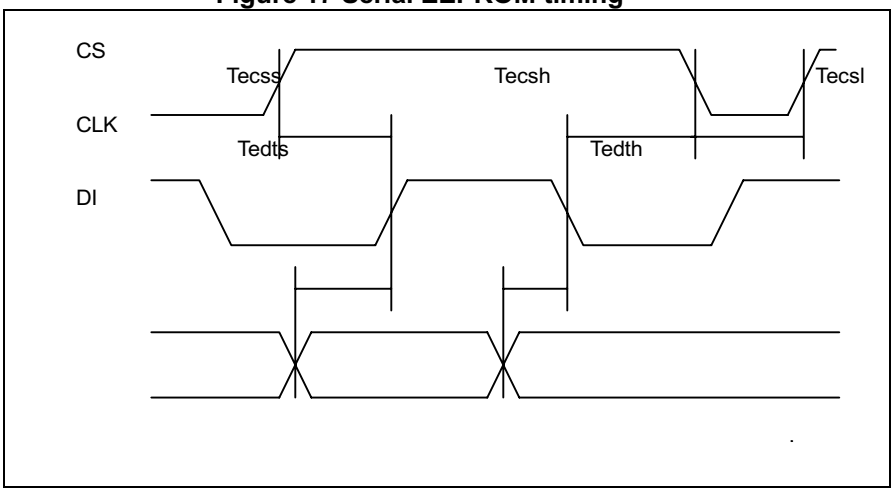


EEPROM Interface Timings (AC/AD)

Parameter	Description	Condition	Min	Typical	Max	Units
Tscf	Serial Clock Frequency	2.7V<Vcc<5.5			0.4M/	Hz

		V			0.1M	
Tecss	Delay from CS High to SK High	2.7V<Vcc<5.5 V	160/640			ns
Tecsh	Delay from SK Low to CS Low	2.7V<Vcc<5.5 V	1120 /4480			ns
Tedts	Setup Time of DI to SK	2.7V<Vcc<5.5 V	160/640			ns
Tedth	Hold Time of DI after SK	2.7V<Vcc<5.5 V	2320 /9280			ns
Tecsl	CS Low Time	2.7V<Vcc<5.5 V	7400/ 29600			ns

Figure 17 Serial EEPROM timing



APPENDIX

■ MII MANAGEMENT ACCESS PROCEDURE:

■ READ MANAGEMENT DATA FROM PHYTER:

1. Write CSR9[18] = 1 to let Mdio become input mode
2. Write CSR9[16] according to the IEEE802.3u spec to generate the MII management clock
3. Read CSR9[19] with reference the MII management clock

■ WRITE MANAGEMENT DATA FROM PHYTER:

1. Write CSR9[18] = 0 to let Mdio become output mode
2. Write CSR9[16] according to the IEEE802.3u spec to generate the MII management clock
3. Write CSR9[17] with reference the MII management clock

■ DEBUGGING PURPOSE REGISTERS : OFFSET FCH

■ MAC(HOME/PNA) MODE / SET FCH[2:0] = 100B

MDC : bra11
TXEN: bra10
TXD[3:0] : bra[9:6]
TXER: bra5
MDIO: bra3
RXDV: brd4
CRS: bra2
RXD[3:0] : brd[3:0]
COL: bra1
RXER: bra0
RXCLK: brwe_
TXCLK: broe_

■ PHY MONITOR MODE / SET FCH[2:0] = 110B

bra[16:0] = rxd[3:0] , crs, col, rx_clk, rx_dv, rx_er, tx_clk,
txd[3:0] , tx_er, tx_en, mdi,
brd[7:6] = mdo, mdc

■ PHY_ONLY MODE / SET FCH[2:0] = 001B

bra[16:9] = rxd[3:0], csr, col, rx_er, rx_dv,

brd[7:0] = mdc, mdio, tx_er, tx_en, txd[3:0],
broez = rx_clk
brwez = tx_clk

■ EEPROM DATA TABLE

Offset	b15 ---------- b8	b7 ---------- b0
08h	PHY ADDR 00	
0Ah	PHY ADDR 01	
0Ch	PHY ADDR 10	
16h	[b15~b4]=csr_MISC_control (offset f8h[15:4]) [b3~b0] = CSR15[31:28]	
20h	Device ID	
22h	Vendor ID	
24h	Subsystem ID	
26h	Subsystem vendor ID	
28h	MaxLat	MinGnt
2Ah	LAN CISL	
2Ch	LAN CISH	
2Eh	CSR18_REG	
30h~ 3Fh		
40h	PWRDATA1HB (LAN D0)	PWRDATA1LB(LAN D321)
42h~ 51h		
52h	CARDBUS CIS word count(<128)	
54h~ 7fh		
80h~ 13Fh		
140h~ 1FFh	CARDBUS CIS DATA(192 Words)	

■ PACKAGE

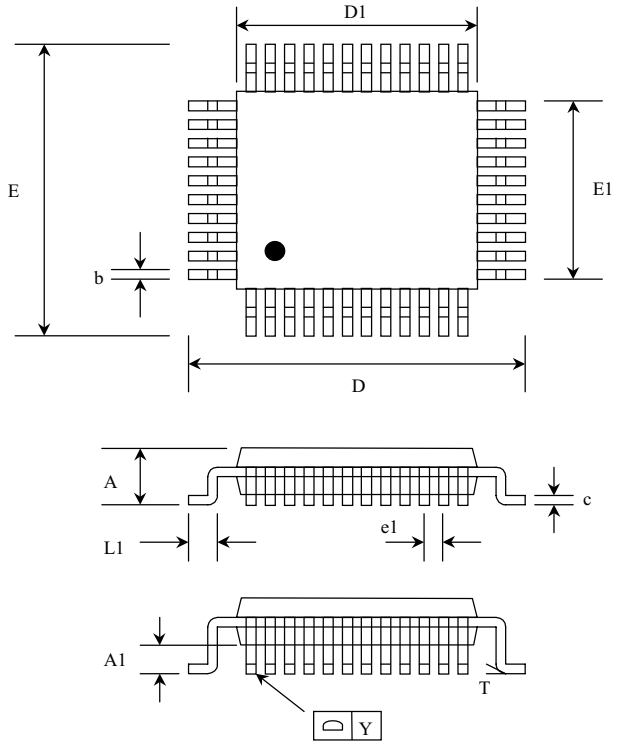


Fig - Package outline for the AN985B

Dimensions for 128 –pin LQFP Package

Symbol	Description	Minimum	Maximum
A	Overall Height	-	1.6mm
A1	Stand Off	0.05mm	0.15mm
b	Lead Width	0.17mm	0.27mm
c	Lead Thickness	0.13mm	0.23mm
D	Terminal Dimension 1	21.9.0mm	22.1mm
D1	Package Body 1	19.9mm	20.1mm
E	Terminal Dimension 2	15.9.0mm	16.1mm
E1	Package Body 2	13.9mm	14.1mm
e1	Lead Pitch	0.50mm	-
L1	Foot Length	0.45mm	0.75mm
T	Lead Angle	0	7

Y	Coplanarity		0.076mm