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Preliminary Data Sheet

BCM4319

Single-Chip IEEE 802.11™ a/b/g/n MAC/Baseband/ Radio with Integrated SDIO and USB Interfaces

GENERAL DESCRIPTION

The Broadcom BCM4319 single-chip device provides the highest level of integration for Wi-Fi enabled SDIO and USB-based wireless systems. Featuring an IEEE 802.11™ a/b/g/n MAC/baseband/radio with integrated CMOS, Power Amplifiers (PAs) and a power management unit (PMU) the BCM4319 provides a compact, ultrasmall form factor solution with few required external components. This enables high-volume costs to be driven down and allows flexibility in the size, form, and function of handheld devices.

The BCM4319 supports SDIO (4-bit, 1-bit, and Serial Peripheral Interface (SPI) modes), generic SPI (gSPI), USB 2.0 (device), and local Bluetooth® coexistence host interfaces.

Using advanced design techniques and process technology to deliver the lowest active and idle power, the BCM4319 extends system battery life in mobile systems, while maintaining consistent connectivity and high performance.

Integrated CMOS WLAN 2.4 GHz and 5 GHz power amplifiers provide sufficient output power to meet the needs of most WLAN devices. An optional external PA and Low-Noise Amplifier (LNA) are also supported.

GENERAL DESCRIPTION

In addition, the BCM4319 includes integrated transmit and receive baluns for both the 2.4 GHz and 5 GHz RF paths, further reducing the overall solution cost.

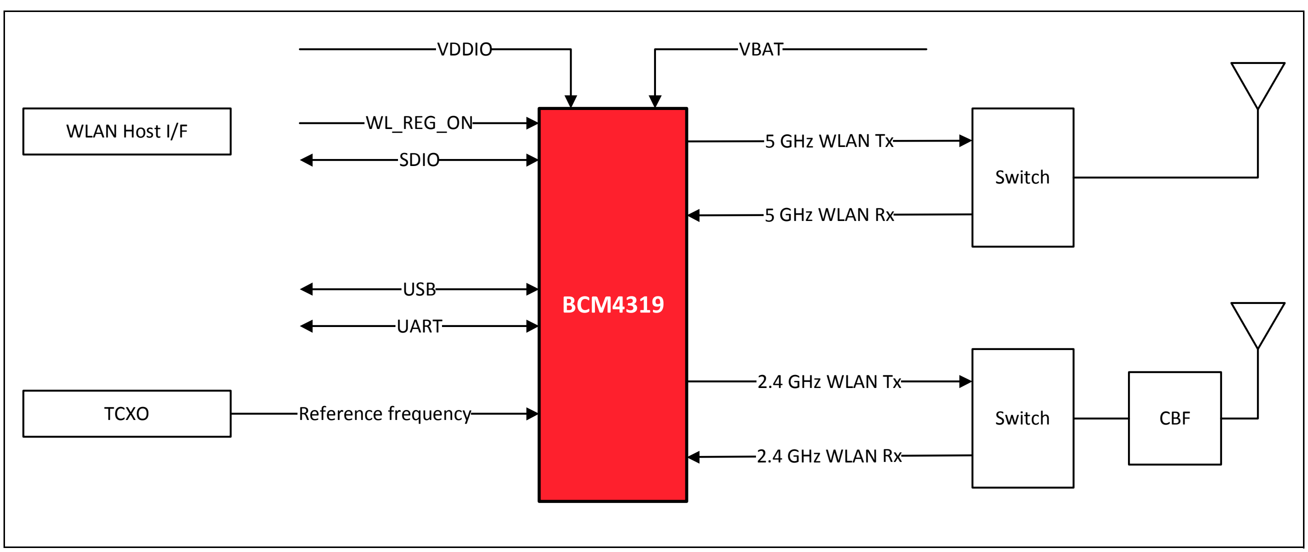
To simplify the system power topology and to enable operation directly from the battery of a mobile platform, the BCM4319 includes one switching regulator (buck mode), five linear low dropout (LDO) voltage regulators, and an advanced PMU. A variable input voltage range of 2.7V–5.5V is supported.

The integrated buck regulator enables the internal power amplifiers to operate at optimal performance, even at low VBAT supply voltages.

APPLICATIONS

- USB 2.0 dongles
- Printers
- Media players
- Cellular and mobile phones
- Gaming systems
- Cameras
- All types of battery powered devices
- Integrated designs with Bluetooth and GPS

Figure 1: BCM4319 System Block Diagram



4319-DS05-R

FEATURES

IEEE 802.11x Key Features

- Dual band 2.4 GHz and 5 GHz 802.11 a/b/g/n.
- Single stream 802.11n support for both 20 MHz and 40 MHz channels provides PHY layer rates up to MCS7 (150 Mbps) for typical upper layer throughput in excess of 70 Mbps.
- Integrated CMOS power amplifiers deliver greater than 20 dBm of linear output power
- Integrated ARM® Cortex-M3 processor and on-chip memory for complete WLAN subsystem functionality minimizing the need to wake up the applications processor for standard WLAN functions. This allows for further minimization of power consumption, while maintaining the capability to field upgrade with future features.
- Provides for the following security features:
  - WPA™ and WPA2™ (Personal) support for powerful encryption and authentication
  - AES and TKIP acceleration hardware for faster data encryption and 802.11i compatibility
  - Cisco® Compatible Extension (CCX, CCX 2.0, CCX 3.0, CCX 4.0) certified
  - SecureEasySetup™ for simple Wi-Fi® setup and WPA2/WPA security configuration
- Provides IEEE 802.11d, e (WMM, QoS, WMM-PS), h, i, j (k, r, and w in the future).
- Supports IEEE 802.15.2 external 3-wire and 4-wire coexistence schemes to support additional co-located wireless technologies such as Bluetooth® GPS, WiMax or UWB.
- Provides an ultra-small form factor solution and ultralow power consumption to support low-cost requirements.
- Wi-Fi Protected Setup (WPS).
- Internal fractional nPLL allows support for a wide range of reference clock frequencies.
- Worldwide regulatory support: Global products supported with worldwide homologated design.

USB 2.0 Key Features

- Support for high speed 480 Mbit/s or full speed 12 Mbit/s operation
- Endpoint management unit
- USB 2.0 protocol engine
- Separate endpoint packet buffers with a 512-byte FIFO buffer in each direction
- Host-to-device communication for bulk, control, and interrupt transfers

SDIO Key Features

- Supports standard SDIO V2.0 (4-bit and 1-bit), and SPI mode
- SDIO clock rates up to 50 MHz

Broadcom Corporation
5300 California Avenue
Irvine, CA 92617

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FEATURES

General Features

- Operation with an input voltage ranging from 2.7V to 5.5V using the internal buck switching regulator
- Five linear LDO regulators
- On-chip PMU
- Programmable dynamic power management
- UART for system debug
- 8 General Purpose I/O (GPIO) pins
- 138-ball, wafer-level WLBGA package (5.74 mm x 4.53 mm x 0.5 mm, 0.4 mm pitch. Dimensions are nominal, see Figure 18 on page 61 for maximum dimensions)

Revision History

Revision	*Date*	*Description*
4319-DS05-R	4/2/2014	**Updated:** • Table 32: "Ordering Information," on page 82
4319-DS04-R	12/12/11	**Updated:** • Table 32 on page 88 • Converted to latest format template
4319-DS03-R	11/10/09	**Updated:** • VBAT range, global update from 2.3V–5.5V to 2.7V–5.5V • "General Description" on Page • Figure 1, "BCM4319 System Block Diagram," on page i • "Mobile Phone Usage Model" on page 2 • Figure 3, "Mobile Phone System Diagram," on page 2 • "Power Management" on page 3 • "Voltage Regulators" on page 3 • "Power Supply Topology" on page 4 • Figure 4, "Power Topology Example," on page 5 • "Low-Power Shutdown" on page 6 • Table 1, "Crystal Oscillator and External Frequency Reference Specifications," on page 7 • "Frequency Selection" on page 9 • "General-Purpose Input/Output Interface" on page 10 • "SDIO V2.0" on page 13 • Figure 8, "Host Interface," on page 14 • Figure 14, "WLAN MAC Architecture," on page 22 • Table 4, "5.79 mm x 4.58 mm 138-Ball WLBGA," on page 29 • Table 6, "138-Ball WLBGA Signal Descriptions," on page 34 • "Strapping Options and GPIO Functions" on page 41 • Table 8, "Strapping Options," on page 42 • Table 9, "Environmental Characteristics," on page 43 • Table 10, "Absolute Maximum Ratings," on page 43 • Table 11, "Recommended Operating Conditions and DC Characteristics," on page 44 • Table 12, "Current Consumption," on page 45 • Cellular Blocking (deleted) • Section 11, WLAN RF Specifications, "Introduction" on page 46 • Table 13, "2.4 GHz Band General RF Specifications," on page 46 • Figure 20, "RF Port Location," on page 46 • Table 14, "2.4 GHz Band Receiver RF Specifications," on page 47 • Table 15, "2.4 GHz Band Transmitter RF Specifications," on page 49 • Table 16, "2.4 GHz Band Local Oscillator Specifications," on page 51 • Table 18, "5 GHz Receiver Sensitivity," on page 52

Revision	*Date*	*Description*

		• Table 21, "Core Buck Regulator (CBUCK)," on page 54
		• Table 22, "Internal PALDO," on page 55
		• Table 23, "2.5V LDO (LDO2p5V)," on page 55
		• Table 24, "CLDO," on page 56
		• Table 25, "LNLDO1, LNLDO2," on page 57
		• Section 13 "Power-Up Sequence" on page 58
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		• MAC Features:
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4319-DS02-R	7/24/09	**Updated:** • "SDIO Key Features" on page ii • Table 1, "Crystal Oscillator and External Frequency Reference Specifications," on page 7 • Table 4, "138-Ball WLBGA Signal Descriptions," on page 28 • Table 6, "Strapping Options," on page 36 • Table 8, "Environmental Characteristics," on page 37 • Table 10, "Recommended Operating Conditions and DC Characteristics," on page 38 • Table 13, "2.4 GHz Band General RF Specifications," on page 42 • Table 15, "2.4 GHz Receiver Sensitivity," on page 44 • Table 16, "2.4 GHz Band Transmitter RF Specifications," on page 45 • "SDIO High Speed Mode Timing" on page 59 • Figure 18, "138-Ball WLBGA Mechanical Information," on page 62 • Table 32, "Ordering Information," on page 63

Revision	*Date*	*Description*
4319-DS01-R	2/6/09	**Updated:** • Document type header • General Description on page i • Features on page ii • Figure 2, ”BCM4319 Block Diagram,” on page 1 • “Voltage Regulators” on page 3 • Figure 4, ”Power Topology Example,” on page 4 • “Power Supply Topology” on page 4 • “Crystal Interface and Clock Generation” on page 6 • Table 1, ”Crystal Oscillator and External Frequency Reference Specifications,” on page 6 • Figure 5, ”Recommended Oscillator Configuration,” on page 7 • “One-Time-Programmable (OTP) Memory” on page 9 • Section 4 ”Global Functions” on page 9 (changed section title, was “System Interfaces”) • “USB 2.0 Device Core” on page 10 • “SDIO V1.2” on page 11 • Section 5 ”USB 2.0 and SDIO Interfaces” on page 10 (changed section title; was “USB 2.0 evice Core” • “SDIO V1.2” on page 11 (moved from Section 4 ”Global Functions” to Section 5 ”USB 2.0 and SDIO Interfaces”) • Section 6 ”802.11 a/b/g/n MAC and PHY” on page 12 (title modified) • “PHY Features” on page 16 • “138-Ball WLBGA Pinout” on page 21 • Table 2, ”5.79 mm x 4.58 mm 138-Ball WLBGA,” on page 20 • Table 3, ”WLBGA Signal Assignments by Pin Number and X- and Y-Coordinates,” on page 21 • Table 4, ”138-Ball WLBGA Signal Descriptions,” on page 25 • Section 10 ”Operating Conditions” on page 33 (changed section title; was “DC Characteristics”) • “Environmental Ratings” on page 33 (was Environmantal Conditions; moved from Section 16 ”Package Information” on page 51) • Table 7, ”Environmental Characteristics,” on page 33

Revision	*Date*	*Description*
		• Table 8, ”Absolute Maximum Ratings,” on page 33 • Table 9, ”Recommended Operating Conditions and DC Characteristics,” on page 34 • Table 11, ”Blocking Signals from Embedded Cellular Transmitter at Cellular Antenna Port,” on page 36 • “Introduction” on page 36 • Table 13, ”2.4 GHz Band Receiver RF Specifications,” on page 38 • Table 14, ”2.4 GHz Receiver Sensitivity,” on page 38 • Table 17, ”5 GHz Band Receiver RF Specifications,” on page 40 • Table 21, ”Core Buck Regulator (CBUCK),” on page 42 • Table 22, ”Internal PALDO,” on page 43 • Table 23, ”2.5V LDO (LDO2p5V),” on page 43 • Table 24, ”CLDO,” on page 44 • Table 25, ”LNLDO1, LNLDO2,” on page 45 • Figure 14, ”Power-Up Sequence Timing Diagram,” on page 46 • Figure 15, ”SDIO Bus Timing (Default Mode),” on page 47 • Figure 16, ”SDIO Bus Timing (High-Speed Mode),” on page 49 • Figure 17, ”138-Ball WLBGA Mechanical Information,” on page 52
		Added: • WLBGA Package • “One-Time-Programmable (OTP) Memory” on page 9 • “Bluetooth Coexistence Interface” on page 9 • Table 6, ”Strapping Options and GPIO Functions,” on page 32 • “Junction Temperature Estimation and PSIJT VERSUS THETAJC” on page 51 • Table 18, ”Ordering Information,” on page 53
		Deleted: • FCBGA Package • “LPO Clock Interface” on page 9 • Table 21, ”PALDO with External PNP,” on page 43 • Table 25, ”Bandgap Reference Block (HVBG),” on page 44 • Table 27, ”LDO Bandgap Reference (LDOBG),” on page 45
4319-DS00-R	05/01/08	Initial release

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About This Document

Purpose and Audience

This data sheet provides details about the functional, operational, and electrical characteristics of the Broadcom BCM4319. It is intended for hardware design, application, and OEM engineers.

Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use.

For a comprehensive list of acronyms and other terms used in Broadcom documents, go to: http://www.broadcom.com/press/glossary.php.

Document Conventions

The following conventions may be used in this document:

Convention	*Description*
Bold	User input and actions: for example, type **exit**, click **OK,** press **Alt+C**
Monospace	Code: #include <iostream> HTML: <td rowspan = 3> Command line commands and parameters: wl [-l] <command>
< >	Placeholders for *required* elements: enter your <username> or wl <command>
[ ]	Indicates *optional* command-line parameters: wl [-l] Indicates bit and byte ranges (inclusive): [0:3] or [7:0]

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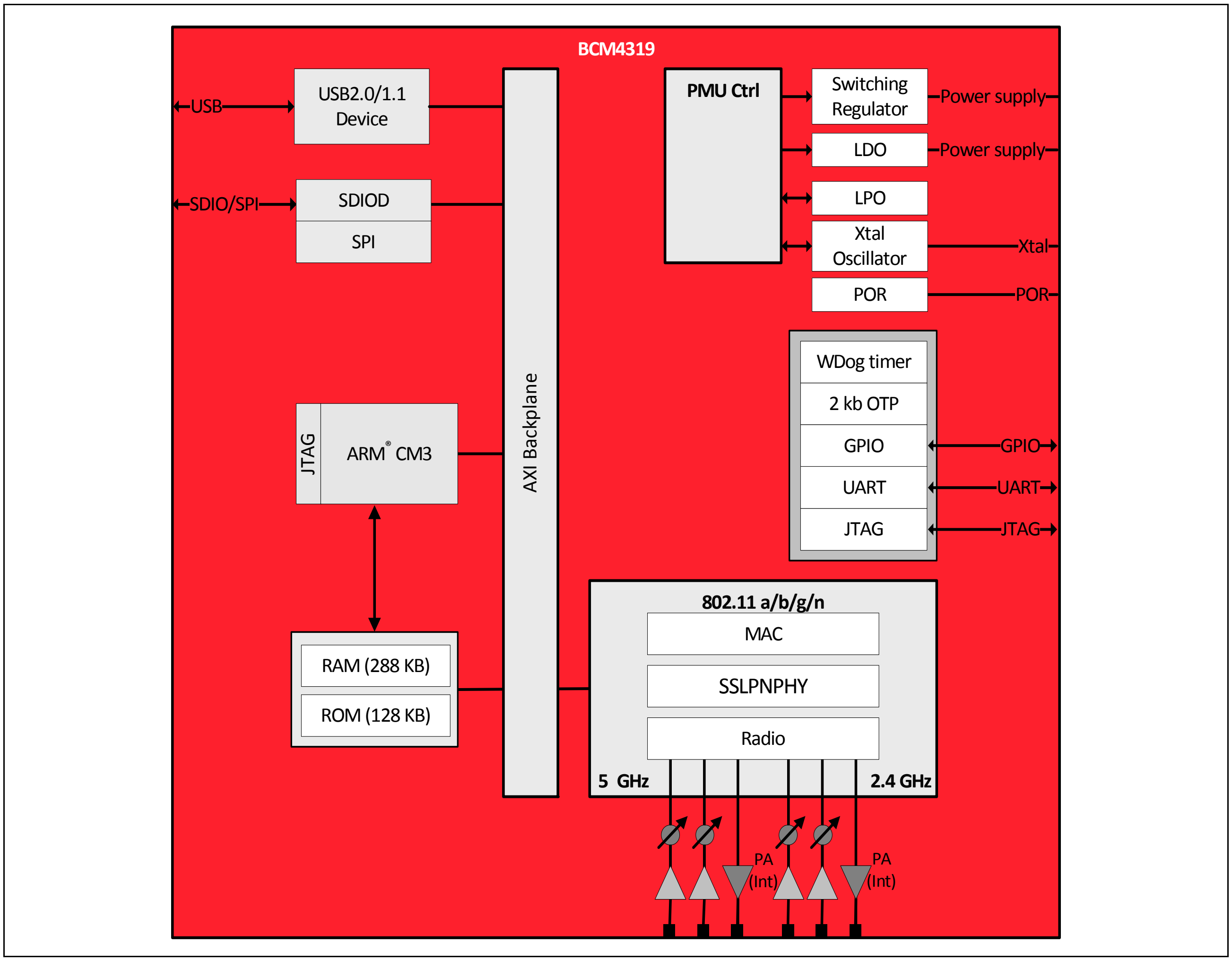
Section 1: Overview

Overview

The Broadcom BCM4319 family of single-chip devices provides the highest level of integration for a mobile or handheld wireless system, with integrated IEEE 802.11™ a/b/g/n (MAC/baseband/radio), power amplifiers (PAs), and power management unit (PMU). It provides a compact, small form factor solution with minimal external components to drive down the costs for mass volumes while enabling handheld device flexibility in size, form, and function. The BCM4319 is designed to address the needs of highly mobile devices that require minimal power consumption and reliable operation.

Figure 2 shows the major blocks and external interfaces of the BCM4319.

Figure 2: BCM4319 Block Diagram



Mobile Phone Usage Model

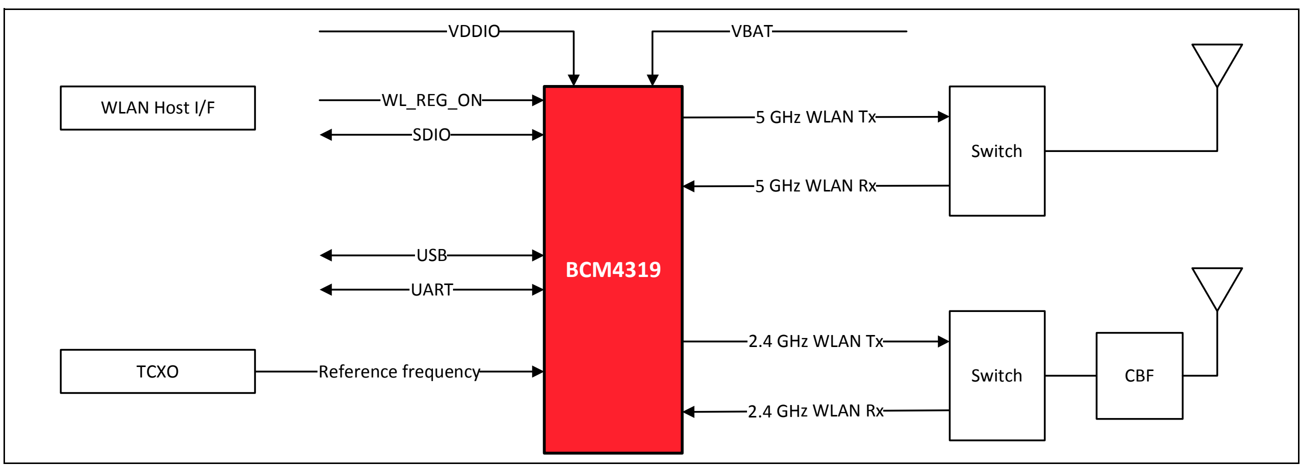
The BCM4319 has a flexible Universal Serial Bus (USB) and a secure digital input/output (SDIO) interface for cellular phone applications, enabling it to transparently connect to existing circuits. In addition, the temperature-compensated crystal oscillator (TCXO) input allows the use of existing clock sources within the system to further minimize the size, power, and cost of the complete system.

The BCM4319 incorporates the following unique features for easy integration into mobile phone platforms:

- The TCXO interface accommodates typical cell phone reference frequencies.
- The transceiver's highly linear design ensures the lowest spurious output regardless of operating state. It has been fully characterized in all global cellular bands.
- The transceiver design, with minimal required external filtering, has excellent blocking and intermodulation performance in the presence of the following cellular transmissions:
  - Global Standard for Mobile Communications (GSM)
  - General Packet Radio Service (GPRS)
  - Code Division Multiple Access (CDMA)
  - Wideband CDMA (WCDMA)
  - Integrated Digital Enhanced Network (IDEN).
- Minimal external components are required for integration; compact packaging is available.

The BCM4319 is designed to interface directly with new and existing handset designs as shown in Figure 3.

Figure 3: Mobile Phone System Diagram



Section 2: Power Supplies and Management

Power Management

The BCM4319 has been designed with the stringent power consumption requirements of mobile devices in mind. All areas of the chip design are optimized to minimize power consumption. Silicon processes and cell libraries were chosen to reduce leakage current and supply voltages. Additionally, the BCM4319 integrated RAM is a high Vt memory with dynamic clock control. Leakage current is the dominant supply current consumed by the RAM.

The BCM4319 includes an advanced wireless local area network (WLAN) PMU. The PMU provides significant power savings by putting the BCM4319 into various power management states appropriate to the current environment and activities that are being performed. The power management unit enables and disables internal regulators, switches, and other blocks based on a computation of the required resources and the relationship between resources and the time needed to enable and disable them. Power-up sequences are fully programmable. Configurable, free-running counters (running on an internal LPO clock) in the PMU are used to turn individual regulators and power switches on and off. Clock speeds are dynamically changed or gated for the current mode. Slower clock speeds are used wherever possible.

The BCM4319 power states are described as follows:

- Active mode—All BCM4319 cores are powered up and fully functional with active carrier sensing, frame transmission, and frame reception. All required regulators are enabled and put in the most efficient mode, either Pulse Width Modulation (PWM) or Burst, based on the load current. Clock speeds are dynamically adjusted by the PMU.
- Sleep mode—The radio, analog front end (AFE), Phase-Locked Loops (PLLs), and read-only memories (ROMs) are powered down. The rest of the BCM4319 remains powered up in an IDLE state. All main clocks are shut down. The internal 32 kHz clock is used by the PMU to wake the chip and transition to Active mode. In Sleep mode, the primary power consumed is due to leakage current. The internal baseband switcher is put into burst mode for better efficiency at low load currents.
- Power-down mode—The BCM4319 is effectively powered off by shutting down all internal regulators. The chip is brought out of this mode by external logic re-enabling the internal regulators.

Voltage Regulators

One Buck regulator, five LDO regulators, and a PMU are integrated into the BCM4319. All regulators are programmable via the PMU.

- Core Buck: 2.7–5.5V in; 1.4V, 300 mA out
- Low-noise LNLDO1: 1.4V in; 1.2V, 150 mA out
- Low-noise LNLDO2 (optional): 1.4V or 3.3V in; 1.2V or 2.5V, 50 mA out
- Low-noise CLDO: 1.4V in; 1.2V, 200 mA out

- PALDO: 2.7–5.5V in; 2.7–4.0V, 400 mA out
- LDO2p5V: 2.7 – 5.5V in; 2.5V, 50 mA out for USB2.0 Phy

Power Supply Topology

The BCM4319 contains power supply building blocks, including a switching regulator, four LDOs, and a power amplifier LDO (see Figure 4 on page 18). These blocks simplify power supply design for WLAN in embedded designs. All regulator inputs and outputs are brought out to pins on the BCM4319, thereby enabling maximum system design flexibility in choosing which of the integrated regulators to use.

A single host power supply, ranging from 2.7V to 5.5V, can be used with all additional voltages being provided by BCM4319 regulators. For additional information see Section 12: “Internal Regulator Electrical Specifications,” on page 68. Alternately, if specific rails such as 3.3V, 2.5V, and 1.2V already exist in the system, appropriate regulators in the BCM4319 can be disabled, thereby reducing the cost and board space associated with external regulator components such as inductors and large capacitors.

When WL_REG_ON is low (< 1.2 – 20% = 0.96V) or the voltage at VDDIO is less than 0.96V, all six regulators are powered down.

When WL_REG_ON is high (> 1.6V) and the voltage at VDDIO is greater than 1.6V, the CBUCK, LDO2p5V, CLDO, and LNLDO1 regulators are powered on by default. The digital logic remains in the reset state while EXT_POR_L is low or while the internal POR is asserted. The internal POR circuit generates a reset within 110 ms after VDDC and VDDIO stabilize. After the resets are deasserted, the BCM4319 powers up the PALDO, OTP, and clock circuitry.

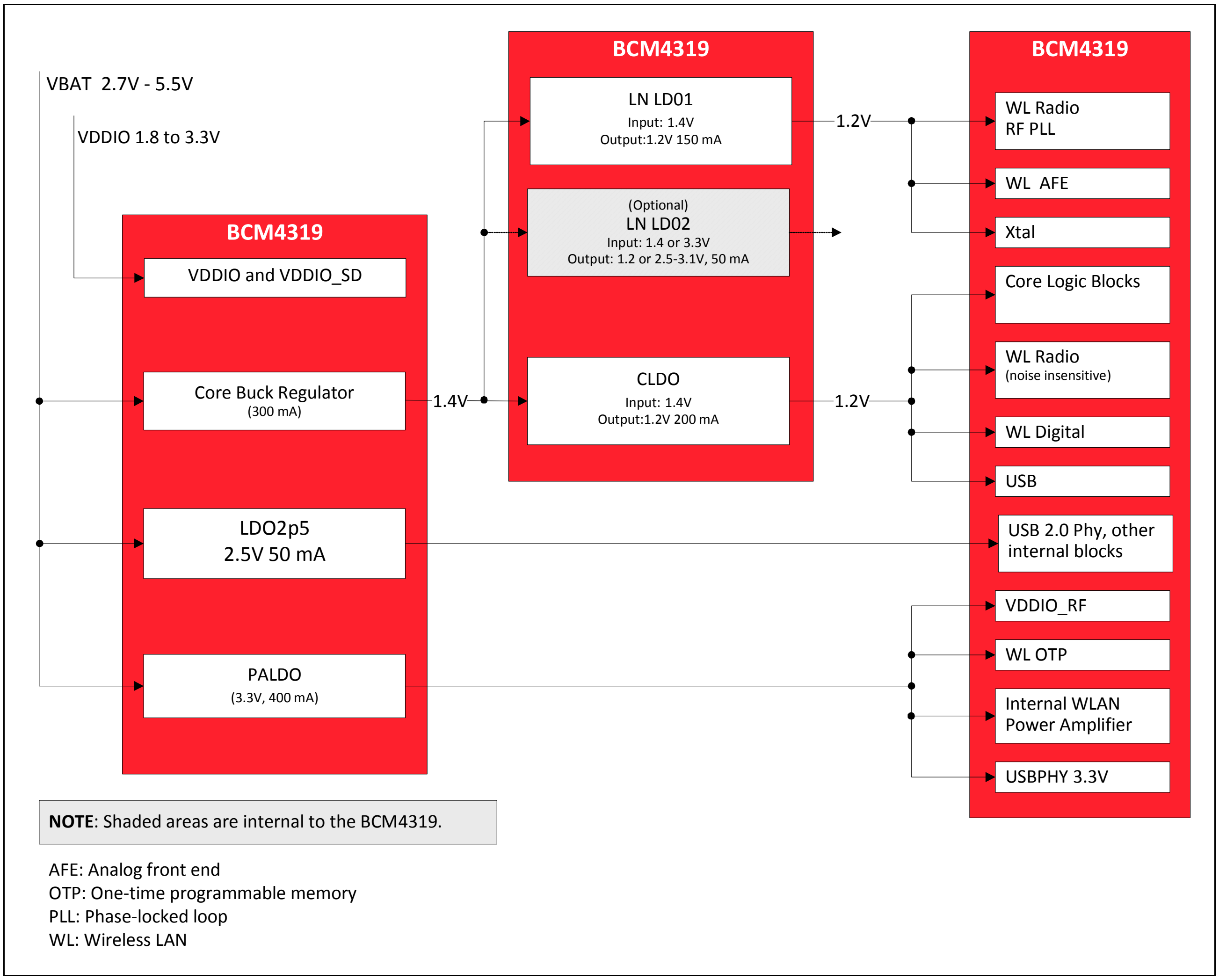
After the digital logic is active and the software is running, the state of all the regulators is controlled dynamically. To keep the digital logic powered up, CBUCK and CLDO cannot be powered down. They can, however, be put into low-power modes. The PALDO can be powered ON or OFF under software control to reduce power consumption, for example during sleep mode.

There is a 200 KΩ (±20%) internal pull-down on WL_REG_ON, which can be disabled after the digital logic is active.

- The voltage at WL_REG_ON should not exceed 3.6V.
- The IO supply for the EXT_POR_L pin is VDDIO.
- VBAT and VDDIO should be supplied externally: VDDIO cannot be supplied by the output of any of the six regulators.
- The POR delays are different for the three IO supplies:
  - VDDIO = 110 ms
  - VDDIO_SD = 8 us
  - VDDIO_RF = 3.4 ms

The trip point of the internal POR circuit is VDDC ~ 0.8V or VDDIO/VDDIO_SD/VDDIO_RF ~ 0.9V and the IOs remain in tristate during the respective POR.

Figure 4: Power Topology Example



PMU Sequencer

The PMU sequencer is responsible for minimizing system power consumption. It enables and disables various system resources based on a computation of the required resources and the relationship between resources and their enable and disable times.

In each device state, a minimum set of resources is always available, as defined in the PMU control registers. Additional resources can be enabled on request from various sources, including clock requests from cores and timers in any of the active resources. The PMU sequencer maps clock requests into a set of resources required to produce the requested clocks.

Each resource is in one of four states: enabled, disabled, transition_on, and transition_off. Each resource has a timer that contains 0 when the resource is enabled or disabled and a nonzero value in the transition states. The timer is loaded with the resource's time_on or time_off value when the PMU determines that the resource must be enabled or disabled, and it decrements on each 32.768 kHz PMU clock. When it reaches 0, the state changes from transition_off to disabled or transition_on to enabled. If the time_on value is 0, the resource can go immediately from disabled to enabled. Similarly, a time_off value of 0 indicates that the resource can go immediately from enabled to disabled. The terms enable sequence and disable sequence refer to either the immediate transition or the timer load-decrement sequence.

During each clock cycle, the PMU sequencer performs the following:

1. Computes the required resource set based on requests and the resource dependency table.
2. Decrements all timers whose values are nonzero. If a timer reaches 0, the PMU clears the ResourcePending bit for the resource and inverts the ResourceState bit.
3. Compares the request with the current resource status and determines which resources must be enabled or disabled.
4. Initiates a disable sequence for each resource that is enabled, no longer being requested, and has no powered-up dependents.
5. Initiates an enable sequence for each resource that is disabled, is being requested, and has all of its dependencies enabled.

Low-Power Shutdown

The BCM4319 provides a low-power shutdown feature that allows the device to be turned off while the host and other system devices remain operational. When the BCM4319 is not needed in the system, WL_REG_ON should be driven low while VDDIO remains powered. This allows the BCM4319 to be effectively off while keeping the I/O pins powered, so that they do not draw extra current from any other devices connected to the I/O.

During a low-power shutdown state, provided VDDIO remains applied to the BCM4319, all outputs are tristated, and most inputs signals are disabled. Input voltages must remain within the limits defined for normal operation. This is done to prevent current paths or to create loading on any digital signals in the system, and it enables the BCM4319 to be fully integrated in an embedded device and to take full advantage of the lowest power saving modes.

The frequency reference input (XTALIN) is designed to be a high-impedance input that does not load down the driving signal, even if the chip does not have VDDIO power applied to it.

When the BCM4319 is powered on from this state, it is the same as a normal power-up, and the device does not contain any information about its state from before it was powered down.

Section 3: Frequency References

The BCM4319 uses the following frequency references for normal and low-power operational modes:

- An external crystal or external frequency reference driven by a TCXO signal is used for generating all radio frequencies and normal operation clocking.
- An internal 32.768 kHz sleep clock is provided for use by the PMU during low power states.

Crystal Interface and Clock Generation

The BCM4319 uses a fractional-N synthesizer to generate the radio frequencies, clocks, and data/packet timing. This enables it to operate using numerous frequency references derived from an external source such as a TCXO or a crystal connected directly to the BCM4319. The default frequency reference is a 30 MHz, 10 ppm crystal or TCXO. The requirements and characteristics for the crystal circuit and external frequency reference are listed in Table 1.

Table 1: Crystal Oscillator and External Frequency Reference Specifications

		Crystal			External Frequency Reference			
Parameter	***Condition*** [a]	***Min***	***Typ***	***Max***	***Min***	***Typ***	***Max***	***Unit***
Frequency	–	–	30	–	12	30	52	MHz [b]
ESR	–	–	–	60	–	N/A	–	Ω
Input impedance	Resistive	–	N/A		1M	–	–	Ω
	Capacitive	–	N/A			–	4.7	pF
Power dissipation	Programmable Depends on external reference input amplitude	0.2	–	1	0.2	–	1	mW
Input voltage	AC-coupled analog signal	–	N/A		400 [c]	–	1200	mV_{p-p}
Output low level	DC-coupled digital signal	–	N/A		0	–		V
Output high level	DC-coupled digital signal	–	N/A		1.0	–	1.36	V
Frequency tolerance [d]	Without trimming	–20	±10	20	–20	±10	20	ppm
Initial frequency tolerance trimming range	–	–50	–	50	–50	–	50	ppm
Duty cycle	For 30 MHz clock	–	N/A	–	40	50	60	%

Table 1: Crystal Oscillator and External Frequency Reference Specifications (Cont.)

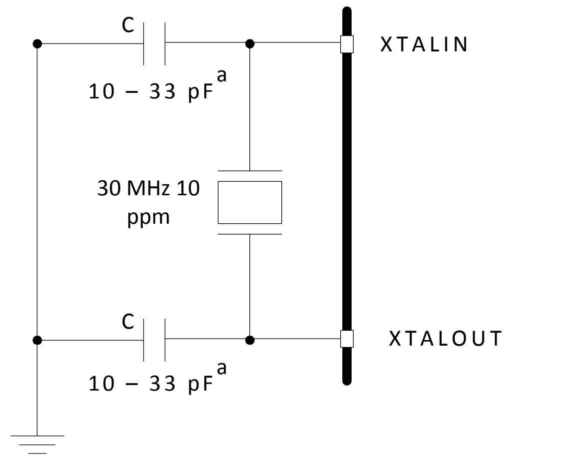
		Crystal			External Frequency Reference			
Parameter	***Condition*** [a]	***Min***	***Typ***	***Max***	***Min***	***Typ***	***Max***	***Unit***
Phase noise requirements [e f]	For 30 MHz clock	–	N/A	–	–	–130[g]	–	dBc/Hz
	For 30 MHz clock	–	N/A	–	–	–140[f]	–	dBc/Hz
	For 30 MHz clock	–	N/A	–	–	–145[f]	–	dBc/Hz
	For 30 MHz clock	–	N/A	–	–	–150[f]	–	dBc/Hz
Jitter	From1 kHz to 1 MHz	–	N/A	–	–	–	< 0.33	ps

a. The supported crystal/external reference frequencies for SDIO mode are 12 MHz to 52 MHz (26 or 30 MHz is recommended). For USB mode, only 30 MHz is supported.
b. Frequency programmable between 12 MHz and 52 MHz, in 2 ppm steps. The step size (resolution) is approximately 80 Hz.
c. Exact value of load capacitance to center the frequency tolerance depends on board layout; see Broadcom reference schematics.
d. Initial + over temperature + aging.
e. If the input signal amplitude is below 800 mV p-p, contact your Broadcom representative for applications assistance.
f. For a clock reference other than 30 MHz, these limits must be scaled by 20*log10(f / 30) dB, where f = the reference clock frequency in MHz.
g. For 5 GHz, 11n (both the 20 and 40 MHz channels): covers all other modes of operation.

Crystal Oscillator

The BCM4319 can use an external crystal to provide a frequency reference. The recommended configuration for the crystal oscillator including all external components is shown in Table 5 on page 22. Refer to the reference board schematics for exact details.

Figure 5: Recommended Oscillator Configuration

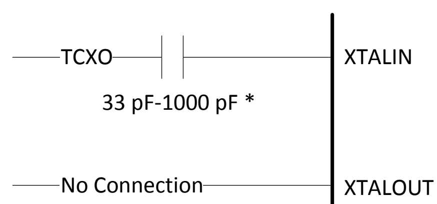


a. The precise value of load capacitance to center the frequency tolerance is dependent on board layout; see Broadcom reference schematics for exact values.

External Frequency Reference

An external frequency reference generated by a TCXO may be directly connected to the XTALIN pin on the BCM4319 as shown in Figure 6. The external frequency reference input is designed to not change the loading on the TCXO when the BCM4319 is powered up or powered down.

Figure 6: Recommended TCXO Connection



* Recommended value is 100 pF.
Higher values produce a longer start-up time.

Frequency Selection

For SDIO mode, any frequency within the ranges specified for the crystal and TCXO reference may be used. These include the standard handset reference frequencies of 12, 13, 14.4, 16.2, 16.8, 18, 19.2, 19.44, 19.68, 19.8, 20, 24, 26, 30, 38.4, and 52 MHz, plus any other frequency in this range. The BCM4319 must have the reference frequency set correctly in order for any of the UART interfaces to function properly, since all bit timing is derived from the reference frequency.

The BCM4319 is set at the factory to a default frequency of 30 MHz. For a typical design using a crystal, it is recommended that the default frequency be used: for USB Mode, 30 MHz is *required*.

Frequency Trimming

The BCM4319 uses a fractional-N synthesizer to digitally fine tune the frequency reference input to within ±2 ppm tuning accuracy. This trimming function can be applied to the crystal or an external frequency source such as a TCXO. Unlike typical crystal trimming methods, the BCM4319 uses a fully digital implementation to change the frequency, which is much more stable and tolerant of the crystal characteristics and temperature. The input impedance and loading characteristics remain unchanged on either the TCXO or the crystal during the trimming process and are unaffected by process and temperature variations.

Section 4: Global Functions

General-Purpose Input/Output Interface

There are eight General-Purpose I/O (GPIO) pins on the BCM4319, which can be used to control various external devices. Upon power-up and reset, these pins become tri-stated. Subsequently, they can be programmed to be either input or output pins via the GPIO control register. If a GPIO output enable is not asserted and the corresponding GPIO signal is not being driven externally, then the GPIO is read as high.

Each GPIO has a programmable option to enable/disable internal pull-up or pull-down (60 KΩ) resistors. The default setting depends on the strapping options: if a strapping option is assigned to a GPIO pin then the default pull is according to the default strapping value. Otherwise, there is no default pull on the GPIO.

GPIOs that do not have interfering strapping options can be safely used as *input* pins. All GPIOs can be safely used in *output* mode.

Internal pull-up and pull-down resistors are active only when VDDC and VDDIO are present.

After the driver is loaded, the software disables the pull to reduce leakage.

UART Interface

One UART interface is provided, which enables the BCM4319 to operate as RS-232 data termination equipment (DTE) for exchanging and managing data with other serial devices. The UART interface is primarily used for debugging during development. It is compatible with the industry standard 16550 UART, and it provides a FIFO size of 64 × 8 in each direction.

One-Time-Programmable (OTP) Memory

Various hardware configuration parameters may be stored in an internal 2k-bit OTP memory, which is read by system software after device reset. In addition, customer-specific parameters, including the system vendor ID and the MAC address, can be stored, depending on the specific board design. A programming utility is provided with the Broadcom manufacturing test tools.

As an alternative to using the internal OTP, an external 4-wire SPROM interface can be enabled.

Bluetooth Coexistence Interface

A 4-wire handshake interface is provided to enable signaling between the device and an external colocated wireless device, such as Bluetooth GPS, WiMax or UWB, to manage wireless medium sharing for optimum performance. The IEEE 802.15.2 coexistence schemes can be supported.

The following signals are provided:

- BTCX_STATUS
- BTCX_RF_ACTIVE
- BTCX_FREQ
- BTCX_TXCONF

JTAG Interface

The BCM4319 supports the IEEE 1149.1 JTAG boundary scan standard for testing the device packaging and PCB during manufacturing. It is also an essential interface for Broadcom to run characterization tests and it is highly recommended to provide access to these pins on all pcb designs.

Section 5: USB 2.0 and SDIO Interfaces

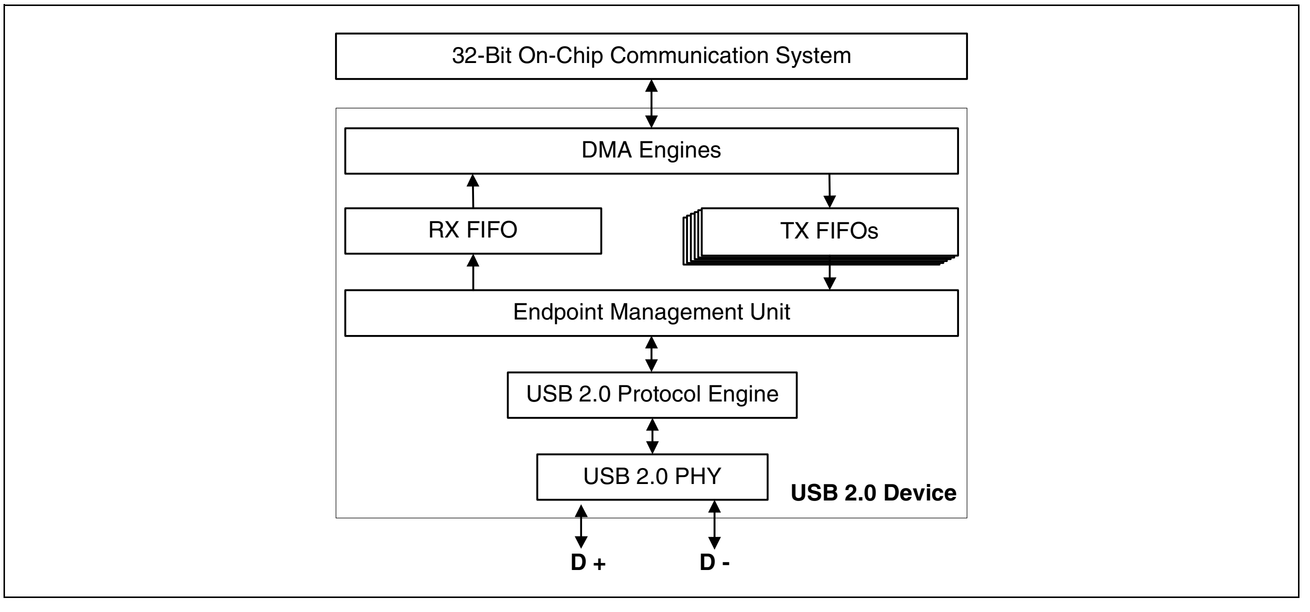
USB 2.0 Device Core

The USB 2.0 device core is enabled by a strapping option, see Table 8 on page 56 for details. It includes the following features: includes the following features:

- Support for high speed at 480 Mbit/s or full speed at 12 Mbit/s operation
  - USB 2.0 transceiver interface
  - Data and clock recovery circuit
  - Bit stuffing and unstuffing; bit stuff error detection
  - SYNC/EOP generation and checking
  - Error detection and handling
  - Wake up, resume, and suspend detection
- Endpoint management unit–Manages USB traffic and DMA engine
- USB 2.0 protocol engine
  - Parallel interface engine (PIE) between packet buffers and USB transceiver
  - Supports up to nine endpoints, including Configurable Control Endpoint 0
- Separate endpoint packet buffers, each with a 512-byte first-in first-out (FIFO) buffer
- Host-to-device communication for bulk, control, and interrupt transfers
- Configuration/status registers

The blocks in the USB 2.0 device core are shown in Figure 7.

Figure 7: USB 2.0 Device Block Diagram



The USB 2.0 PHY handles the USB protocol and the serial signaling interface between the host and the device. It is primarily responsible for data transmission and recovery. On the transmit side, data and a clock are encoded using the NRZI scheme with bit stuffing to ensure that the receiver detects a transition in the data stream. A SYNC field that precedes each packet enables the receiver to synchronize the data and clock recovery circuits. On the receive side, the serial data is deserialized, unstuffed, and checked for errors. The recovered data and clock are then shifted to the clock domain that is compatible with the internal bus logic.

The endpoint management unit contains the PIE control logic and the endpoint logic. The PIE interfaces the packet buffers to the USB transceiver. It handles packet identification (PID), USB packets, and transactions. The endpoint logic contains nine uniquely addressable endpoints. These endpoints are the source or sink of communication flow between the host and the device. Endpoint zero is used as a default control port for both the input and output directions. The USB system software uses this default control method to initialize and configure the device information and allows USB status and control access. Endpoint zero is always accessible after a device is attached, powered, and reset.

Endpoints are supported by 512-byte FIFO buffers, one for each IN endpoint and one shared by all OUT endpoints. Both TX and RX data transfers support a DMA burst of 4, which guarantees low latency and maximum throughput performance. The RX FIFO can never overflow by design. The maximum USB packet size cannot be more than 512 bytes.

SDIO V2.0

The SDIO Interface is enabled by a strapping option, see Table 8 on page 56 for details.

The BCM4319 supports all of the SDIO version 2.0 modes:

- 1-bit SDIO-SPI mode (25 Mbps)
- 1-bit SDIO-SD mode (25 Mbps)
- 4-bit SDIO-SD Default Speed mode (100 Mbps)
- 4-bit SDIO-SD High Speed mode (200 Mbps)

The SDIO interface supports the full clock range, from 0 to 50 MHz.

The chip has the ability to stop the SDIO clock between transactions to reduce power consumption. As an option, GPIO_0 pin may be mapped to provide an SDIO Interrupt signal. This out-of-band interrupt is hardware generated and is always valid (unlike the SDIO in-band interrupt, which is signalled only when data is not driven on SDIO lines).The ability to force control of the gated clocks from within the WLAN chip is also provided.

Three functions are supported:

- Function 0 — Standard SDIO function. Maximum BlockSize/ByteCount = 32 bytes.
- Function 1 — Backplane function to access the internal System-on-a-Chip (SoC) address space. Maximum BlockSize/ByteCount = 64 bytes.
- Function 2 — WLAN function for efficient WLAN packet transfer through direct memory access (DMA). Maximum BlockSize/ByteCount = 512 bytes.

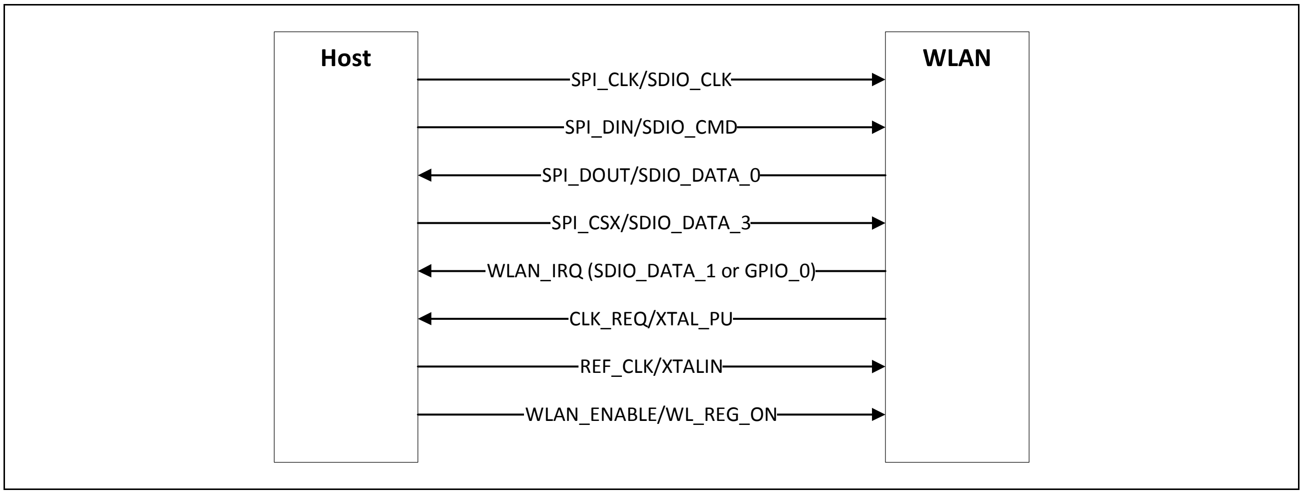
Detailed SDIO pin description and signal connection block diagrams are shown in Section 9: “Pinout and Signal Descriptions,” on page 45. In addition, the generic SPI (gSPI) mode, with clock ranges from 0 to 48 MHz, is supported.

gSPI

The BCM4319 also includes the generic SPI (gSPI) interface/protocol functionality. Characteristics of the BCM4319 interface includes support for:

- Up to 48 MHz operation
- Fixed delays for responses and data from device
- Alignment to host SPI frames (16- or 32-bits)
- Up to 2 KB frame size per transfer
- Little endian and big endian configurations
- Configurable active edge for shifting
- Packet transfer through DMA for WLAN

Figure 8: Host Interface



SPI Protocol

The SPI protocol supports both 16-bit and 32-bit word operation. Byte endianess is supported in both modes. Figure 9 and Figure 10 show the basic write and write-read commands.

Figure 9: SPI Write Protocol

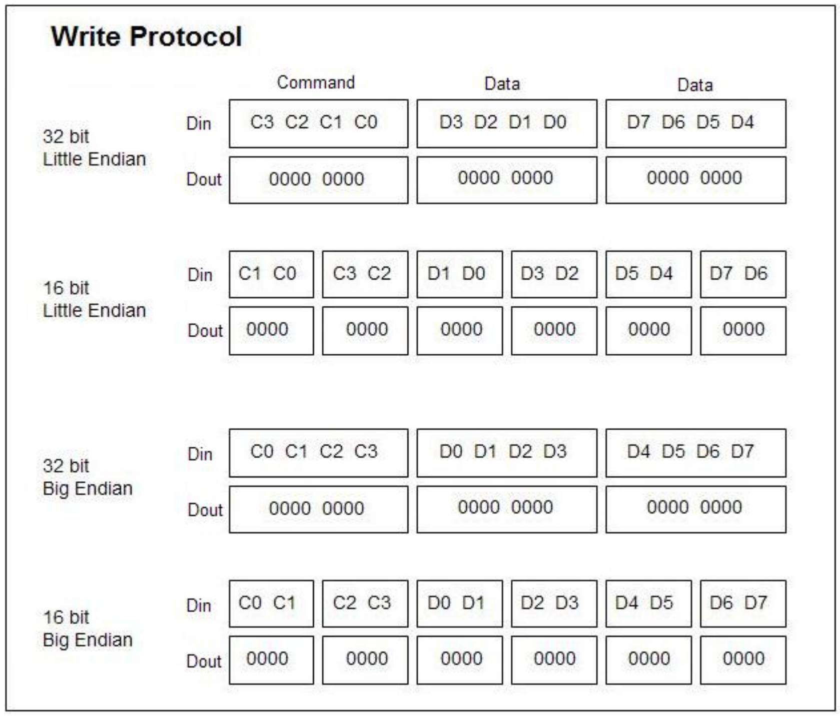
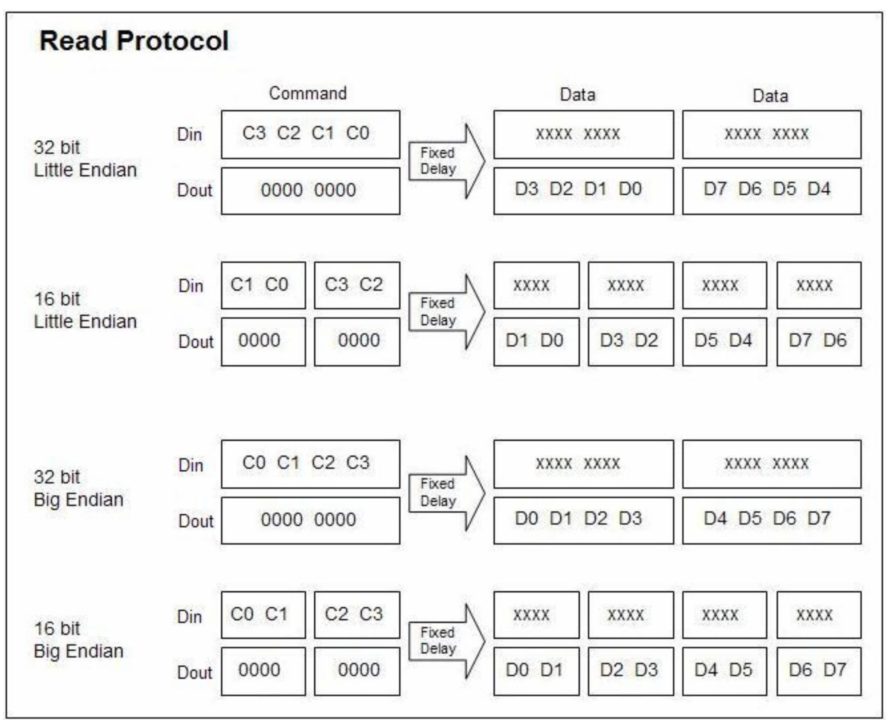


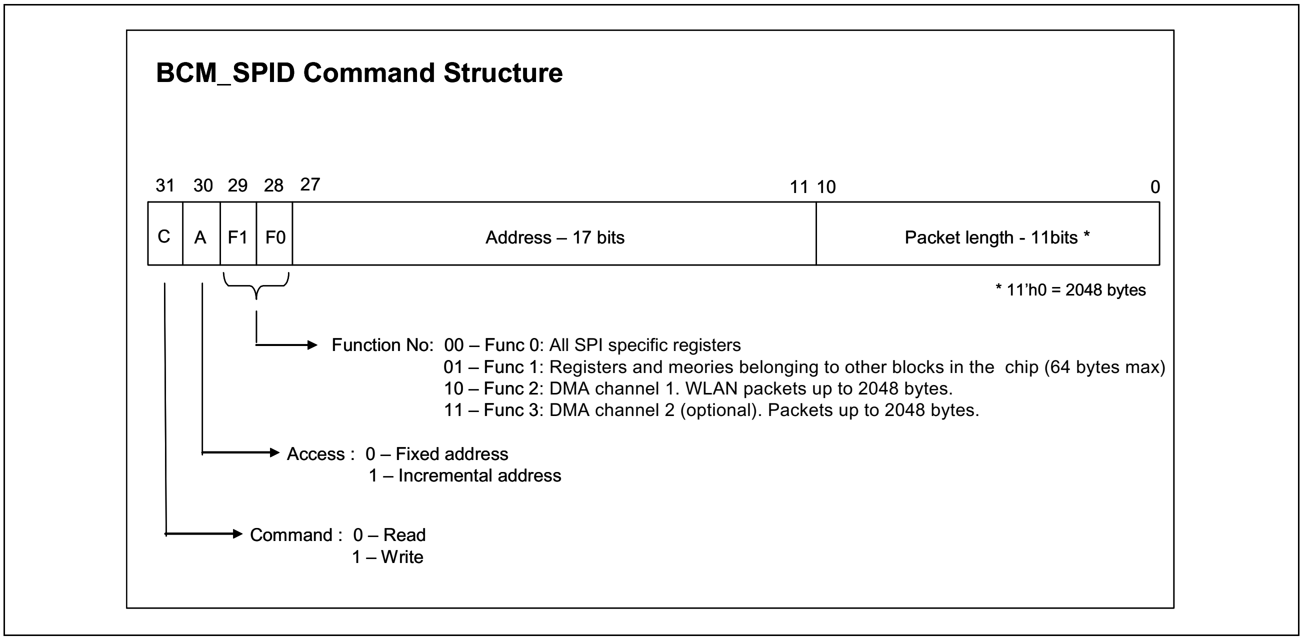
Figure 10: SPI Read Protocol



Command Structure

The SPI command structure is 32 bits. The bit positions and definitions are as shown in Figure 11.

Figure 11: SPI Command Structure



Write

The host puts the first bit of the data onto the bus one-half clock-cycle before the first active edge following the CS going low. The following bits are clocked out on the falling edge of the SPI clock. The device samples the data on the active edge.

Write-Read

The host reads on the rising edge of the clock requiring data from the device to be made available before the first rising clock edge of the clock burst for the data. The last clock edge of the fixed delay word can be used to represent the first bit of the following data word. This allows data to be ready for the first clock edge without relying on asynchronous delays.

Read

The read command always follows a separate write to set up the WLAN device for a read. This command differs from the write-read command in the following respects: a) chip selects go high between the command/address and the data and b) the time interval between the command/address is not fixed.

Status

The SPI interface supports status notification to the host after a read/write transaction. This status notification provides information about any packet errors, protocol errors, information about available packet in the RX queue, etc. The status information helps in reducing the number of interrupts to the Host. The status-reporting feature can be switched off using a register bit, without any timing overhead. The SPI bus timing for read/write transactions with and without status notification are as shown in Figure 12 and Figure 13 on page 32. See Table 2 on page 32 for information on status field details.

Figure 12: SPI Signal Timing Without Status

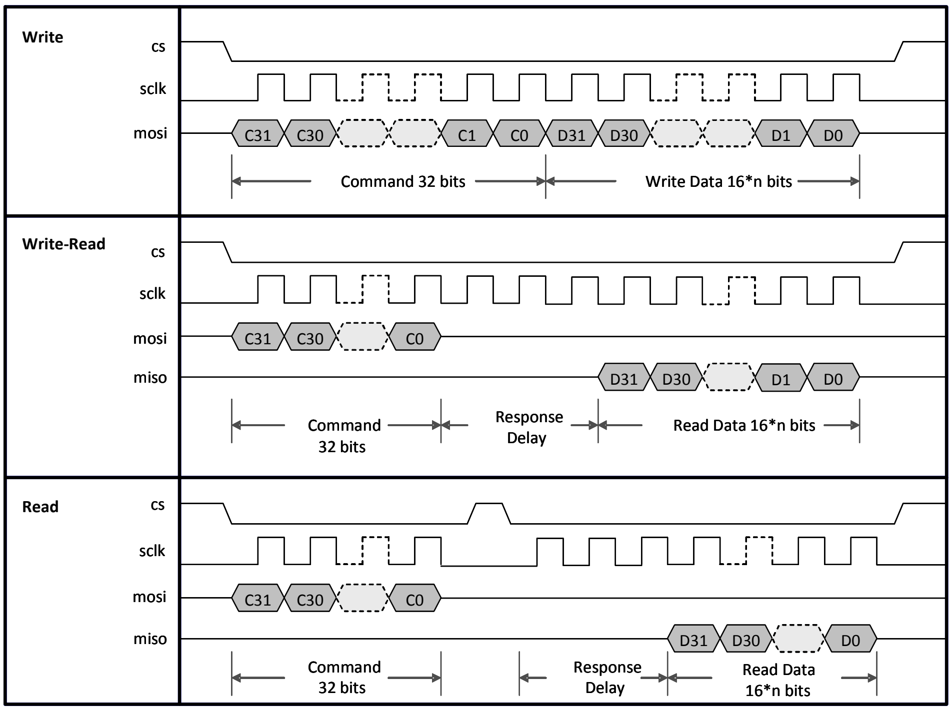


Figure 13: SPI Signal Timing with Status (Response Delay = 0)

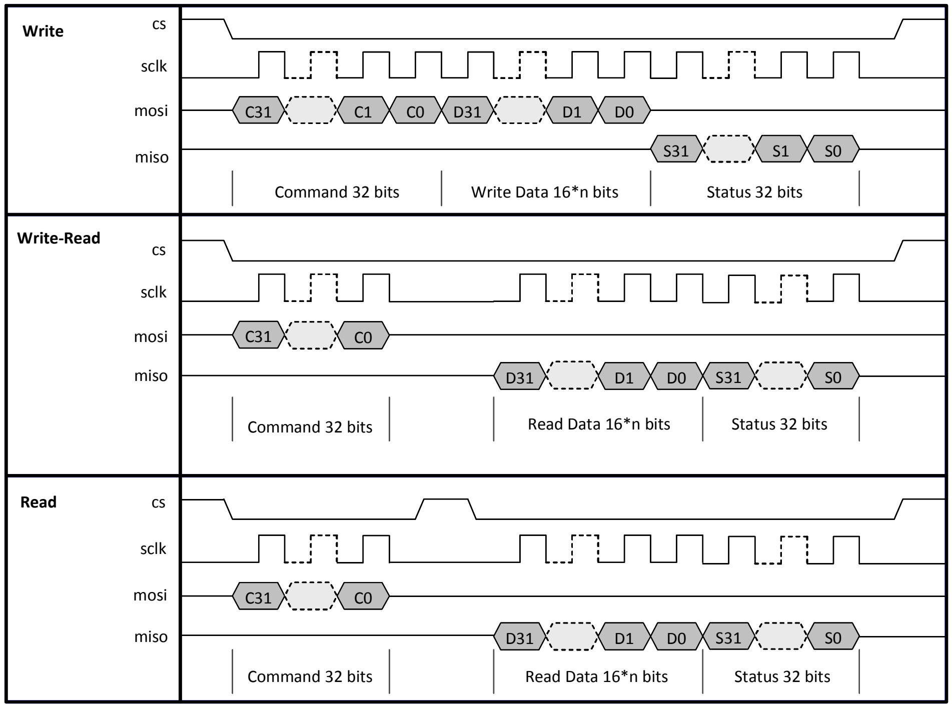


Table 2: SPI Status Field Details

Bit	Name	Description
0	Data not available	The requested read data is not available
1	Underflow	FIFO underflow occurred due to current (F2, F3) read command
2	Overflow	FIFO overflow occurred due to current (F1, F2, F3) write command
3	F2 interrupt	F2 channel interrupt
4	F3 interrupt	F3 channel interrupt
5	F2 RX Ready	F2 FIFO is ready to receive data (FIFO empty)
6	F3 RX Ready	F3 FIFO is ready to receive data (FIFO empty)
7	Reserved	–
8	F2 Packet Available	Packet is available/ready in F2 TX FIFO
9:19	F2 Packet Length	Length of packet available in F2 FIFO
20	F3 Packet Available	Packet is available/ready in F3 TX FIFO
21:31	F3 Packet Length	Length of packet available in F3 FIFO

SPI Host-Device Handshake

To initiate communication through the SPI after power-up, the Host needs to bring up the WLAN/Chip by writing to the Wake-up WLAN register bit. Writing a 1 to this bit will start up the necessary crystals and PLLs so that the BCM4319 is ready for data transfer. The device can signal an interrupt to the Host indicating that the device is awake and ready. This procedure also needs to be followed for waking up the device in sleep mode. The device can interrupt the Host using the WLAN IRQ line whenever it has any information to pass to the Host. On getting an interrupt, the Host needs to read the interrupt and/or status register to determine the cause of interrupt and then take necessary actions.

Boot-Up Sequence

After power-up, the SPI Host needs to wait for the device to be out of reset. For this, the Host needs to poll with a read command to F0 addr 0x14. Address 0x14 contains a predefined bit pattern. As soon as the Host gets a response back with the correct register content, it implies that the device has powered up and is out of reset. After that, the Host needs to set wakeup-wlan bit (F0 reg 0x00 bit 7). Wakeup-wlan issues a clock request to the PMU.

For the first time after power-up, the Host needs to wait for the availability of low power clock inside the device. Once that is available, the host needs to write to a PMU register to set the crystal frequency. This will turn on the PLL. After the PLL is locked, chipActive interrupt is issued to the Host. This indicates device awake/ready status. See Table 3 for information on SPI registers.

In Table 3, the following notation is used for register access:

- R: Readable from Host and CPU
- W: Writable from Host
- U: Writable from CPU

Table 3: SPI Registers

Address	*Register*	*Bit*	*Access*	*Default*	*Description*
x0000	Word length	0	R/W/U	0	0 – 16 bit word length 1 – 32 bit word length
	Endianess	1	R/W/U	0	0 – Little Endian 1 – Big Endian
	High speed mode	4	R/W/U	1	0 – Normal mode. RX and TX at different edges. 1 – High speed mode. RX and TX on same edge (default).
	Interrupt polarity	5	R/W/U	1	0 – Interrupt active polarity is low 1 – Interrupt active polarity is high (default)
	Wake-up	7	R/W	0	A write of 1 will denote wake-up command from Host to device. This will be followed by a F2 Interrupt from SPI device to Host, indicating device awake status.
x0001	Response delay	7:0	R/W/U	8‘h04	Configurable read response delay in multiples of 8 bits

Table 3: SPI Registers (Cont.)

Address	Register	Bit	Access	Default	Description
x0002	Status enable	0	R/W	1	0 – No status sent to host after read/write 1 – Status sent to host after read/write
	Interrupt with status	1	R/W	0	0 – Do not interrupt if status is sent 1 – Interrupt host even if status is sent
	Response delay for all	2	R/W	0	0 – Response delay applicable to F1 read only 1 – Response delay applicable to all function read
x0003	Reserved				
x0004	Interrupt register	0	R/W	0	Requested data not available; Cleared by writing a 1 to this location
		1	R	0	F2/F3 FIFO underflow due to last read
		2	R	0	F2/F3 FIFO overflow due to last write
		5	R	0	F2 packet available
		6	R	0	F3 packet available
		7	R	0	F1 overflow due to last write
x0005	Interrupt register	5	R	0	F1 Interrupt
		6	R	0	F2 Interrupt
		7	R	0	F3 Interrupt
x0006 - x0007	Interrupt enable register	15:0	R/W/U	16'hE0E7	Particular Interrupt is enabled if a corresponding bit is set
x0008 - x000B	Status register	31:0	R	32'h0000	Same as status bit definitions
x000C - x000D	F1 info register	0	R	1	F1 enabled
		1	R	0	F1 ready for data transfer
		13:2	R/U	12'h40	F1 max packet size
x000E - x000F	F2 info register	0	R/U	1	F2 enabled
		1	R	0	F2 ready for data transfer
		15:2	R/U	14'h800	F2 max packet size
x0010 - x0011	F3 info register	0	R/U	1	F3 enabled
		1	R	0	F3 ready for data transfer
		15:2	R/U	14'h800	F3 max packet size
x0014 - x0017	Test–Read only register	31:0	R	32'hFEE DBEAD	This register contains a predefined pattern, which the host can read and determine if the SPI interface is working properly.
x0018 - x001B	Test–R/W register	31:0	R/W/U	32'h0000 0000	This is a dummy register where the host can write some pattern and read it back to determine if the SPI interface is working properly.

Section 6: 802.11 a/b/g/n MAC and PHY

Introduction to the IEEE 802.11™ Standard

The IEEE 802.11™ standard defines two different ways to configure a wireless network: ad hoc mode and infrastructure mode. In ad hoc mode, nodes are brought together to form a network on the fly, whereas infrastructure mode uses fixed access points through which mobile nodes can communicate. These network access points are sometimes connected to wired networks through bridging or routing functions.

The medium access control (MAC) layer is a contention resolution protocol that is responsible for maintaining order in the use of a shared wireless medium. IEEE 802.11 specifies both contention-based and contention-free channel access mechanisms. The contention-based scheme is also called the distributed coordination function (DCF) and the contention-free scheme is also called the point coordination function (PCF).

The DCF employs a carrier sense multiple access with collision avoidance (CSMA/CA) protocol. In this protocol, when the MAC receives a packet to be transmitted from its higher layer, the MAC first listens to ensure that no other node is transmitting. If the channel is clear, it then transmits the packet. Otherwise, it chooses a random backoff factor that determines the amount of time the node must wait until it is allowed to transmit its packet. During periods in which the channel is clear, the MAC waiting to transmit decrements its backoff counter, and when the channel is busy, it does not decrement its backoff counter. When the backoff counter reaches zero, the MAC transmits the packet. Because the probability that two nodes will choose the same backoff factor is low, collisions between packets are minimized. Collision detection, as employed in Ethernet, cannot be used for the radio frequency transmissions of devices following IEEE 802.11. The IEEE 802.11 nodes are half-duplex—when a node is transmitting, it cannot hear any other node in the system that is transmitting because its own signal drowns out any others arriving at the node.

Optionally, when a packet is to be transmitted, the transmitting node can first send out a short request to send (RTS) packet containing information on the length of the packet. If the receiving node hears the RTS, it responds with a short clear to send (CTS) packet. After this exchange, the transmitting node sends its packet. When the packet is received successfully, as determined by a cyclic redundancy check (CRC), the receiving node transmits an acknowledgment (ACK) packet. This back and forth exchange is necessary to avoid the hidden node problem. Hidden node is a situation where node A can communicate with node B, node B can communicate with node C, but node A cannot communicate with node C. For instance, although node A can sense that the channel is clear, node C can be transmitting to node B. This protocol alerts node A that node B is busy, and that it must wait before transmitting its packet.

MAC Features

The BCM4319 WLAN MAC supports features specified in the 802.11 base standard plus those amended by 802.11n. The salient features are listed below:

- Transmission and reception of aggregated MAC protocol data units (A-MPDUs)
- Support for power management schemes, including Wi-Fi Multimedia™ (WMM®) power save, Power Save Multipoll (PSMP) and multiphase PSMP operation
- Support for immediate ACK and Block-ACK policies

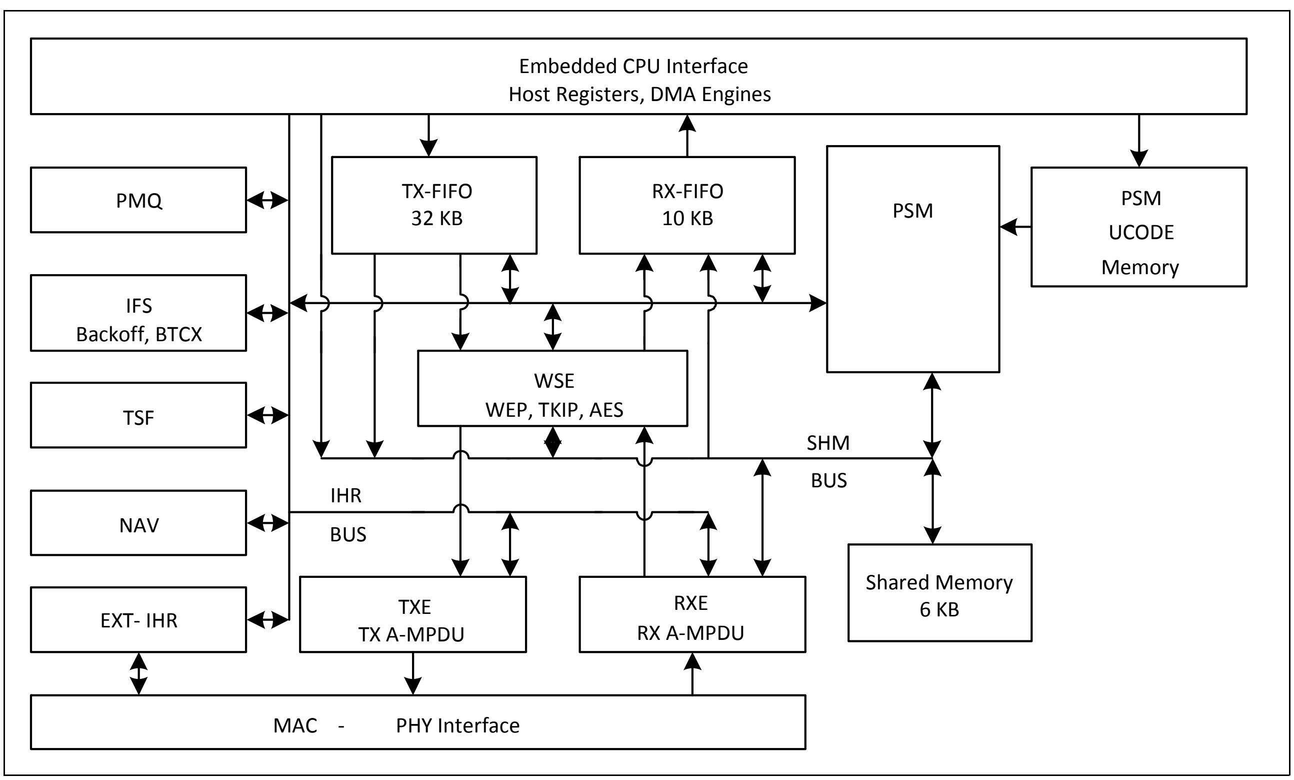
- Interframe space timing support, including reduced interframe spacing (RIFS)
- Support for RTS/CTS and CTS-to-self frame sequences for protecting frame exchanges
- Back-off counters in hardware for supporting multiple priorities as specified in the WMM® specification
- Timing synchronization function (TSF), network allocation vector (NAV) maintenance, and target beacon transmission time (TBTT) generation in hardware
- Hardware offload for AES-CCMP, legacy WPA™ TKIP, legacy WEP ciphers, and support for key management
- Support for coexistence with Bluetooth® (BT) and other external radios
- Programmable independent basic service set (IBSS) or infrastructure basic service set functionality
- Statistics counters for management information base (MIB) support

MAC Description

The BCM4319 WLAN MAC is designed to support high throughput operation with low power consumption. In addition, several power saving modes have been implemented that allow the MAC to consume very little power while maintaining network wide timing synchronization. The architecture diagram of the MAC is shown in Figure 14.

The following sections provide an overview of the important MAC modules.

Figure 14: WLAN MAC Architecture



PSM

The programmable state machine (PSM) is a microcode engine that provides most of the low-level hardware control for implementing the 802.11 specification. It is a microcontroller that is highly optimized for flow control operations, which are predominant in implementations of communication protocols. The instruction set and fundamental operations are simple and general, which allows algorithms to be optimized late in the design process. It also allows algorithm changes to track evolving 802.11 specifications.

The PSM fetches instructions from the microcode memory. It uses shared memory to obtain operands for instructions and to exchange data between both the host and the MAC data pipeline (via the SHM bus). The PSM also uses a scratchpad memory, similar to a register bank, to store frequently accessed and temporary variables.

The PSM exercises fine grained control over the hardware engines by programming Internal Hardware Registers (IHRs). These IHRs are colocated with the hardware functions they control, and are accessed by the PSM via the IHR bus.

The PSM fetches instructions from the microcode memory using an address determined by the program counter, instruction literal, or a program stack. For arithmetic and logic unit (ALU) operations, the operands are obtained from shared memory, scratchpad memory, IHRs, or instruction literals, and the results are written into the shared memory, scratchpad memory, or IHRs.

There are two basic branch instructions: conditional branches and ALU-based branches. To better support the many decision points in the 802.11 algorithms, branches can depend on either readily available signals from the hardware modules (branch condition signals are available to the PSM without polling the IHRs) or on the results of ALU operations.

WSE

TheWireless Security Engine (WSE) encapsulates all the hardware accelerators to perform encryption, decryption, and message integrity check (MIC) computation and verification. The accelerators implement the legacy WEP, WPA TKIP, and WPA2™ AES-CCMP cipher algorithms.

The PSM determines the appropriate cipher algorithm to use based on frame type and association information. It supplies the keys to the hardware engines from an on-chip key table. WSE interfaces with the transmit engine (TXE) to encrypt and compute the MIC on transmit frames and the receive engine (RXE) to decrypt and verify the MIC on receive frames.

TXE

The TXE constitutes the transmit data path of the MAC. It coordinates the DMA engines to store the transmit frames in the TXFIFO. It interfaces with the WSE module to encrypt frames, and transfers the frames across the MAC-PHY interface at the appropriate time determined by the channel access mechanisms.

The data received from the DMA engines are stored in transmit FIFOs. The MAC supports multiple logical queues to support traffic streams that have different Quality of Service (QoS) priority requirements. The PSM uses the channel access information from the interframe spacing (IFS) module to schedule a queue from which the next frame is transmitted. Once the frame is scheduled, the TXE hardware transmits the frame based on a precise timing trigger received from the IFS module.

The TXE module also contains the hardware that allows the rapid assembly of MPDUs into an A-MPDU for transmission. The hardware module aggregates the encrypted MPDUs by adding appropriate headers and pad delimiters as needed.

RXE

The RXE constitutes the receive data path of the MAC. It interfaces with the DMA engine to drain the received frames from the RXFIFO. It transfers bytes across the MAC-PHY interface and interfaces with the WSE module to decrypt frames. The decrypted data is stored in the RXFIFO.

The RXE module contains programmable filters that are programmed by the PSM to accept or filter frames based on several criteria such as receiver address, BSSID, and certain frame types.

The RXE module also contains the hardware required to detect A-MPDUs, parse the headers of the containers, and disaggregate them into component MPDUS.

IFS

The IFS module contains the timers required to determine interframe space timing including RIFS timing. It also contains multiple backoff engines required to support prioritized access to the medium as specified by WMM.

The interframe spacing timers are triggered by the cessation of channel activity on the medium as indicated by the PHY. These timers provide precise timing to the TXE to begin frame transmission. The TXE uses this information to send response frames or perform transmit frame bursting (RIFS or SIFS separated, as within a TXOP).

The backoff engines (for each access category) monitor channel activity in each slot duration to determine whether to continue or pause the backoff counters. When the backoff counters reach 0, the TXE gets notified so that it may commence frame transmission. In the event that multiple backoff counters decrement to 0 at the same time, the hardware resolves the conflict based on policies provided by the PSM.

The IFS module also incorporates hardware that allows the MAC to enter a low-power state when operating under the IEEE power-save mode. In this mode, the MAC is in a suspended state with its clock turned off. A sleep timer, whose count value is initialized by the PSM, runs on a slow clock and determines the duration over which the MAC remains in this suspended state. The MAC is restored to its functional state when the timer expires. The PSM updates the TSF timer based on the sleep duration, ensuring that the TSF is synchronized to the network.

The IFS module also contains the PTA hardware that assists the PSM in Bluetooth coexistence functions.

TSF

The TSF module maintains the TSF timer of the MAC. It also maintains the target beacon transmission time (TBTT). The TSF timer hardware, under the control of the PSM, is capable of adopting timestamps received from beacon and probe response frames in order to maintain synchronization with the network.

The TSF module also generates trigger signals for events that are specified as offsets from the TSF timer, such as uplink and downlink transmission times used in PSMP.

NAV

The network allocation vector (NAV) timer module is responsible for maintaining the NAV information conveyed through the duration field of MAC frames. This ensures that the MAC complies with the protection mechanisms specified in the standard.

The hardware, under the control of the PSM, maintains the NAV timer and updates the timer appropriately based on received frames. This timing information is provided to the IFS module, which uses it as a virtual carrier-sense indication.

MAC-PHY Interface

The MAC-PHY interface consists of a data path interface to exchange RX/TX data from/to the PHY. In addition, there is a programming interface that can be controlled either by the host or the PSM to configure and control the PHY.

PHY Features

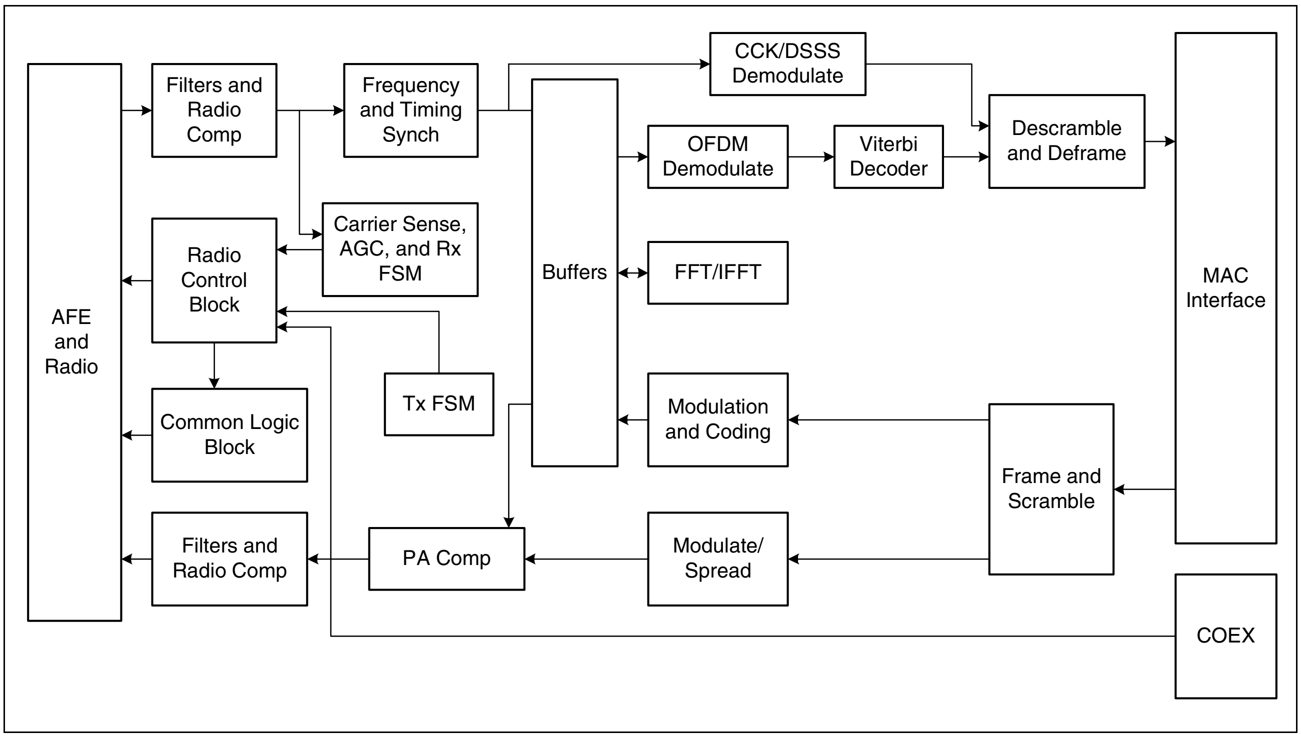
- Supports IEEE 802.11a, 11b, 11g, 11n single stream, and 11j PHY standards
- 802.11n single-stream operation in 20 MHz or 40 MHz channels
- Supports Optional Short GI and Green Field modes in Tx and Rx.
- Supports optional Space-Time Block Code (STBC) reception of two space-time streams.
- Supports 802.11h/k for worldwide operation
- Algorithms achieving low power, enhanced sensitivity, range, and reliability
- Automatic gain control scheme for blocking and non-blocking during cellular application scenarios
- Closed-loop transmit power control
- Digital RF chip calibration algorithms to handle CMOS RF chip non-idealities
- On-the-fly channel frequency and transmit power selection
- Supports per packet Rx Antenna diversity
- Designed to meet FCC and other regulatory requirements

PHY Description

The BCM4319 WLAN digital PHY is designed to comply with IEEE 802.11a/b/g/j/n single stream to provide WLAN connectivity supporting data rates from 1 Mbps to 72.2 Mbps (150 Mbps in the 40 MHz channel) for low power, high performance, handheld applications.

The PHY has been designed to work with interference, radio nonlinearity, and impairments. It incorporates efficient implementations of the filters, fast fourier transform (FFT), and Viterbi-decoder algorithms. Efficient algorithms have been designed to achieve maximum throughput and reliability, including algorithms for carrier sense/rejection, frequency/phase/timing acquisition and tracking, and channel estimation and tracking. The PHY receiver also contains a robust 11b demodulator. The PHY carrier sense has been tuned to provide high throughput for 802.11g/11b hybrid networks with Bluetooth coexistence. It has also been designed for shared single antenna systems between WLAN and BT to support simultaneous Rx-Rx. In dual antenna designs, the digital PHY has been designed for Maximal Ratio Combining (MRC) in RF.

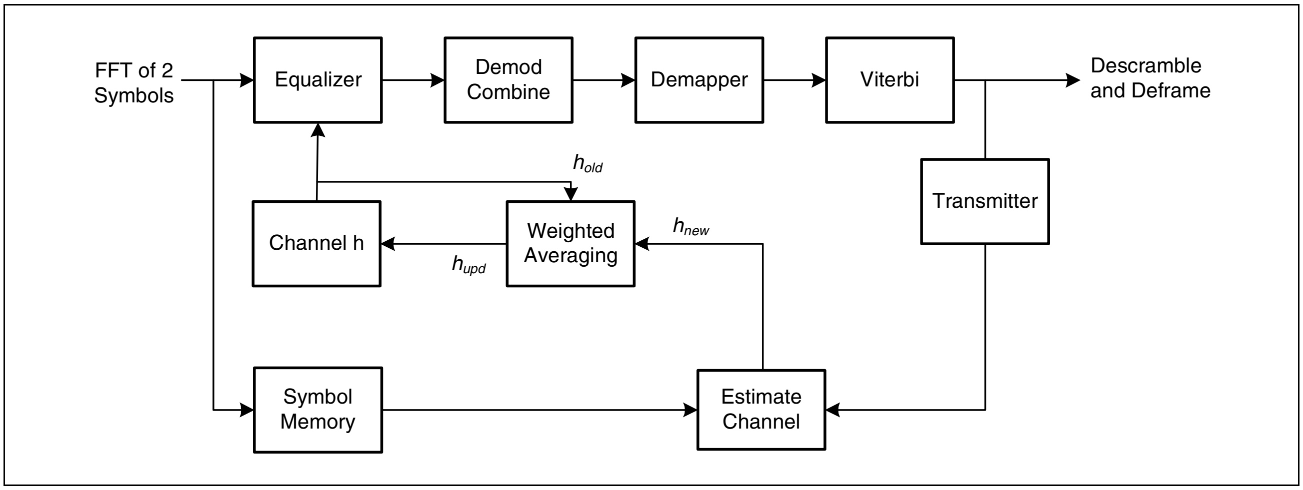
Figure 15: WLAN PHY Block Diagram



The PHY is capable of fully calibrating the RF front end to extract the highest performance. On power-up, PHY calibrations correct for IQ mismatch and local oscillator leakage. PHY periodic calibrations compensate for temperature related drift to yield high performance over time. A closed-loop transmit control algorithm maintains the output power to a fixed level with the capability to control Tx power on a per packet basis.

The PHY can receive two spatial streams. The STBC scheme can obtain diversity gains by using multiple transmit antennas at the access point (AP) in a fading channel environment, without increasing the complexity at the station (STA). Details of STBC reception are shown in Figure 16 on page 41.

Figure 16: STBC Receive Block Diagram

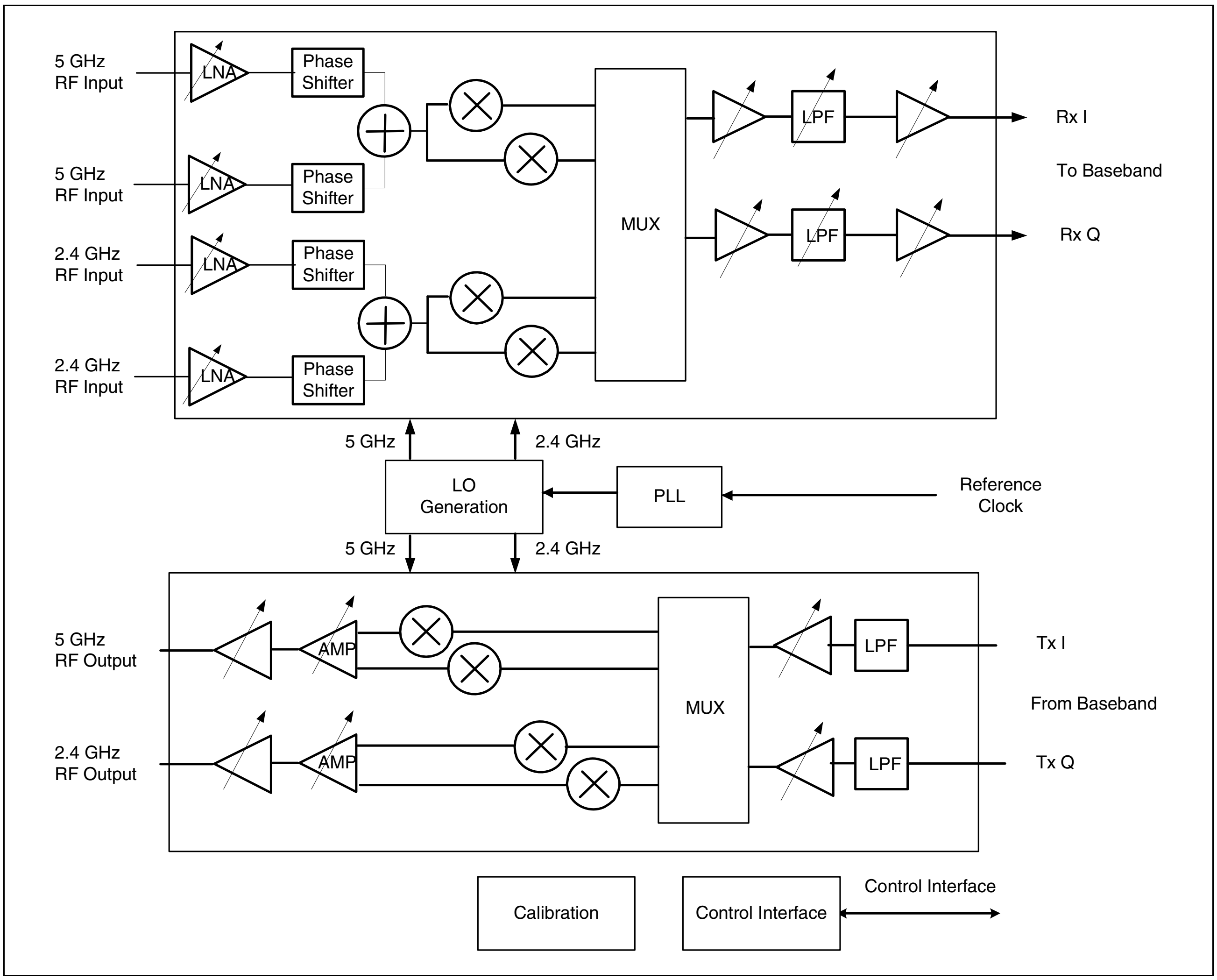


In STBC mode, symbols are processed in pairs. Equalized output symbols are linearly combined and decoded. Channel estimates are refined on every pair of symbols using the received symbols and reconstructed symbols.

Section 7: WLAN 802.11 Radio Subsystem

The BCM4319 includes an integrated dual-band WLAN RF transceiver that has been optimized to provide low power, low cost, and robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM or 5 GHz U-NII bands (but not both simultaneously). With its integrated internal transmit power amplifiers, it provides full output power per the IEEE 802.11a/b/g/n specifications. Support for optional external power amplifiers is also provided. The transmit and receive sections include on-chip filtering, mixing, and gain control functions.

Figure 17: Radio Functional Block Diagram



Receiver Path

The BCM4319 has a wide dynamic range, direct conversion receiver. It employs high order, on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band or the entire 5 GHz U-NII band. The excellent noise figure of the receiver makes an external Low-Noise Amplifier (LNA) unnecessary.

Transmitter Path

In the transmit path, baseband data is modulated and upconverted to the 2.4 GHz ISM or 5 GHz U-NII bands, respectively. The integrated linear on-chip PAs are capable of delivering a nominal output power of 20 dBm while meeting the IEEE 802.11a and 802.11g specifications. The TX gain has a 32 dB range with a resolution of 0.25 dB.

Calibration

The BCM4319 features dynamic on-chip calibration, eliminating process variation across components. This enables the BCM4319 to be used in high-volume applications because calibration routines are not required during manufacturing testing. These calibration routines are performed periodically in the course of normal radio operation. An example of this is automatic calibration of the baseband filters for optimum transmit and receive performance.

Section 8: Pin Assignments

5.79 mm x 4.58 mm 138-BALL WLBGA Package

Table 4: 5.79 mm x 4.58 mm 138-Ball WLBGA

	1	2	3	4	5	6	7	8	9	10	11	
WA	WRF_GNDPAA_3P3	WRF_GNDTX_1P2	WRF_VDDTX_1P2	WRF_RFINP_A1	WRF_VDDRX_1P2	WRF_RFINP_G1	–	WRF_RFINN_G1_XFMR	WRF_GNDCAB_1P2	xtalin	–	**WA**
WB	WRF_VDDPAA_3P3	WRF_RFOUTP_A	–	WRF_RFINN_A1_XFMR	WRF_GNDRX_1P2	–	–	WRF_GNDD_1P2	WRF_RES_EXT	–	VDDXO	**WB**
WC	WRF_GNDPAA_3P3	WRF_GNDPAG_3P3	–	–	WRF_VDDLO_1P2	–	WRF_VDDA_1P2	WRF_VDDD_1P2	WRF_VDDPFDCP_1P2	VDD	xtalout	**WC**
WD	WRF_VDDPAG_3P3	–	–	–	–	–	–	WRF_GNDA_1P2	WRF_GNDPFDCP_1P2	VSS	VSSXO	**WD**
WE	WRF_RFOUTP_G	WRF_GNDPAG_3P3	WRF_AFE_PAD_TSSI_G	WRF_GPIO_OUT2	WRF_GNDLO_1P2	WRF_VDDVCO_1P2	WRF_GNDVCO_1P2	WRF_VDDCAB_1P2	–	XTAL_PU	SDIO_CMD	**WE**
WF	WRF_AFE_PAD_TEST_IP	WRF_AFE_PAD_TEST_IN	WRF_AFE_PAD_IQADC_VREF	WRF_GPIO_OUT1	VSS	VDDIO	VDD	SDIO_DATA_3	WRF_EXTREFIN	WL_REG_ON	GPIO_9	**WF**
WG	WRF_AFE_PAD_AVSS_RXADC	WRF_AFE_PAD_AVDD_RXADC	WRF_AFE_PAD_AVDD_AUX	WRF_BBPLL_GND_1P2	GMODE_EXT_LNA_PU	GMODE_EXT_LNA_GAIN	RF_SW_CTRL_N_0	RF_SW_CTRL_P_0	VDDIO_SD	VDDIO_SD	SDIO_DATA_2	**WG**
WH	WRF_AFE_PAD_TEST_OP	WRF_AFE_PAD_TEST_ON	WRF_AFE_PAD_TSSI_A	WRF_BBPLL_VDD_1P2	TDI	TMS	GMODE_TX_PU	RF_SW_CTRL_N_2	RF_SW_CTRL_P_2	GPIO_1	SDIO_DATA_1	**WH**
WJ	AMODE_TX_PU	VDDIO_RF	TCK	JTAG_TRST_L	RF_SW_CTRL_N_3	RF_SW_CTRL_P_3	AMODE_EXT_LNA_PU	AMODE_EXT_LNA_GAIN	GPIO_3	GPIO_7	SDIO_DATA_0	**WJ**
WK	TDO	VDDIO_RF	BTCX_RF_ACTIVE	VSS	VDD	OTP_VDD33	VDDIO	GPIO_0	GPIO_2	GPIO_6	SDIO_CLK	**WK**
WL	usb20phy_avdd25_pad	usb20phy_avdd12_pad	BTCX_STATUS	BTCX_FREQ	BT_REG_ON	WL_REG_ON	VDD_LNLDO2	VOUT_LNLDO2	SR_TESTSWG	SR_VDDBAT1	SR_VDDBAT1	**WL**
WM	usb20phy_rref_pad	usb20phy_avdd33_pad	usb20phy_moncdr_pad	GPIO_8	AVSS_LDO	VREF_LDO	SR_PNPO	SR_PAVSS	SR_AVSS	SR_PVSS1	SR_VLX1	**WM**
WN	usb20_dev_dpls	usb20phy_agndpll_pad	usb20phy_monpll_pad	UART_TX	VDD_CLDO	VDD_LNLDO1	SR_PALDO	SR_VDDBAT3	SR_VDDBAT2	SR_PVSS1	SR_VLX1	**WN**
WP	usb20_dev_dmns	usb20phy_agnd_pad	BTCX_TXCONF	UART_RX	VOUT_CLDO	VOUT_LNLDO1	SR_PALDO	SR_VDDBAT3	SR_AVDD2P5	SR_VDDNLDO	SR_VSSPLDO	**WP**

Section 9: Pinout and Signal Descriptions

Signal Assignments

138-Ball WLBGA Pinout

The 138-Ball WLBGA pinout is provided in Table 5.

Note: The X- and Y-coordinate orientation is looking at the silicon face (i.e., looking up at the bottom of the die at the bumps, as opposed to top down). See Figure 25 on page 81 for the origin location (0, 0).

Bump Side View (0,0 center of die)

Table 5: WLBGA Signal Assignments by Pin Number and X- and Y-Coordinates

Ball Pad	*Signal Name*	*X Coord*	*Y Coord*
WA1	WRF_GNDPAA_3P3	–2654.9	1940
WA10	XTALIN	–2654.9	–1660
WA2	WRF_GNDTX_1P2	–2654.9	1540
WA3	WRF_VDDTX_1P2	–2654.9	1140
WA4	WRF_RFINP_A1	–2654.9	740
WA5	WRF_VDDRX_1P2	–2654.9	340
WA6	WRF_RFINP_G1	–2654.9	–60
WA8	WRF_RFINN_G1_XFMR	–2654.9	–860
WA9	WRF_GNDCAB_1P2	–2654.9	–1260
WB1	WRF_VDDPAA_3P3	–2254.9	1940
WB11	VDDXO	–2254.9	–2060
WB2	WRF_RFOUTP_A	–2254.9	1540
WB4	WRF_RFINN_A1_XFMR	–2254.9	740
WB5	WRF_GNDRX_1P2	–2254.9	340
WB8	WRF_GNDD_1P2	–2254.9	–860
WB9	WRF_RES_EXT	–2254.9	–1260
WC1	WRF_GNDPAA_3P3	–1854.9	1940
WC10	VDD	–1854.9	–1660
WC11	XTALOUT	–1854.9	–2060
WC2	WRF_GNDPAG_3P3	–1854.9	1540
WC5	WRF_VDDLO_1P2	–1854.9	340
WC7	WRF_VDDA_1P2	–1854.9	–460
WC8	WRF_VDDD_1P2	–1854.9	–860

Table 5: WLBGA Signal Assignments by Pin Number and X- and Y-Coordinates (Cont.)

Ball Pad	*Signal Name*	*X Coord*	*Y Coord*
WC9	WRF_VDDPFDCP_1P2	–1854.9	–1260
WD1	WRF_VDDPAG_3P3	–1454.9	1940
WD10	VSS	–1454.9	–1660
WD11	VSSXO	–1454.9	–2060
WD8	WRF_GNDA_1P2	–1454.9	–860
WD9	WRF_GNDPFDCP_1P2	–1454.9	–1260
WE1	WRF_RFOUTP_G	–1054.9	1940
WE10	XTAL_PU	–1054.9	–1660
WE11	SDIO_CMD	–1054.9	–2060
WE2	WRF_GNDPAG_3P3	–1054.9	1540
WE3	WRF_AFE_PAD_TSSI_G	–1054.9	1140
WE4	WRF_GPIO_OUT2	–1054.9	740
WE5	WRF_GNDLO_1P2	–1054.9	340
WE6	WRF_VDDVCO_1P2	–1054.9	–60
WE7	WRF_GNDVCO_1P2	–1054.9	–460
WE8	WRF_VDDCAB_1P2	–1054.9	–860
WF1	WRF_AFE_PAD_TEST_IP	–654.9	1940
WF10	WL_REG_ON	–654.9	–1660
WF11	GPIO_9	–654.9	–2060
WF2	WRF_AFE_PAD_TEST_IN	–654.9	1540
WF3	WRF_AFE_PAD_IQADC_VREF	–654.9	1140
WF4	WRF_GPIO_OUT1	–654.9	740
WF5	VSS	–654.9	340
WF6	VDDIO	–654.9	–60
WF7	VDD	–654.9	–460
WF8	SDIO_DATA_3	–654.9	–860
WF9	WRF_EXTREFIN	–654.9	–1260
WG1	WRF_AFE_PAD_AVSS_RXADC	–254.9	1940
WG10	VDDIO_SD	–254.9	–1660
WG11	SDIO_DATA_2	–254.9	–2060
WG2	WRF_AFE_PAD_AVDD_RXADC	–254.9	1540
WG3	WRF_AFE_PAD_AVDD_AUX	–254.9	1140
WG4	WRF_BBPLL_GND_1P2	–254.9	740
WG5	GMODE_EXT_LNA_PU	–254.9	340
WG6	GMODE_EXT_LNA_GAIN	–254.9	–60
WG7	RF_SW_CTRL_N_0	–254.9	–460
WG8	RF_SW_CTRL_P_0	–254.9	–860
WG9	VDDIO_SD	–254.9	–1260
WH1	WRF_AFE_PAD_TEST_OP	145.1	1940

Table 5: WLBGA Signal Assignments by Pin Number and X- and Y-Coordinates (Cont.)

Ball Pad	Signal Name	X Coord	Y Coord
WH10	GPIO_1	145.1	–1660
WH11	SDIO_DATA_1	145.1	–2060
WH2	WRF_AFE_PAD_TEST_ON	145.1	1540
WH3	WRF_AFE_PAD_TSSI_A	145.1	1140
WH4	WRF_BBPLL_VDD_1P2	145.1	740
WH5	TDI	145.1	340
WH6	TMS	145.1	–60
WH7	GMODE_TX_PU	145.1	–460
WH8	RF_SW_CTRL_N_2	145.1	–860
WH9	RF_SW_CTRL_P_2	145.1	–1260
WJ1	AMODE_TX_PU	545.1	1940
WJ10	GPIO_7	545.1	–1660
WJ11	SDIO_DATA_0	545.1	–2060
WJ2	VDDIO_RF	545.1	1540
WJ3	TCK	545.1	1140
WJ4	JTAG_TRST_L	545.1	740
WJ5	RF_SW_CTRL_N_3	545.1	340
WJ6	RF_SW_CTRL_P_3	545.1	–60
WJ7	AMODE_EXT_LNA_PU	545.1	–460
WJ8	AMODE_EXT_LNA_GAIN	545.1	–860
WJ9	GPIO_3	545.1	–1260
WK1	TDO	945.1	1940
WK10	GPIO_6	945.1	–1660
WK11	SDIO_CLK	945.1	–2060
WK2	VDDIO_RF	945.1	1540
WK3	BTCX_RF_ACTIVE	945.1	1140
WK4	VSS	945.1	740
WK5	VDD	945.1	340
WK6	OTP_VDD33	945.1	–60
WK7	VDDIO	945.1	–460
WK8	GPIO_0	945.1	–860
WK9	GPIO_2	945.1	–1260
WL1	USB20PHY_AVDD25_PAD	1345.1	1940
WL10	SR_VDDBAT1	1345.1	–1660
WL11	SR_VDDBAT1	1345.1	–2060
WL2	USB20PHY_AVDD12_PAD	1345.1	1540
WL3	BTCX_STATUS	1345.1	1140
WL4	BTCX_FREQ	1345.1	740
WL5	BT_REG_ON	1345.1	340

Table 5: WLBGA Signal Assignments by Pin Number and X- and Y-Coordinates (Cont.)

Ball Pad	Signal Name	X Coord	Y Coord
WL6	WL_REG_ON	1345.1	–60
WL7	VDD_LNLDO2	1345.1	–460
WL8	VOUT_LNLDO2	1345.1	–860
WL9	SR_TESTSWG	1345.1	–1260
WM1	USB20PHY_RREF_PAD	1745.1	1940
WM10	SR_PVSS1	1745.1	–1660
WM11	SR_VLX1	1745.1	–2060
WM2	USB20PHY_AVDD33_PAD	1745.1	1540
WM3	USB20PHY_MONCDR_PAD	1745.1	1140
WM4	GPIO_8	1745.1	740
WM5	AVSS_LDO	1745.1	340
WM6	VREF_LDO	1745.1	–60
WM7	SR_PNPO	1745.1	–460
WM8	SR_PAVSS	1745.1	–860
WM9	SR_AVSS	1745.1	–1260
WN1	USB20_DEV_DPLS	2145.1	1940
WN10	SR_PVSS1	2145.1	–1660
WN11	SR_VLX1	2145.1	–2060
WN2	USB20PHY_GNDPLL_PAD	2145.1	1540
WN3	USB20PHY_MONPLL_PAD	2145.1	1140
WN4	UART_TX	2145.1	740
WN5	VDD_CLDO	2145.1	340
WN6	VDD_LNLDO1	2145.1	–60
WN7	SR_PALDO	2145.1	–460
WN8	SR_VDDBAT3	2145.1	–860
WN9	SR_VDDBAT2	2145.1	–1260
WP1	USB20_DEV_DMNS	2545.1	1940
WP10	SR_VDDNLDO	2545.1	–1660
WP11	SR_VSSPLDO	2545.1	–2060
WP2	USB20PHY_AGND_PAD	2545.1	1540
WP3	BTCX_TXCONF	2545.1	1140
WP4	UART_RX	2545.1	740
WP5	VOUT_CLDO	2545.1	340
WP6	VOUT_LNLDO1	2545.1	–60
WP7	SR_PALDO	2545.1	–460
WP8	SR_VDDBAT3	2545.1	–860
WP9	SR_AVDD2P5	2545.1	–1260

Signal Descriptions

138-Ball WLBGA Package

Signal descriptions for the 138-Ball WLBGA are provided in Table 6. *See Table 7: “SDIO Pin Descriptions,” on page 54 for additional information.

Note: Digital IOs are *not* failsafe. Other devices should not drive BCM4319 lines when the corresponding IO supply is absent. If such a requirement exists in the system, add a series resistor greater than 3.9 KΩ on the line.

Note: Internal pulls on digital IOs are active only when VDDC and the corresponding IO supply are present.

Note: XTALIN *is* failsafe.

Table 6: 138-Ball WLBGA Signal Descriptions

Ball	Signal Name	Type	Description
RF Interface			
WE1	WRF_RFOUTP_G	O	802.11g internal power amplifier RF output
WA6	WRF_RFINP_G1	I	802.11g RX RF input (50Ω)
WA8	WRF_RFINN_G1_XFMR	O	802.11g RX transformer RF ground
WE3	WRF_AFE_PAD_TSSI_G	I	Transmit signal strength indicator for optional external 802.11g power amplifier. Leave NC if not used.
WB2	WRF_RFOUTP_A	O	802.11a internal power amplifier RF output.
WA4	WRF_RFINP_A1	I	802.11a RX RF input (50Ω)
WB4	WRF_RFINN_A1_XFMR	I	802.11a RX transformer RF ground
WH3	WRF_AFE_PAD_TSSI_A	I	Transmit signal strength indicator for optional external 802.11a power amplifier. Leave NC if not used.
WB9	WRF_RES_EXT	O	Connect to external 15 kΩ (1% tolerance) resistor to ground.
RF Control Lines (IO Supply = VDDIO_RF)			
WG8	RF_SW_CTRL_P_0	O	Programmable RF switch control lines: default = low.
WG7	RF_SW_CTRL_N_0	O	
WH9	RF_SW_CTRL_P_2	O	
WH8	RF_SW_CTRL_N_2	O	
WJ6	RF_SW_CTRL_P_3	O	Programmable RF switch control line: default = high.
WJ5	RF_SW_CTRL_N_3	O	Programmable RF switch control line: default = low.
WH7	GMODE_TX_PU	O	802.11g optional external PA control
WG5	GMODE_EXT_LNA_PU	O	Enable signal for optional external 802.11g LNA
WG6	GMODE_EXT_LNA_GAIN	O	Control signal for optional external 802.11g LNA
WJ1	AMODE_TX_PU	O	802.11a optional external PA control

Table 6: 138-Ball WLBGA Signal Descriptions (Cont.)

Ball	Signal Name	Type	Description
WJ7	AMODE_EXT_LNA_PU	O	Enable signal for optional external 802.11a LNA.
WJ8	AMODE_EXT_LNA_GAIN	O	Control signal for optional external 802.11a LNA.
Integrated LDOs			
WN5	VDD_CLDO	I	Input supply pin for CLDO: also functions as the feedback pin for the CBUCK switching regulator
WN6	VDD_LNLDO1	I	Input supply pin for LNLDO1
WL7	VDD_LNLDO2	I	Input supply pin for LNLDO2 (backup linear regulator)
WP5	VOUT_CLDO	O	1.2V output for core LDO, 200 mA
WP6	VOUT_LNLDO1	O	1.2V output for low noise LNLDO1, 150 mA
WL8	VOUT_LNLDO2	O	1.2V or 2.5V–3.1V programmable output for low noise LNLDO2, 50 mA
WM6	VREF_LDO	O	Vref bypass: Connect external decoupling capacitor to ground.
WP9	SR_AVDD2P5	O	2.5V LDO2p5 output: used for various internal BCM4319 blocks in addition to the USB PHY: the output capacitor is *required* even when USB functionality is not used.
WN7	SR_PALDO	O	Internal PALDO output or feedback of output from external PNP
WP7	SR_PALDO	O	
WM7	SR_PNPO	O	Control output for PNP base
WL9	SR_TESTSWG	O	Test output for switcher/LDOs
WN8	SR_VDDBAT3	I	Battery supply input for PALDO
WP8	SR_VDDBAT3	I	
WP10	SR_VDDNLDO	O	NLDO reference pin output: Connect to 220 nF external capacitor to ground. Do not use for other external circuits.
Integrated Switching Regulator			
WL10	SR_VDDBAT1	I	Core buck regulator: Battery voltage input
WL11	SR_VDDBAT1	I	
WN9	SR_VDDBAT2	I	
WM11	SR_VLX1	O	Core buck regulator: Output to inductor
WN11	SR_VLX1	O	–
WP11	SR_VSSPLDO	I	Tracks battery voltage: Connect to 220 nF external capacitor to battery.
SDIO Bus Interface* (IO supply = VDDIO_SD)			
WE11	SDIO_CMD	I/O	SDIO command line
WJ11	SDIO_DATA_0	I/O	SDIO data line 0
WH11	SDIO_DATA_1	I/O	SDIO data line 1
WG11	SDIO_DATA_2	I/O	SDIO data line 2
WF8	SDIO_DATA_3	I/O	SDIO data line 3
WK11	SDIO_CLK	I/O	SDIO clock

Table 6: 138-Ball WLBGA Signal Descriptions (Cont.)

Ball	Signal Name	Type	Description
USB 2.0 Interface			
WN1	USB20_DEV_DPLS	I/O	USB port data plus
WP1	USB20_DEV_DMNS	I/O	USB port data minus
WM1	USB20PHY_RREF_PAD	I/O	USB PHY bandgap reference resistor. Connect to ground via a 4.02k resistor in parallel with a 100 pF capacitor.
WM3	USB20PHY_MONCDR_PAD	I/O	USB CDR monitor (reserved for testing)
WN3	USB_MONPLL	I/O	USB PHY PLL monitor (reserved for testing)
UART Interface (IO supply = VDDIO)			
WP4	UART_RX	I	Serial Output for UART. Connect to RS-232 DTE for exchanging data with other serial devices. This signal has an internal pull-up resistor (approximately 60K ohms) and can be left unconnected (NC) if not used.
WN4	UART_TX	O	Serial Input for UART. Connect to RS-232 DTE for exchanging data with other serial devices. If not used, it may be left unconnected.
External Coexistence Interface (IO supply = VDDIO)			
WL4	BTCX_FREQ	I	Indicates that the coexistent BT is about to transmit on a restricted channel: internal pull-down.
WK3	BTCX_RF_ACTIVE	I	Indicates that the coexistent BT is active: internal pull-down.
WL3	BTCX_STATUS	I	Indicates the coexistent BT priority status and RX/TX direction.
WP3	BTCX_TXCONF	O	Output permission for the coexistent BT to transmit.
JTAG Interface (IO supply = VDDIO_RF) (for testing only)			
WH6	TMS	I	For normal operation, connect as described in the JTAG specification (IEEE Std 1149.1). Otherwise, if JTAG is not used, these pins can be left unconnected (NC) as they have internal pull-up resistors (approximately 60K ohms).
WK1	TDO	O	
WH5	TDI	I	
WJ3	TCK	I	
WJ4	JTAG_TRST_L	I	
GPIO Interface (IO supply = VDDIO, Programmable Pulls)			
WK8	GPIO_0	I/O	General-purpose interface pins.
WH10	GPIO_1	I/O	
WK9	GPIO_2	I/O	
WJ9	GPIO_3	I/O	
WK10	GPIO_6	I/O	
WJ10	GPIO_7	I/O	
WM4	GPIO_8	I/O	
WF11	GPIO_9	I/O	

Table 6: 138-Ball WLBGA Signal Descriptions (Cont.)

Ball	Signal Name	Type	Description
Miscellaneous Signals			
WL6	WL_REG_ON	I	Used by PMU to enable/disable power the internal regulators. Vih = 1.6V, maximum = 3.6V, internal pull-down 200 Kohm. Analog input pin.
WA10	XTALIN	I	Crystal oscillator input
WC11	XTALOUT	O	Crystal oscillator output
WE10	XTAL_PU	O	Request signal to host to provide reference clock. The BCM4319 asserts this signal when the reference clock (e.g., TCXO) should be enabled. **StateXTAL_PU** XTAL clock neededHIGH XTAL clock not needed60 KΩ internal pull-down Add a external pull-down (100 KΩ) to keep the signal deasserted when the BCM4319 is powered down. IO supply = VDDIO
WF10	EXT_POR_L	I	Low asserting global chip reset: digital input pin. IO supply = VDDIO
Radio and Baseband Power Supplies			
WD1	WRF_VDDPAG_3P3	I	3.3V for the internal power amplifiers
WB1	WRF_VDDPAA_3P3	I	3.3V for the internal power amplifiers
WE6	WRF_VDDVCO_1P2	I	1.2V supply for PLL
WA3	WRF_VDDTX_1P2	I	1.2V supply for radio transmit section
WA5	WRF_VDDRX_1P2	I	1.2V supply for radio receive section
WC9	WRF_VDDPFDCP_1P2	I	1.2V supply for PLL
WC5	WRF_VDDLO_1P2	I	1.2V supply for LO generator
WC8	WRF_VDDD_1P2	I	1.2V supply for PLL
WE8	WRF_VDDCAB_1P2	I	1.2V supply for CAB
WC7	WRF_VDDA_1P2	I	1.2V supply for PLL
WH4	WRF_BBPLL_VDD_1P2	I	1.2V supply for baseband PLL
WG2	WRF_AFE_PAD_AVDD_RXA DC	I	1.2V filtered supply for ADC
WG3	WRF_AFE_PAD_AVDD_AUX	I	1.2V filtered supply for AFE AUX

Table 6: 138-Ball WLBGA Signal Descriptions (Cont.)

Ball	Signal Name	Type	Description
Miscellaneous Power Supplies			
WG9	VDDIO_SD	I	SDIO I/O supply (1.8V to 3.3V)
WG10	VDDIO_SD	I	VDDIO_SD should be supplied externally if the SDIO interface is used. Even if the SDIO interface is not used, VDDIO_SD should not be grounded (instead, the PALDO output can be used for VDDIO_SD. Alternately VDDIO_SD can use the same supply as VDDIO).
WJ2	VDDIO_RF	I	RF I/O supply (2.6V to 3.3V)
WK2	VDDIO_RF	I	VDDIO_RF should be supplied externally (it cannot be supplied from the PALDO) when the RF front-end is shared with other devices, such as Bluetooth. The same external supply should be used for pulls-ups, because PALDO is shutdown during sleep mode and when the BCM4319 is powered down.
WF6	VDDIO	I	Digital I/O supply (1.8V to 3.3V)
WK7	VDDIO	I	VDDIO should be supplied externally
WC10	VDD	I	1.2V digital core supply
WF7	VDD	I	
WK5	VDD	I	
WB11	VDDXO	I	1.2V crystal oscillator filtered power supply
WK6	OTP_VDD33	I	3.3V OTP power supply (no lower than 3.0V)
WL1	USB20PHY_AVDD25_PAD	I	USB Phy analog 2.5V supply
WL2	USB20PHY_AVDD12_PAD	I	USB Phy core 1.2V supply
WM2	USB20PHY_AVDD33_PAD	I	USB Phy analog 3.3V supply
Ground			
WD10	VSS	–	Digital ground
WF5			
WK4			
WM5	AVSS_LDO	–	Ground
WD11	VSSXO	–	Crystal oscillator ground
WN10	SR_PVSS1	–	Ground
WM10	SR_PVSS1	–	Ground
WM8	SR_PAVSS	–	Ground
WM9	SR_AVSS	–	Ground
WA1	WRF_GNDPAA_3P3	–	Ground
WA2	WRF_GNDTX_1P2	–	Ground
WA9	WRF_GNDCAB_1P2	–	Ground
WB5	WRF_GNDRX_1P2	–	Ground
WB8	WRF_GNDD_1P2	–	Ground
WC1	WRF_GNDPAA_3P3	–	Ground
WC2	WRF_GNDPAG_3P3	–	Ground

Table 6: 138-Ball WLBGA Signal Descriptions (Cont.)

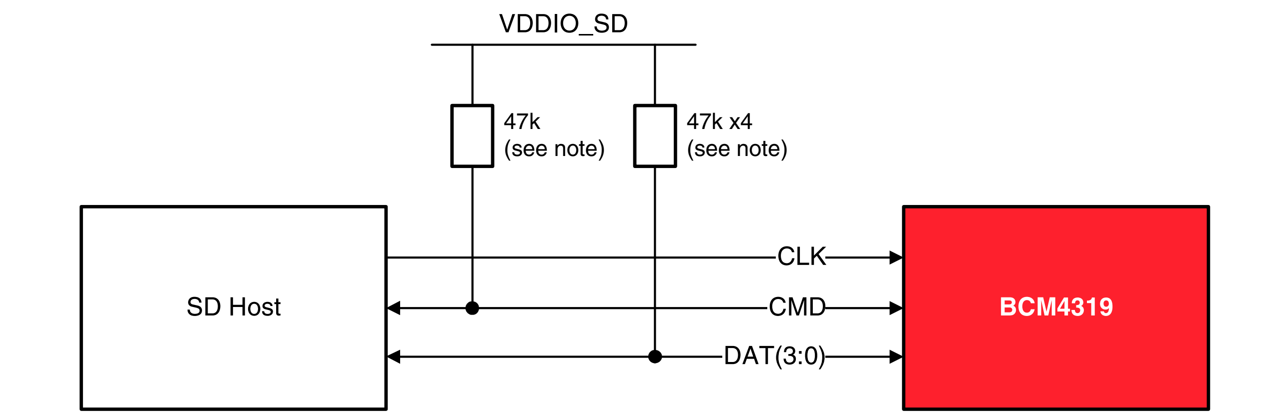
Ball	Signal Name	Type	Description
WD8	WRF_GNDA_1P2	–	Ground
WD9	WRF_GNDPFDCP_1P2	–	Ground
WE2	WRF_GNDPAG_3P3	–	Ground
WE5	WRF_GNDLO_1P2	–	Ground
WE7	WRF_GNDVCO_1P2	–	Ground
WG1	WRF_AFE_PAD_AVSS_RXADC	–	Ground
WG4	WRF_BBPLL_GND_1P2	–	Ground
WL5	BT_REG_ON	–	Ground
WP2	USB20PHY_AGND_PAD	–	Ground
WN2	USB20PHY_GNDPLL_PAD	–	Ground
No Connect			
WE4	WRF_GPIO_OUT2	O	No connect
WF1	WRF_AFE_PAD_TEST_IP	I	No connect
WF2	WRF_AFE_PAD_TEST_IN	I	No connect
WF3	WRF_AFE_PAD_IQADC_VREF	O	No connect
WF4	WRF_GPIO_OUT1	O	No connect
WF9	WRF_EXTREFIN	I	No connect
WH1	WRF_AFE_PAD_TEST_OP	O	No connect
WH2	WRF_AFE_PAD_TEST_ON	O	No connect

SDIO Pin Descriptions

Table 7: SDIO Pin Descriptions

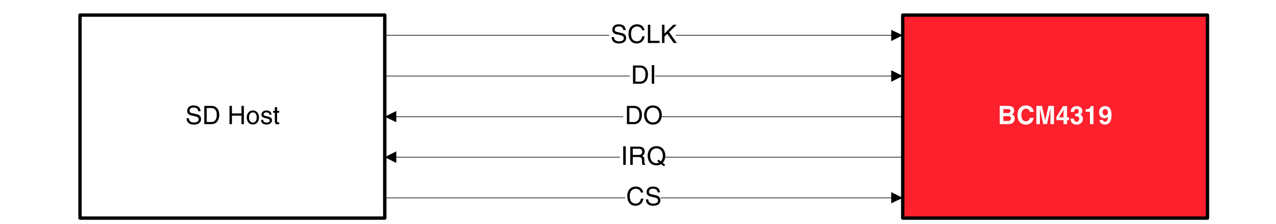
SD 4-Bit Mode		SD 1-Bit Mode		gSPI Mode	
SDIO_DATA_0	Data line 0	DATA	Data line	DO	Data output
SDIO_DATA_1	Data line 1 or interrupt	IRQ	Interrupt	IRQ	Interrupt
SDIO_DATA_2	Data line 2 or read wait	RW	Read wait	NC	Not used
SDIO_DATA_3	Data line 3	N/C	Not used	CS	Card select
SDIO_CLK	Clock	CLK	Clock	SCLK	Clock
SDIO_CMD	Command line	CMD	Command line	DI	Data input

Figure 18: Signal Connections to SDIO Card (SD 4-Bit Mode)



Note: Section 6 of the SDIO physical layer specification specifies that the SDIO host must provide a 10k - 100k ohm pull-up resistor on each CMD and DAT(3:0) signal line. This requirement must be met to properly operate the BCM4319.

Figure 19: Signal Connections to SDIO Card (gSPI Mode)



Strapping Options and GPIO Functions

The pins listed in Table 8 on page 56 are sampled at power-on reset (POR) after WL_REG_ON goes high, to determine the various operating modes. Sampling occurs within 150 milliseconds after WL_REG_ON goes high. After POR each pin assumes the GPIO or alternative function specified in the signal descriptions table. Each pin has an programmable internal pull-up or pull-down resistor that determines the default mode. To change the mode, connect an external pull-up resistor to VDDIO or a pull-down resistor to GND—use a 10 KΩ resistor or less (refer to the reference board schematics for more information).

All GPIOs can be safely used in output mode. GPIOs that do not have interfering strapping options can be safely used as input pins, specifically including:

- USB mode: 1, 2, and 3
- SDIO mode: 1, 2, 3, and 9
- gSPI mode: 2 and 9

Table 8: Strapping Options

Pin Name	Ball #	Default State	Function	Description	
GPIO_0	WK8	Low	Selects Interface modes[a] (depends on strapping). This pin should not be used as a generic input and should not be driven by other devices.	–	USB mode (strapping): • 0: normal (default) • 1: USB CPU-less mode SDIO mode (strapping): • 0: SDIO (default) • 1: gSPI mode
GPIO_1	WH10	Low	GPIO	–	gSPI clock polarity strapping in gSPI mode: do not care in all other modes[b]. Default = 0
GPIO_2	WK9	–	GPIO	–	No strapping functions for this pin
GPIO_3	WJ9	Low	GPIO	–	gSPI clock phase strapping in gSPI mode: do not care in all other modes.
GPIO_6 GPIO_7	WK10 WJ10	Low High	GPIO[7:6]	[7:6] = 00	OTP enabled, use default SDIO CIS
				[7:6] = 01	01 Reserved
				[7:6] = 10	OTP enabled, load SDIO CIS from OTP (default)
				[7:6] = 11	11 Reserved
GPIO_8	WM4	Low	Sets SDIO and USB	0	USB mode (default)
				1	SDIO mode
GPIO_9	WF11	High	Boot mode	–	USB mode: USB normal mode 0: remap to RAM, ARM held in reset after POR (internal use only) 1: boot from ROM, ARM automatically runs after POR (required for USB normal mode) USB CPU-less mode: Do not care, ARM held in reset after POR SDIO/gSPI Mode Do not care, ARM held in reset after POR

a. Typically used as an output for WLAN_HOST_WAKE and as an out-of-band interrupt for the SDIO interface. It has a hardware generated interrupt and is always valid (unlike the SDIO in-band interrupt, which is valid only when data is not driven on the SDIO lines). This out-of-band interrupt mimics the final in-band interrupts so all of the interrupt enables (such as per-function interrupt enables) should be set appropriately.

b. This pin is often used as an input for the out-of-band power control signal WLAN_WAKE.

Section 10: Operating Conditions

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Environmental Ratings

Table 9: Environmental Characteristics

Characteristic	*Value*	*Units*	*Conditions/Comments*
Ambient temperature (T_A)	–30 to +85[a]	°C	Operation
Storage temperature	–40 to +105	°C	–
Relative humidity	Less than 60	%	Storage
	Less than 85	%	Operation
ESD	± 2	kV	Human Body model

a. The BCM4319 supports a functional operating range of –30° to +85° C. However, the optimal RF performance specified in this datasheet is only guaranteed for temperatures from –10° to +55° C.

Absolute Maximum Ratings

These specifications indicate levels where permanent damage to the device can occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 10: Absolute Maximum Ratings

Rating	*Symbol*	*Value*	*Unit*
DC supply voltage for VBAT	VBAT	–0.5 to +6.5	V
DC supply voltage for I/O	VDDO[a]	–0.5 to +4.1	V
DC supply voltage for RF	VDDRF	–0.5 to +1.32	V
DC supply voltage for core	VDDC	–0.5 to +1.32	V
Maximum undershoot voltage for I/O	Vundershoot	–0.5	V
Maximum junction temperature	T_j	125	°C

a. VDDO = VDDIO/VDDIO_SD/VDDIO_RF

Recommended Operating Conditions and DC Characteristics

Table 11: Recommended Operating Conditions and DC Characteristics

Element	Symbol	Value Minimum	Value Typical	Value Maximum	Unit
DC supply voltage for VBAT [a]	–	2.7 [b]	–	5.5[b]	V
DC supply voltage for OTP, USB [a]	–	3.0	3.3	3.63	V
DC supply voltage for PA [a]	–	2.8[c]	3.3	3.63	V
DC supply voltage for I/O[a, d]	VDDO	1.62	3.3 or 1.8	3.63	V
DC supply voltage for core [a]	VDDC	1.176	1.225	1.30	V
1.2V Analog (Radio/AFE/PLL/XTAL/USB 1.2)[a]	–	1.176	1.225	1.30	V
2.5V USB[a]	–	2.25	2.5	2.75	V
Input low voltage (VDDO = 3.3V)[e]	V_{IL}	–	–	0.8	V
Input high voltage (VDDO = 3.3V)[e]	V_{IH}	2.0	–	VDDO	V
Input low voltage (VDDO = 1.8V)[e]	V_{IL}	–	–	0.6	V
Input high voltage (VDDO = 1.8V)[e]	V_{IH}	1.1	–	VDDO	V
Input high voltage (WL_REG_ON pin)	V_{IH}	1.6	–	3.6	V
Output low voltage (IOL = 100 µA)	V_{OL}	–	–	0.2	V
Output high voltage (IOH = –100 µA)	V_{OH}	VDDO – 0.2V	–	–	V
Input low current	I_{IL}	–	0.3	–	µA
Input high current	I_{IH}	–	0.3	–	µA
Output low current (VDDIO/VDDIO_RF)	I_{OL}	–	–	3.0	mA
Output high current (VDDIO/VDDIO_RF)	I_{OH}	–	–	3.0	mA
Output low current (VDDIO_SD)	I_{OL}	–	–	Programmable: 2 to 12 mA (default 10 mA)	mA
Output high current (VDDIO_SD)	I_{OH}	–	–		mA

a. Functional operation is not guaranteed outside these limits, and operation outside these limits for extended periods can adversely affect long-term reliability of the device.
b. The BCM4319 is functional across this range of voltages. However, optimal RF performance specified in the datasheet is only guaranteed while VBAT is between 3.0 and 5.25V.
c. With VBAT = 3.0V PALDO output = 3.0 –0.2 (dropout voltage) = 2.8V
d. The supported voltage range applies to all three I/O supplies: VDDIO, VDDIO_SD, and VDDIO_RF. VDDIO and VDDIO_SD often use 1.8V signaling; however, VDDIO_RF tends to use a higher voltage rail, such as 3.3V, because this supply rail is used for the BCM4319 RF switch and front-end control lines. RF front-end components (such as transmit/receive switches) tend to require higher control voltages.
e. For any other VDDO from 1.8V to 3.3V (±10%), V_{IH} and V_{IL} are specified as V_{IH} = from 0.7 * VDDO to VDDO and V_{IL} = from 0V to 0.2 * VDDO.

Current Consumption

Table 12: Current Consumption

		VBAT=3.6V, VDDIO = 3.3V , 25°C	
Operational State		***SDIO Typical***	***USB Typical***
OFF (WL_REG_ON = Low)[a]		16 uA	450 uA[b]
Sleep		180 uA	41 mA[c]
Idle between beacons		180 uA	41 mA[c]
IEEE PS @ DTIM = 100 ms[d]		1.25 mA	43 mA[c]
IEEE PS @ DTIM = 300 ms[d]		550 uA	42 mA[c]
Beacon reception		71 mA	103 mA
Rx listen		65 mA	97 mA
Rx 1 Mbps		71 mA	103 mA
Rx 11 Mbps		71 mA	103 mA
Rx 6 Mbps		72 mA	103 mA
Rx 54 Mbps		76 mA	107 mA
Rx MCS0 20 MHz channel		72 mA	103 mA
Rx MCS7 20 MHz channel		77 mA	108 mA
Rx Listen 40 MHz channel		77 mA	108 mA
Rx MCS0 40 MHz channel		82 mA	113 mA
Rx MCS7 40 MHz channel		87 mA	118 mA
Tx Rate	***Tx Power at ChipOut[e]***	–	–
Tx CCK	20 dBm	320 mA	355 mA
Tx OFDM BPSK	19 dBm	305 mA	340 mA
Tx OFDM QPSK	19 dBm	305 mA	340 mA
Tx OFDM 16 QAM	18 dBm	290 mA	325 mA
Tx OFDM 64 QAM	18 dBm	290 mA	325 mA
Tx MCS0 20 MHz channel	16 dBm	275 mA	310 mA
Tx MCS7 20 MHz channel	16 dBm	270 mA	305 mA
Tx MCS0 40 MHz channel	16 dBm	290 mA	325 mA
Tx MCS7 40 MHz channel	16 dBm	285 mA	320 mA

a. All measurements include VDDIO current. Depending on factors such as the power topology, external PU/PD resistors, etc., additional leakage current may occur at the board level.
b. Assumes VBAT is directly used for USB 3.3V supply
c. USB interface remains in active mode
d. Beacon Interval = 102.4 ms, DTIM = 1 or 3, Beacon duration = 1 ms @ 1 Mbps = 192 µs PHY header + 808 us (101 byte) MPDU
e. Chip Tx output power is based on Broadcom reference board measurements and backward calculation from antenna test port.

Section 11: WLAN RF Specifications

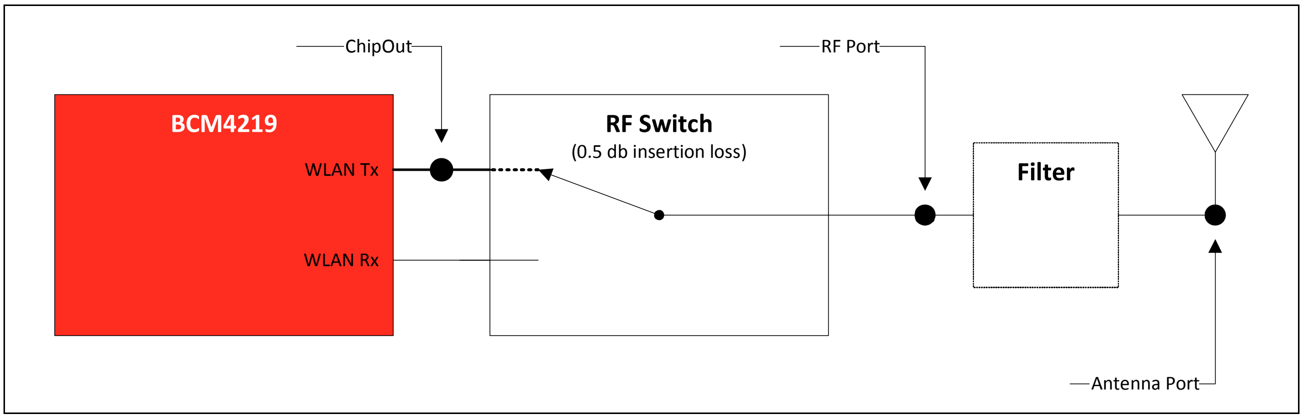
Introduction

The BCM4319 includes an integrated dual-band direct conversion radio that supports either the 2.4 GHz IEEE 802.11g band or the 5 GHz IEEE 802.11a band. The BCM4319 does not provide simultaneous 2.4 GHz and 5 GHz operation. This section describes the RF characteristics of the 2.4 GHz and 5 GHz sections of the radio.

Note: Unless otherwise stated, these specifications apply over the range of operating conditions specified in Table 9, and Table 10 on page 57, and Table 11 on page 58. Outside these limits, functional operation is not guaranteed.

Typical values apply for VBAT = 3.6V and ambient temperature = 25°C.

Figure 20: RF Port Location



2.4 GHz Band General RF Specifications

Table 13: 2.4 GHz Band General RF Specifications

Item	*Condition*	*Minimum*	*Typical*	*Maximum*	*Unit*
Tx/Rx switch time	Including TX ramp down	–	5	10	µs
Rx/Tx switch time	Including TX ramp up	–	5	5	µs
Power Up / Down Ramp Time	DSSS/CCK modulations	–	–	< 2	µs

2.4 GHz Band Receiver RF Specifications

Table 14: 2.4 GHz Band Receiver RF Specifications

Parameter	***Condition/Notes***	***Min***	***Typ***[a]	***Max***	***Unit***
Out-of-band blocking performance. The blocking level at the WLAN RF port for 1 dB Rx sensitivity degradation (without external filtering)	776–794 MHz (CDMA2000)	–8 dbm	–	–	dBm
	824–849 MHz (cdmaOne)	–24.5	–	–	dBm
	824–849 MHz (GSM850)[b]	–16.5	–	–	dBm
	880–915 MHz (E-GSM)	–2	–	–	dBm
	1710–1785 MHz (GSM1800)	–17	–	–	dBm
	1850–1910 MHz (GSM1800)	–21	–	–	dBm
	1850–1910 MHz (cdmaOne)	–32	–	–	dBm
	1850–1910 MHz (WCDMA)	–29	–	–	dBm
	1920–1980 MHz (WCDMA)	–32	–	–	dBm
RX sensitivity (8% PER for 1024 octet PSDU) at WLAN RF port[c]	1 Mbps DSSS	–94	–97	–	dBm
	2 Mbps DSSS	–91	–94	–	dBm
	5.5 Mbps DSSS	–90	–92	–	dBm
	11 Mbps DSSS	–88	–90	–	dBm
RX sensitivity (10% PER for 1024 octet PSDU) at WLAN RF port[a]	6 Mbps OFDM	–89.5	–91.5	–	dBm
	9 Mbps OFDM	–89	–90.5	–	dBm
	12 Mbps OFDM	–88	–90	–	dBm
	18 Mbps OFDM	–86	–88	–	dBm
	24 Mbps OFDM	–84	–86	–	dBm
	36 Mbps OFDM	–80	–82	–	dBm
	48 Mbps OFDM	–76	–78	–	dBm
	54 Mbps OFDM	–74	–76	–	dBm

Table 14: 2.4 GHz Band Receiver RF Specifications (Cont.)

Parameter	***Condition/Notes***		***Min***	***Typ[a]***	***Max***	***Unit***
RX sensitivity (10% PER for 4096 octet PSDU) at WLAN RF port[a,d]. Defined for default parameters: GF, 800 ns GI, and non-STBC.	20 MHz channel spacing for all MCS rates					
	MCS 7		–71	–73	–	dBm
	MCS 6		–72.5	–74.5	–	dBm
	MCS 5		–74.5	–76.5	–	dBm
	MCS 4		–78.5	–80.5	–	dBm
	MCS 3		–82	–84	–	dBm
	MCS 2		–84.5	–86.5	–	dBm
	MCS 1		–86.5	–88.5	–	dBm
	MCS 0		–88	–90	–	dBm
	40 MHz channel spacing for all MCS rates					
	MCS 7		–67.5	–69.5	–	dBm
	MCS 6		–69.0	–71.0	–	dBm
	MCS 5		–70.5	–72.5	–	dBm
	MCS 4		–74.5	–76.5	–	dBm
	MCS 3		–77.0	–79.0	–	dBm
	MCS 2		–80.0	–82.0	–	dBm
	MCS 1		–82.5	–84.5	–	dBm
	MCS 0		–85.0	–87.0	–	dBm
In-band static CW jammer immunity (fc – 8 MHz < fcw + 8 MHz)	Rx PER < 1%, 54 Mbps OFDM, 1000 octet PSDU for: (RxSens + 23 dB < Rxlevel < max input level)		–80	–	–	dBm
Maximum Receive Level @ 2.4 GHz	@ 1, 2 Mbps (8% PER, 1024 octets)		–3.5	–	–	dBm
	@ 5.5, 11 Mbps (8% PER, 1024 octets)		–9.5	–	–	dBm
	@ 6–54 Mbps (10% PER, 1024 octets)		–9.5	–	–	dBm
	@ MCS0–7 rates (10% PER, 4095 octets)		–9.5	–	–	dBm
Adjacent channel rejection-DSSS (Difference between interfering and desired signal at 8% PER for 1024 octet PSDU with desired signal level as specified in Condition/Notes)	***Desired and interfering signal 30 MHz apart***					
	1 Mbps DSSS	–74 dBm	35	–	–	dB
	2 Mbps DSSS	–74 dBm	35	–	–	dB
	Desired and interfering signal 25 MHz apart					
	5.5 Mbps DSSS	–70 dBm	35	–	–	dB
	11 Mbps DSSS	–70 dBm	35	–	–	dB

Table 14: 2.4 GHz Band Receiver RF Specifications (Cont.)

Parameter	Condition/Notes		Min	Typ[a]	Max	Unit
Adjacent channel rejection-OFDM (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 1024 octet PSDU with desired signal level as specified in Condition/Notes)	6 Mbps OFDM	–79 dBm	16	–	–	dB
	9 Mbps OFDM	–78 dBm	15	–	–	dB
	12 Mbps OFDM	–76 dBm	13	–	–	dB
	18 Mbps OFDM	–74 dBm	11	–	–	dB
	24 Mbps OFDM	–71 dBm	8	–	–	dB
	36 Mbps OFDM	–67 dBm	4	–	–	dB
	48 Mbps OFDM	–63 dBm	0	–	–	dB
	54 Mbps OFDM	–62 dBm	–1	–	–	dB
Adjacent channel rejection MCS0–7 (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 4096 octet PSDU with desired signal level as specified in Condition/Notes)	MCS7	–61 dBm	–2	–	–	dB
	MCS6	–62 dBm	–1	–	–	dB
	MCS5	–63 dBm	0	–	–	dB
	MCS4	–67 dBm	4	–	–	dB
	MCS3	–71 dBm	8	–	–	dB
	MCS2	–74 dBm	11	–	–	dB
	MCS1	–76 dBm	13	–	–	dB
	MCS0	–79 dBm	16	–	–	dB
Maximum receiver gain	–	–	–	105	–	dB
Gain control step	–	–	–	3	–	dB
RSSI accuracy[e]	Range –98 dBm to –30 dBm		–5	–	5	dB
	Range above –30 dBm		–8	–	8	dB

a. Values are measured at the input of the BCM4319. Thus, they include insertion losses from the integrated baluns, but exclude losses from the external circuits.

b. The blocking levels are valid for channels 1 through 11. (For higher channels, the performance may be lower due to third harmonic signals (3 × 824 MHz) falling within band.)

c. Derate by 1.5 dB for –30 °C to –10°C and 55°C to 85°C.

d. Sensitivity degradations for alternate settings in MCS modes. MM: 0.5 dB drop, SGI: 2 dB drop, and STBC: 0.75 dB drop.

e. The minimum and maximum values shown have 95% confidence

2.4 GHz Band Transmitter RF Specifications

Table 15: 2.4 GHz Band Transmitter RF Specifications

Characteristic	*Condition*	*Min*	*Typ*	*Max*	*Unit*
RF output frequency range	–	2400	–	2500	MHz
Tx power at ChipOut for highest power level setting at 25°C, VBAT = 3.6V and spectral mask and EVM compliance[a] [b]	CCK	18.5	20	21.5	dBm
	OFDM BPSK	17.5	19	20.5	dBm
	OFDM QPSK	17.5	19	20.5	dBm
	OFDM 16 QAM	16.5	18	19.5	dBm
	OFDM 64 QAM	16.5	18	19.5	dBm
	MCS0 to MCS7 20 MHz channels	14.5	16	17.5	dBm
	MCS0 to MCS7 40 Mhz channels	14.5	16	17.5	dBm
Gain flatness	Maximum gain	–	–	2	dB
Output IP3	Maximum gain	–	37	–	dBm
Output P1dB	–	–	27	–	dBm
Carrier suppression	–	15	–	–	dBr
CCK Tx spectrum mask @ max gain	fc – 22 MHz < f < fc – 11 MHz	–	–	–30	dBr
	fc + 11 MHz < f< fc + 22 MHz	–	–	–30	dBr
	f < fc – 22 MHz; and f > fc + 22 MHz	–	–	–50	dBr
OFDM Tx spectrum mask (chip output power = 16 dBm)	f < fc – 11 MHz and f > fc + 11 MHz	–	–	–26	dBc
	f < fc – 20 MHz and f > fc + 20 MHz	–	–	–35	dBr
	f < fc – 30 MHz and f > fc + 30 MHz	–	–	–40	dBr
Tx modulation accuracy (i.e. EVM) at maximum gain	IEEE 802.11b mode	–	–	35%	–
	IEEE 802.11g mode QAM64 54 Mbps	–	–	5%	–
Gain control step size	–	–	0.25 dB	–	dB/step
Amplitude balance[c]	DC input	–1	–	1	dB
Phase balance[a]	DC input	–1.5	–	1.5	°
Baseband differential input voltage	Shaped pulse	–	0.6	–	Vpp
Tx power ramp up	90% of final power	–	–	2	µsec
Tx power ramp down	10% of final power	–	–	2	µsec
Tx power control dynamic range	–	10	–	–	dB
Closed-loop Tx power variation	Across full temperature and voltage range. Power accuracy of ±1.5 dB for 10–20 dBm and ±3 dB for 5–10 dBm.	–	–	±1.5	dB
Carrier suppression	–	15	–	–	dBc
Gain control step	–	–	.25	–	dB
See next page for additional footnotes.					

a. Derate by 1.5 dB for –30°C to –10°C, and 55°C to 85°C.

b. Powers shown are at ChipOut. Measurements taken at the antenna port are lower due to insertion losses of the external RF front end, including any RF switches or filters. Front end insertion losses are system-design dependent.
The WLAN driver power-control algorithm keeps the output power within +/- 1.5 dB of the values specified in NVRAM.
Output power can vary, depending on target output power and modulation offset settings in the NVRAM file.
Values shown assume the following NVRAM variable settings:
pa0maxpwr = 82
cckpo = 0
ofdmpo = 0x44442222
mcs2gpo0 = 0x8888
mcs2gpo1 = 0x8888
mcs2gpo4 = 0x8888
mcs2gpo5 = 0x8888
In this case an insertion loss of 1 dB is assumed between the output and the antenna port.

c. At 3 MHz offset from the carrier frequency.

2.4 GHz Band Local Oscillator Specifications

Table 16: 2.4 GHz Band Local Oscillator Specifications

Characteristic	*Condition*	*Minimum*	*Typical*	*Maximum*	*Unit*
VCO frequency range	–	2412	–	2484	MHz
Reference input frequency range	–	–	Various[a]	–	MHz
Reference spurs	–	–	–	–34	dBc
Local oscillator phase noise, single-sided from 1–300 kHz offset	–	–	–	–86.5	dBc/Hz
Clock frequency tolerance	–	–	–	±20	ppm

a. Reference supported frequencies range from 12 MHz to 52 MHz.

5 GHz Band RF Receiver Specifications

Table 17: 5 GHz Band Receiver RF Specifications[a]

Characteristic	*Condition*	*Minimum*	*Typical*	*Maximum*	*Unit*
Cascaded noise figure	Maximum RX gain	–	4.5	–	dB
Maximum receive level[a]	5.24 GHz @ 6 Mbps	–10	–	–	dBm
	5.24 GHz @ 54 Mbps	–15	–	–	dBm
DC rejection servo loop bandwidth (normal operation)	Wideband mode	–	500	–	kHz
	Narrowband mode	120 Hz	–	230	kHz
Adjacent channel power rejection	At 20-MHz offset	–	TBD	–	dBc
Alternate channel power rejection	At 40-MHz offset	–	TBD	–	dBc
Minimum RX gain	–	–	15	–	dB
Maximum RX gain	–	–	>100	–	dB
IQ amplitude balance	–	–	0.5	–	dB
IQ phase balance	–	–	1.5	–	°
Out-of-Band Blocking Performance without RF Band-Pass Filter (–1 dB desensitization):					
CW	30–4300 MHz	–10	–	–	dBm
CW	4300–4800 MHz	–25	–	–	dBm
CW	5900–6400 MHz	–25	–	–	dBm

a. With minimum RF gain.

Table 18: 5 GHz Receiver Sensitivity

Parameter	*Condition/Notes*	*Minimum*	*Typical*	*Maximum*	*Unit*
Frequency range	–	4900	–	5845	MHz
RX sensitivity (10% PER for 1000 octet PSDU) at External LNA Input	6 Mbps OFDM	–87.5	–89	–	dBm
	9 Mbps OFDM	–86.5	–88	–	dBm
	12 Mbps OFDM	–86.5	–88	–	dBm
	18 Mbps OFDM	–85.5	–87	–	dBm
	24 Mbps OFDM	–82.5	–84	–	dBm
	36 Mbps OFDM	–79.5	–81	–	dBm
	48 Mbps OFDM	–73.5	–75	–	dBm
	54 Mbps OFDM	–71.5	–73	–	dBm
RX sensitivity (10% PER for 4096 octet PSDU) at external LNA input[a, b]	HT mode MCS 7 (64 QAM, R = 5/6, 20 MHz channel spacing)	–69.5	–71	–	dBm

a. Contact Broadcom for details on recommended LNAs.
b. Derate by 1.5 dB for -30 °C to -10°C and 55°C to 85°C.

5 GHz Band RF Transmitter Specifications

Table 19: 5 GHz Band Transmitter RF Specifications

Characteristic	*Condition*	*Minimum*	*Typical*	*Maximum*	*Unit*
RF output frequency range	–	4920	–	5805	MHz
Gain flatness	Maximum gain	–	–	1	dB
Output IP3	Maximum gain	–	35	–	dBm
Output P1dB	Maximum gain	–	25	–	dBm
Output power (EVM compliant)	–	–	–	TBD	dBm
Carrier suppression	–	–15	–	–	dBr
OFDM TX spectrum mask (chip output power = 16 dBm)	f < fc – 11 MHz and f > fc + 11 MHz	–	–	–26	dBc
	f < fc – 20 MHz and f > fc + 20 MHz	–	–	–35	dBr
	f < fc – 30 MHz and f > fc + 30 MHz	–	–	–40	dBr
Gain control step size	–	–	0.25	–	dB/ step
I/Q baseband 3-dB bandwidth	–	–	12	–	MHz
Amplitude balance	DC Input	–0.5	–	0.5	dB
Phase balance	DC Input	–1.5	–	1.5	°
Baseband differential input voltage	–	–	0.7	–	Vpp
TX power ramp up	90% of final power	–	–	2	µsec
TX power ramp down	10% of final power	–	–	2	µsec

5 GHz Band Local Oscillator Frequency Generator Specifications

Table 20: 5 GHz Band Local Oscillator Frequency Generator Specifications

Characteristic	*Condition*	*Minimum*	*Typical*	*Maximum*	*Unit*
VCO frequency range	–	4920	–	5805	MHz
Reference input frequency range	–	–	various[a]	–	MHz
Reference spurs	–	–	–	–30	dBc
Local oscillator integrated phase noise (1–300 kHz)	4.920–5.700 GHz	–	0.7	–	°
	5.725–5.805 GHz	–	1.4	–	
Clock frequency tolerance	–	–	–	±20	ppm

a. Reference supported frequencies range from 13 MHz to 52 MHz.

Section 12: Internal Regulator Electrical Specifications

Caution! Functional operation outside the limits specified in this section is not guaranteed. In addition, operating the device under such conditions for an extended period of time can adversely affect the long-term reliability of the device.

Core Buck Regulator (CBuck)

Table 21: Core Buck Regulator (CBUCK)

Specification	Notes	Minimum	Typical	Maximum	Units
Input supply voltage	–	2.7	–	5.5	V
PWM mode switching frequency	–	2.24	2.8	3.36	MHz
PWM output current	–	–	–	300	mA
Output voltage range	Programmable, 25 mV steps	1.0	1.45	1.75	V
Output voltage accuracy	–	–5	–	5	%
PWM ripple voltage, static load	–	–	7	20	mVpp
PWM ripple voltage, dynamic load	200 mA, 1 µs rise/fall current step	–	70	100	mV
Burst mode ripple voltage, static	<30 mA load current	–	–	80	mVpp
PWM mode efficiency	200 mA load current	80	90	–	%
Burst mode efficiency	10 mA load current	70	80	–	%
Low Power mode efficiency	200 µA load current	–	60	–	%
	5 mA load current	–	75	–	
Quiescent current	Burst mode	–	30	–	µA
	Low-Power mode	–	20	–	
	Power-down	–	1	–	
Output current limit	–	–	600	–	mA
Output capacitor	Must be X5R, rated at ≥6.3V	3.76	4.7	5.64	µF
Output inductor	See reference schematics and application notes for recommended inductor types.	2.64	3.3	3.96	µH
Start-up time from power-down	–	–	500	1000	µs
Settling time: LPOM to burst	Ensure load current < 5 mA during mode change.	–	–	200	µs
Settling time: Burst To PWM mode	Ensure load current < 30 mA during mode change.	–	–	400	µs

PALDO

Table 22: Internal PALDO[a]

Specification	Notes	Minimum	Typical	Maximum	Units
Input supply voltage	–	2.7	–	5.5	V
Output current	–	–	–	400	mA
Output voltage range [b]	Programmable, 100 mV steps	2.7	3.3	4.0	V
Output voltage accuracy	–	–5	–	5	%
Quiescent current	No load	–	40	–	µA
	Maximum load	–	8	–	mA
Output noise	@30 kHz, 100 mA	–	–	500	$nV/\sqrt{Hz}$
Output capacitor (ESR: 30m–200 mΩ)	–	–	3.3	–	µF
Output current limit	–	–	700	–	mA
Dropout voltage	400 mA load	–	–	200	mV
Start-up time from power-down	–	–	30	60	µs
Settling time for voltage step change [c]	2.5 to 3.3V(10–90%)	–	20	–	µs

a. PALDO has programmable overvoltage protection that can be set to 3.6V or 4.4V: default is enabled.
b. For PSRR performance, the input supply should be at least 200 mV higher than the output.
c. Settling time for ΔV high to low voltage change will depend on load current: Tset ~ Cout.ΔV / Iload.

2.5V LDO (LDO2p5V)

Table 23: 2.5V LDO (LDO2p5V)

Specification	Notes	Minimum	Typical	Maximum	Units
Input supply voltage	–	2.7	–	5.5	V
Output current	–	–	–	50	mA
Output voltage	–	2.25	2.5	2.75	V
Quiescent current	No load	–	6	–	µA
	Max load	–	1.5	–	mA
Output capacitor (ESR: 30 mΩ–200 mΩ)	–	0.7	1	5	µF
Start-up time from power-down	–	–	500	1000	µs

CLDO

Table 24: CLDO

Specification	*Notes*	*Minimum*	*Typical*	*Maximum*	*Units*
Input supply voltage	–	1.35	1.4	2.0	V
Output voltage	Programmable in 25 mV steps	1.10	1.225	1.35	V
Absolute accuracy	–	–	–	±4	%
Output current	–	–	–	200	mA
LDO quiescent current	–	–	10	15	µA
Leakage current through output transistor	CLDO_pu = 0	–	0.1	10	µA
Output noise	@30 kHz, 200-mA load	–	80	–	$nV/\sqrt{Hz}$
Power supply rejection (PSR)	@1 kHz, 150-mV dropout	–	40	–	dB
Output capacitor	Output Capacitor (ESR: 30m–200 mΩ)	–	4.7	–	µF
Dropout voltage	–	150	–	–	mV
Start-up time	–	–	–	0.5	ms

LNLDO1, LNLDO2

Table 25: LNLDO1[a], LNLDO2

Specification	Notes	Minimum	Typical	Maximum	Units
Input supply voltage	LNLDOi_vo_sel = 0	1.35	1.4	2.0	V
	LNLDOi_vo_sel = 1	3.0	3.3	3.6	
Output voltage	LNLDOi_vo_sel = 0	1.10	1.225	1.35	V
	LNLDOi_vo_sel = 1	2.5	2.5	3.1	
Absolute accuracy	–	–	–	±4	%
Output current for LNLDO1	–	–	–	150	mA
Output current for LNLDO2	–	–	–	50	mA
Quiescent current for LNLDO1	LNLDOi_vo_sel = 0	–	31	44	µA
	LNLDOi_vo_sel = 1	–	110	206	
Quiescent current for LNLDO2, 3, 4	LNLDOi_vo_sel = 0	–	29	42	µA
	LNLDOi_vo_sel = 1	–	108	202	
Leakage current for LNLDO1	LNLDO1_pu = 0	–	–	–	µA
	LNLDOi_vo_sel = 0	–	0.1	5	
	LNLDOi_vo_sel = 1	–	0.1	9	
Leakage current for LNLDO2, 3, 4	LNLDO1_pu = 0	–	–	–	µA
	LNLDOi_vo_sel = 0	–	0.1	2	
	LNLDOi_vo_sel = 1	–	0.1	4	
Output noise @30 kHz, 50 mA load	LNLDOi_vo_sel = 0	–	20	–	$nV/\sqrt{Hz}$
	LNLDOi_vo_sel = 1	–	31	–	
PSR for LNLDO	@1 kHz, 150 mV dropout	–	50	–	dB
Dropout voltage	–	150	–	–	mV
Start-up time	–	–	–	0.5	ms

a. LNLDO1 is only used with LNLDOi_vo_sel=0 (1.225V output) to supply sensitive analog blocks: LNLDO2s use is not required or recommended.

Table 26: Power Management Unit

Specification	Notes	Min	Typ	Max	Units
Total Quiescent Current from VBAT	Burst Mode	–	100[a]	–	uA
	Low Power Burst Mode	–	50[a]	–	uA
	Power Down	–	11	–	uA
Input Supply Voltage Ramp-up Time	0 to 4.3V	44	–	–	uS
	4.3 to 5.5V	100	–	–	uS

a. Assumes CBUCK load current = 0 uA, with PALDO, CLDO, and LNLDOs powered down.

Section 13: Power-Up Sequence

SDIO Host Timing Requirement

The SDIO host must wait a minimum of 150 ms after the VDDC (1.25V DC supply for core) ramps up and settles before initiating access to the BCM4319. For typical designs, one of the BCM4319 internal regulators generates VDDC: the regulators are enabled by WL_REG_ON going HIGH.

Reset and Regulator Control Signal Sequencing

The BCM4319 has two control signals that allow the host to control power consumption by enabling or disabling the WLAN and internal regulator blocks. These control signals are as follows:

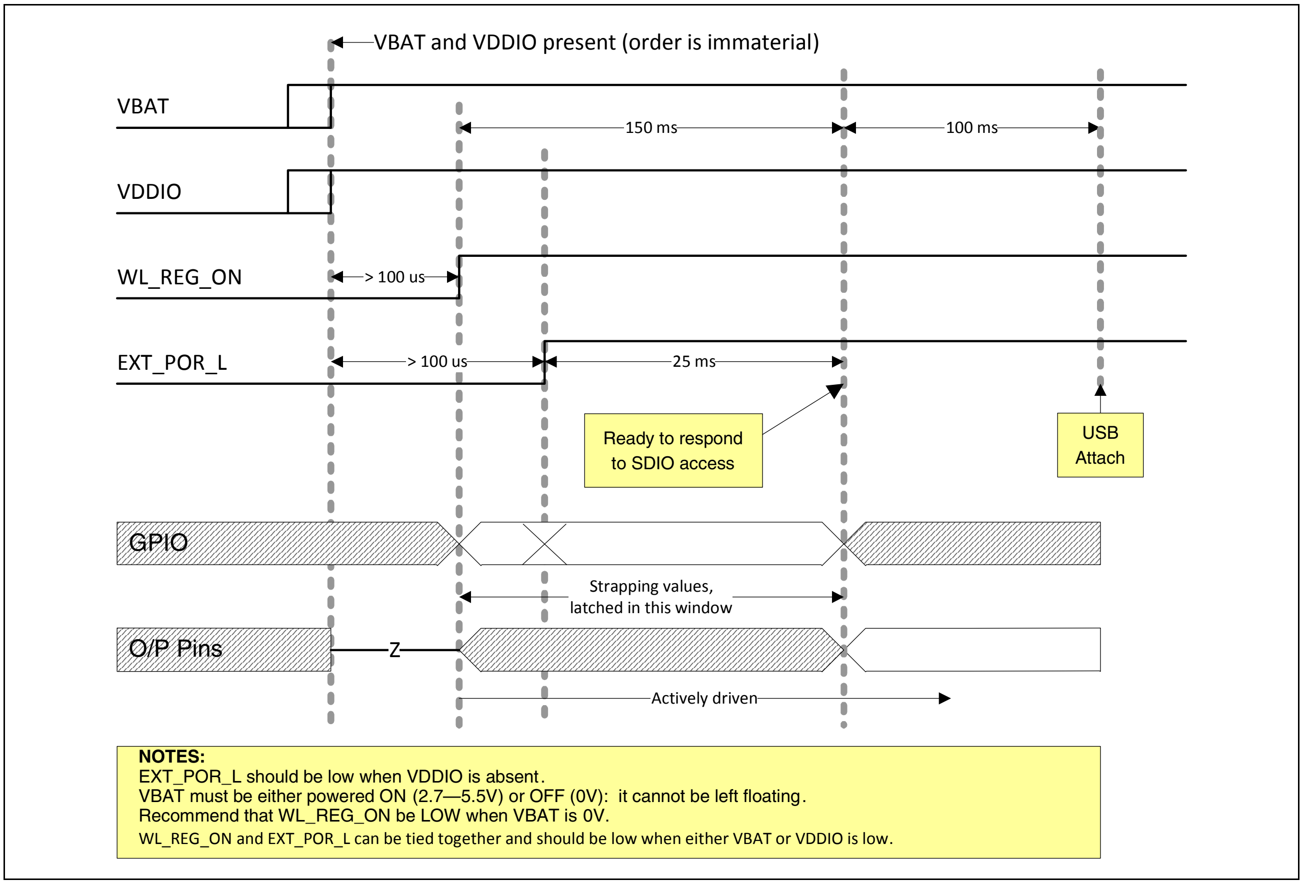
- WL_REG_ON: Can be used by a host CPU to power-up or power down the internal BCM4319 regulators.
- EXT_POR_L: Low asserting reset for the WLAN core. This pin needs to be driven high or low; it must not be left floating. If EXT_POR_L is low, the BCM4319 core will be powered off.

WL_REG_ON and EXT_POR_L can be tied together.

The timing diagram shown in Figure 21 on page 73 is provided to indicate proper sequencing of the signals for WLAN operation. The timing values indicated are minimum required values; longer delays are also acceptable.

Note: The timing diagram is not to scale and is only for illustration purposes.

Figure 21: Power-Up Sequence Timing Diagram



Section 14: Interface Timing Specifications

This section describes the interface timing for gSPI, SDIO (default), and SDIO high-speed modes.

gSPI Timing

The gSPI host and device always use the rising edge of the clock to sample data.

Figure 22: gSPI Timing

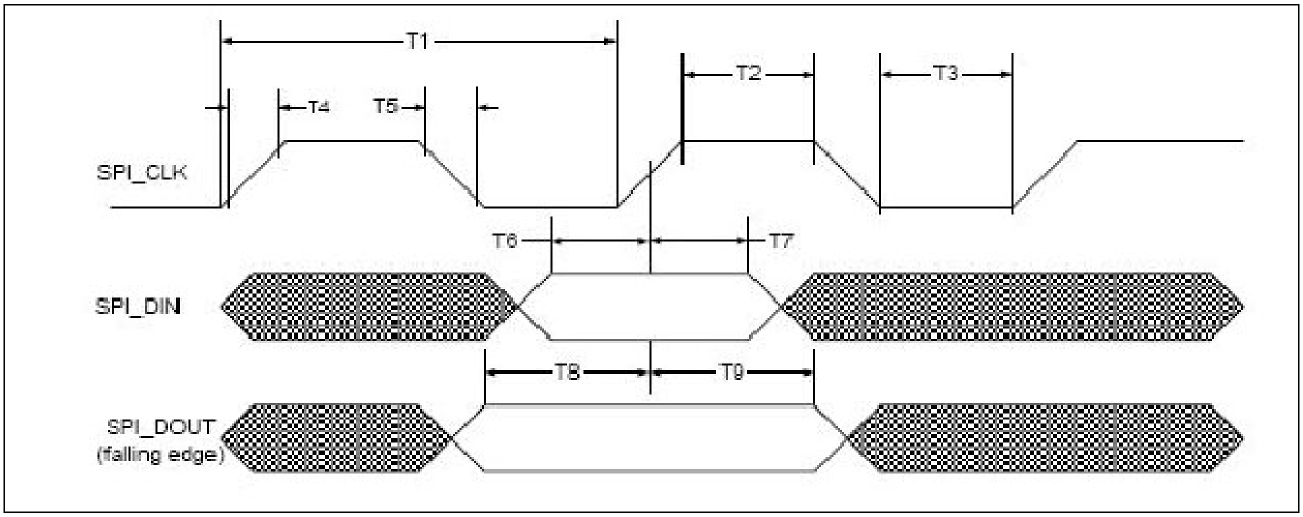


Table 27: gSPI Timing

Parameter	*Symbol*	*Minimum*	*Maximum*	*Units*	*Note*
Clock period	T1	20.8	–	ns	F_{max} = 48 MHz
Clock high/low	T2/T3	(0.45 × T1) – T4	(0.55 × T1) – T4	ns	–
Clock rise/fall time	T4/T5	–	2.5	ns	–
Input setup time	T6	5.0	–	ns	Setup time, SIMO valid to SPI_CLK active edge
Input hold time	T7	5.0	–	ns	Hold time, SPI_CLK active edge to SIMO invalid
Output setup time	T8	5.0	–	ns	Setup time, SOMI valid before SPI_CLK rising
Output hold time	T9	5.0	–	ns	Hold time, SPI_CLK active edge to SOMI invalid
CSX to clock[a]	–	7.86	–	ns	CSX fall to 1st rising edge

Table 27: gSPI Timing

Parameter	***Symbol***	***Minimum***	***Maximum***	***Units***	***Note***
Clock to CSX[a]	–	–	–	ns	Last falling edge to CSX high

a. SPI_CSx remains active for entire duration of SPI read/write/write_read transaction (i.e., overall words for multiple word transaction).

SDIO Default Mode Timing

SDIO default mode timing is shown by the combination of Figure 23 and Table 28 on page 75.

Figure 23: SDIO Bus Timing (Default Mode)

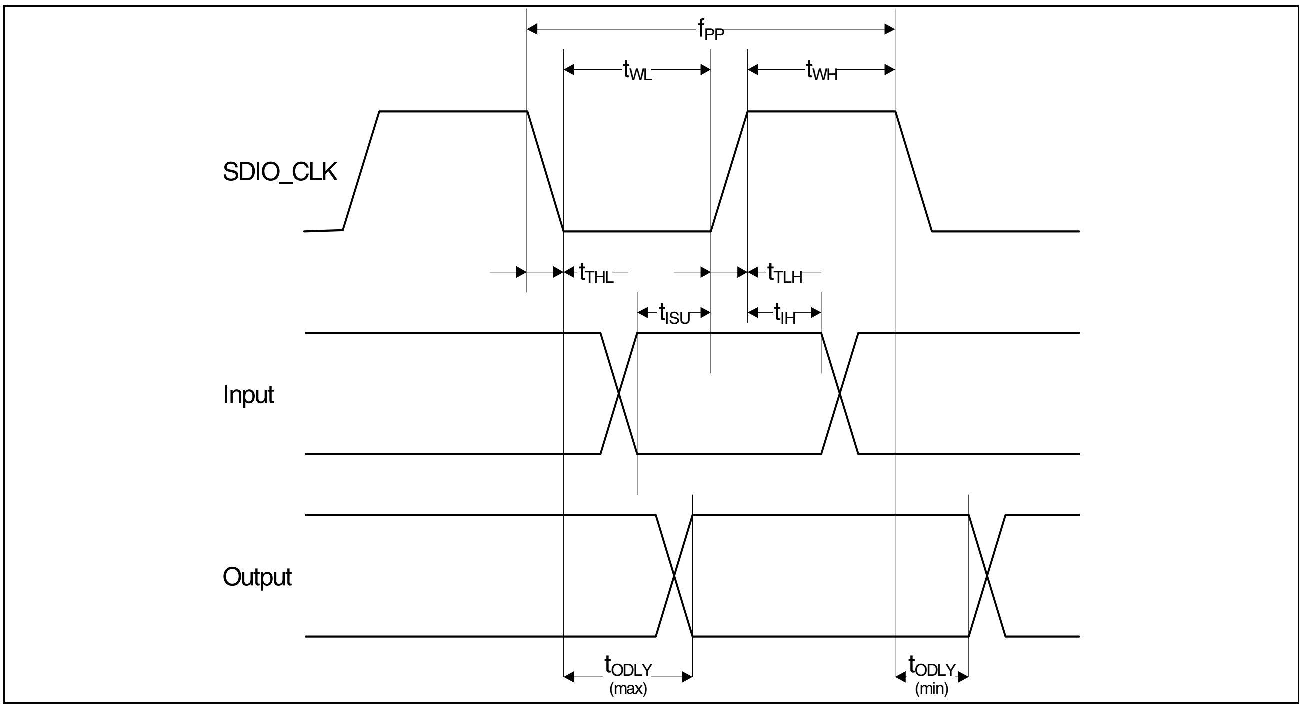


Table 28: SDIO Bus Timing [a] Parameters (Default Mode)

Parameter	***Symbol***	***Minimum***	***Typical***	***Maximum***	***Unit***
SDIO CLK (All values are referred to minimum VIH and maximum VIL[b])					
Frequency – Data Transfer mode	fPP	0	–	25	MHz
Frequency – Identification mode	fOD	0	–	400	kHz
Clock low time	tWL	10	–	–	ns
Clock high time	tWH	10	–	–	ns
Clock rise time	tTLH	–	–	10	ns
Clock low time	tTHL	–	–	10	ns

Table 28: SDIO Bus Timing [a] Parameters (Default Mode) (Cont.)

Parameter	***Symbol***	***Minimum***	***Typical***	***Maximum***	***Unit***
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	5	–	–	ns
Input hold time	tIH	5	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	0	–	14	ns
Output delay time – Identification mode	tODLY	0	–	50	ns

a. Timing is based on CL ≤ 40pF load on CMD and Data.
b. min(Vih) = 0.7 × VDDIO_SD and max(Vil) = 0.2 × VDDIO_SD.

SDIO High Speed Mode Timing

SDIO high speed mode timing is shown by the combination of Figure 24 and Table 29.

Figure 24: SDIO Bus Timing (High-Speed Mode)

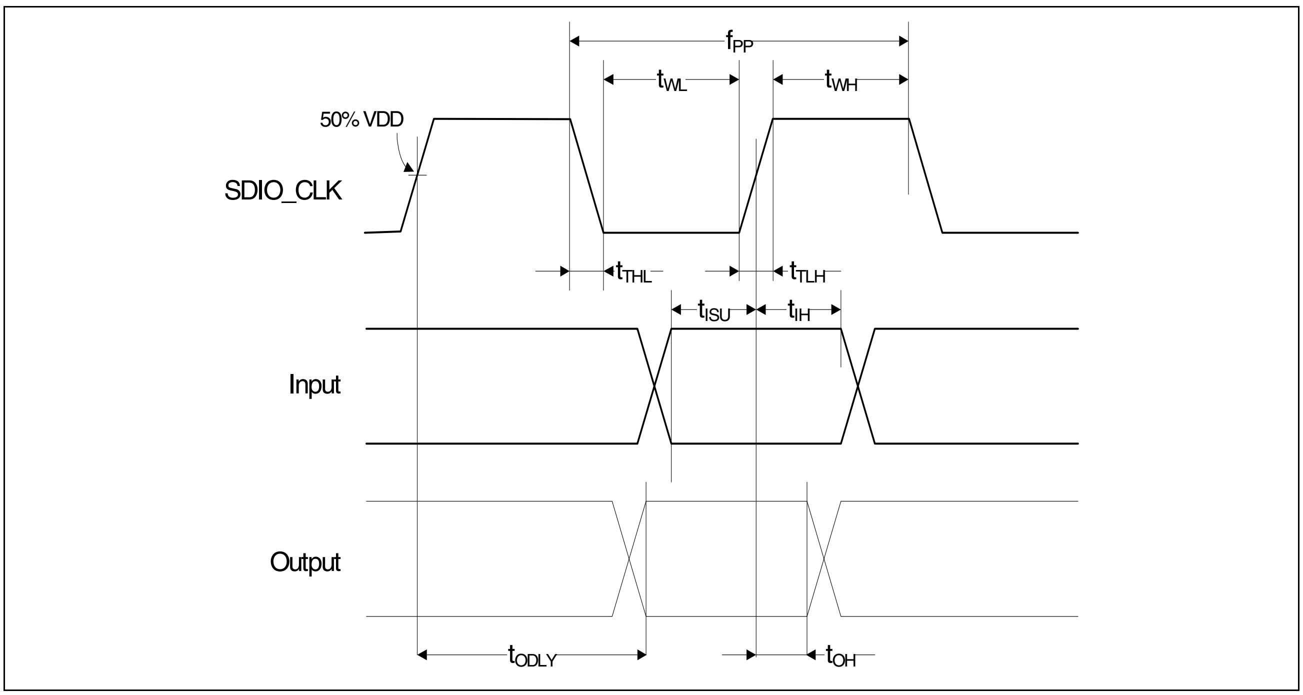


Table 29: SDIO Bus Timing [a] Parameters (High-Speed Mode)

Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Unit*
SDIO CLK (all values are referred to minimum VIH and maximum VIL[b])					
Frequency – Data Transfer Mode	fPP	0	–	50	MHz
Frequency – Identification Mode	fOD	0	–	400	kHz
Clock low time	tWL	7	–	–	ns
Clock high time	tWH	7	–	–	ns
Clock rise time	tTLH	–	–	3	ns
Clock low time	tTHL	–	–	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup Time	tISU	6	–	–	ns
Input hold Time	tIH	2	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer Mode	tODLY	–	–	14	ns
Output hold time	tOH	2.5	–	–	ns
Total system capacitance (each line)	CL	–	–	40	pF

a. Timing is based on CL ≤ 40pF load on CMD and Data.
b. min(Vih) = 0.7 × VDDIO_SD and max(Vil) = 0.2 × VDDIO_SD.

Section 15: USB Interface Timing Specifications

USB 2.0 Electrical and Timing Parameters

Table 30: USB 2.0 Electrical and Timing Parameters

Parameter	Symbol	Condition	Value			Unit
			Minimum	Typical	Maximum	
Baud Rate	B_{PS}	–	–	480	–	Mbit/s
Unit Interval	UI	–	–	2083	–	ps
PLL Clock Generator						
PLL Reference Clock Jitter	$\Delta\tau r_{\phi}$	Peak-to-peak jitter input	–	–	10	ps
PLL Output Jitter	Dt_f	Peak-to-peak jitter	–	–	150	ps
PLL Lock Time	–	–	–	–	30	µs
Receiver—HS						
Differential Input Voltage Sensitivity	V_{HSDI}	Static $\mid V_{IDP} - V_{IDN} \mid$	300	–	–	mV
Input Common Mode Voltage Range	V_{HSCM}	–	–50	–	–	mV
Input Waveform Requirements[a]						
RX Jitter Tolerance[a]	$\Delta\tau_{HSRX}$	Input jitter tolerance	–0.15		0.15	UI
Input Impedance	R_{IN}	Single-ended	40.5	45	49.5	Ω
Squelch Detection Threshold (differential)	V_{HSSQ}	Squelch detected		–	100	mV
		No squelch detected	150	–		mV
Disconnect Detection Threshold (differential)	V_{HSDSC}	Disconnect detected	625	–		mV
		Disconnect not detected	–	–	525	mV
Transmitter—HS						
Output High Voltage	V_{HSOH}	Static condition	360	400	440	mV
Output Low Voltage	V_{HSOL}	Static condition	–10	0	10	mV
Output Waveform Requirements[a]						
Output Rise Time[a]	T_{HSR}	10 to 90%	500	–		ps
Output Fall Time[a]	T_{HSF}	10 to 90%	500	–		ps
TX Jitter Performance[a]	$\Delta\tau_{HSTX}$	TX output jitter	–0.05	–	0.05	UI
Output Impedance	R_O	Single-ended	40.5	45	49.5	Ω
Chirp-J Output Voltage (differential)	V_{CHIRPJ}	HS termination disabled. RPU connected	700	–	1100	mV

Table 30: USB 2.0 Electrical and Timing Parameters (Cont.)

Parameter	Symbol	Condition	Value			Unit
			Minimum	Typical	Maximum	
Chirp-K Output Voltage (differential)	V_{CHIRPK}	HS termination disabled. RPU connected	–900	–	–500	mV

a. See Receiver Eye Diagram Template 4 Figure 7-16 Section 7.1.2.2 of USB 2.0 Specifications.

Section 16: Package Information

Package Thermal Characteristics

Table 31: 138-Ball WLBGA Package Thermal Characteristics[a]

Airflow	0 fpm, 0 mps	100 fpm, 0.508 mps	200 fpm, 0.508 mps	400 fpm, 0.508 mps	600 fpm, 0.508 mps
θ_{JA} (°C/W)	29.79	27.34	26.59	25.79	25.29
θ_{JB} (°C/W)	1.06	–	–	–	–
θ_{JC} (°C/W)	0.09	–	–	–	–
ψ_{JT} (°C/W)	0.03	0.03	0.03	0.03	0.03

a. No heat sink, TA = 85ºC. This is an estimate based on 2-layer PCB and P = 1.1W.

Junction Temperature Estimation and PSI_{JT} VERSUS $THETA_{JC}$

Package thermal characterization parameter PSI-JT (Ψ_{JT}) yields a better estimation of actual junction temperature (T_J) versus using the junction-to-case thermal resistance parameter Theta-JC (Θ_{JC}). The reason for this is Θ_{JC} assumes that all the power is dissipated through the top surface of the package case. In actual applications, some of the power is dissipated through the bottom and sides of the package. Ψ_{JT} takes into account power dissipated through the top, bottom, and sides of the package.

The equation for calculating the device junction temperature is as follows:

$$T_J = T_T + P \times \Psi_{JT}$$

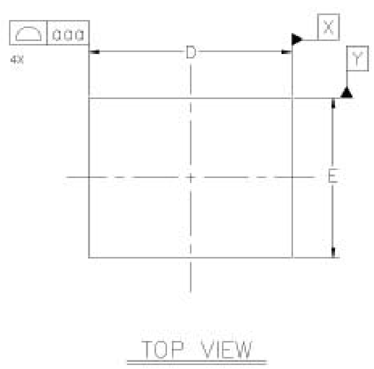
Where:

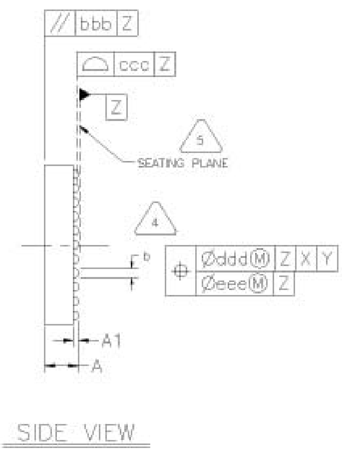
- T_J = Junction temperature at steady-state condition (°C)
- T_T = Package case top center temperature at steady-state condition (°C)
- P = Device power dissipation (Watts)
- Ψ_{JT} = Package thermal characteristics; no airflow (°C/W)

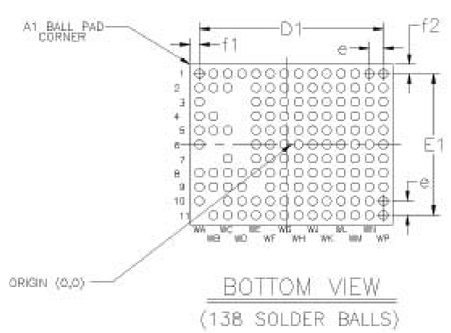
Section 17: Mechanical Information

138-Ball WLBGA Package

Figure 25: 138-Ball WLBGA Mechanical Information







DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0.160	0.190	0.220
D	5.69	5.74	5.79
D1	5.20 REF.		
E	4.48	4.53	4.58
E1	4.00 REF.		
b	0.200	0.250	0.300
e	0.40 BSC		
f1	0.28 BSC		
f2	0.28 BSC		
aaa	–	–	0.10
bbb	–	–	0.10
ccc	–	–	0.05
ddd	–	–	0.10
eee	–	–	0.05

Filename: MOD-033-1263-001

6. PCB LAND PATTERN RECOMMENDATION: LAND PATTERN KEY A REFER TO BROADCOM PACKAGING APPLICATION NOTE "PRINTED CIRCUIT BOARD LAND PATTERN RECOMMENDATIONS FOR BALL GRID ARRAY PACKAGES." PACKAGING-AN503

5. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BUMPS.

4. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BUMP DIAMETER, PARALLEL TO PRIMARY DATUM Z.

3. THE BASIC SOLDER BUMP PITCH IS 0.40mm

2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MO-225.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.

NOTES: UNLESS OTHERWISE SPECIFIED

Section 18: Ordering Information

Table 32: Ordering Information

Part Number	Package	Description	Ambient Temperature
BCM4319GKUBG	138-ball, wafer-level WLBGA package (5.74 mm x 4.53 mm x 0.5 mm, 0.4 mm pitch)	Single-band 802.11b/g/n 2.4GHz WLAN, USB 2.0, SDIO	–30 °C to 85 °C
BCM4319XKUBG	138-ball, wafer-level WLBGA package (5.74 mm x 4.53 mm x 0.5 mm, 0.4 mm pitch)	Dual-band 802.11a/b/g/n 2.4 GHz and 5 GHz WLAN, USB 2.0, SDIO	–30 °C to 85 °C
BCM4319SKUBG	138-ball, wafer-level WLGBA package with Back Side Protection (BSP) (5.74 mm x 4.53 mm x 0.5 mm, 0.4 mm pitch)	Single-band 802.11b/g/n 2.4 GHz WLAN USB2.0, SDIO	–30 °C to 85 °C

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Broadcom Corporation

5300 California Avenue

Irvine, CA 92617

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Phone: 949-926-5000

Fax: 949-926-5203

E-mail: info@broadcom.com

Web: www.broadcom.com

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