

## Low $I_Q$ , Low Dropout 900mA Fixed Voltage Regulator

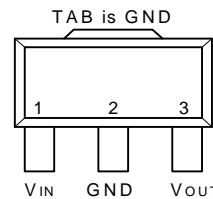
### Features

- Low Noise :  $50\mu V_{RMS}$  (100Hz to 100kHz)
- Low Quiescent Current :  $50\mu A$  (No load)
- Low Dropout Voltage :  $210mV$  (@900mA)
- Very low Shutdown Current :  $< 1\mu A$
- Fixed Output Voltage :  $1.3V \sim 3.4V$
- Stable with  $4.7\mu F$  Output Capacitor
- Stable with Aluminum , Tantalum or Ceramic Capacitors .
- Reverse Current Protection
- No Protection Diodes Needed
- Built in Thermal Protection
- Built in Current Limit Protection
- Controlled Short Circuit Current :  $200mA$
- Fast Transient Response
- Short Setting Time
- SOT-89, SOT-89-5, SOT-223, SO-8 ,TO-252 and TO-252-5 Packages

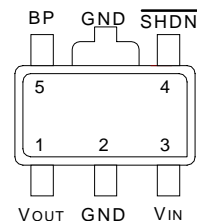
Design with an internal P-channel MOSFET pass transistor, the APL5901/2 maintains a low supply current, independent of the load current and dropout voltage. Other features include reverse current protection, thermal-shutdown protection, current limit protection to ensure specified output current and controlled short-circuit current. The APL5901/2 regulator come in a miniature SOT-89, SOT-89-5, SOT-223, SO-8, TO-252 and TO-252-5 packages.

### Pin Configuration

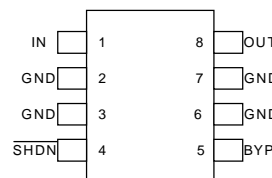
APL5901



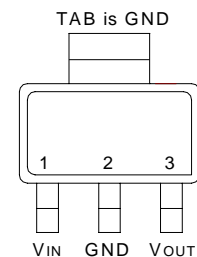
SOT-89 (Top View)



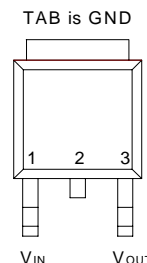
SOT-89-5 (Top View)



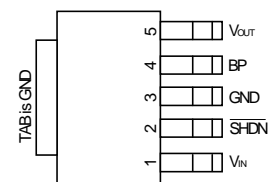
SO-8 (Top View)



SOT-223 (Top View)



TO-252 (Top View)



TO-252-5 (Top View)

### Applications

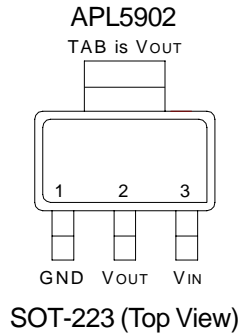
- Notebook Computer
- PDA or Portable Equipments
- Noise-Sensitive Instrumentation Systems

### General Description

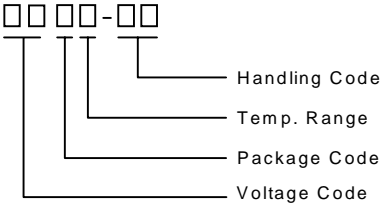

The APL5901/2 is micropower, low noise, low dropout linear regulator. Operate from 2.7V to 6V input voltage and deliver up to 900mA. Typical output noise is just  $50\mu V_{RMS}$  with the addition of an external  $0.1\mu F$  bypass capacitor in BP pin and typical dropout voltage is only  $210mV$  at 900mA loading. Designed for use in battery-powered system, the low  $50\mu A$  quiescent current makes it an ideal choice.

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

### Pin Configuration (Cont.)



### Ordering and Marking Information

<p>APL5901/2 - □□□□-□□</p>  <p style="margin-left: 100px;">Handling Code Temp. Range Package Code Voltage Code</p>	<p>Package Code D : S OT-89                      D5 : SOT-89-5                      U : TO-252 U5 : TO-252-5                      V : SOT-223                      K : SO-8 Temp. Range C : 0 to 70 °C Handling Code TR : Tape &amp; Reel Voltage Code : 13 : 1.3V ~ 34 : 3.4V</p>
<p>APL5901/2 - 13 D/V/K : <span style="border: 1px solid black; padding: 2px;">APL5901/2 XXXXX13</span></p>	<p>XXXXX - Date Code , 13 - 1.3V</p>
<p>APL5901/2 - 13 U : <span style="border: 1px solid black; padding: 2px;"> 13 APL5901/2 XXXXX</span></p>	<p>XXXXX - Date Code , 13 - 1.3V</p>

### Pin Description

PIN		I/O	Description
No.	Name		
1	V <sub>IN</sub>	I	Supply voltage input.
2	GND		Ground pins of the circuitry, and all ground pins must be soldered to PCB with proper power dissipation.
3	SHDN <sup>(Note1)</sup>	I	Shutdown control pin, low = off , high = normal .
4	BP <sup>(Note1)</sup>	O	Bypass signal pin in fixed output type device
5	V <sub>OUT</sub>	O	Output pin of the regulator.

Note1 : These pins do not exist in 3-pin package.

## Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
$V_{IN}, V_{OUT}$	Input Voltage or Out Voltage	6	V
$\overline{SHDN}$	Shutdown Control Pin	6	V
$R_{TH,JA}$	Thermal Resistance – Junction to Ambient	SOT-89 : 180 SOT-223 : 135 SO-8 : 150 TO-252 : 50	°C/W
$P_D$	Power Dissipation	Internally Limited	W
$T_J$	Operating Junction Temperature		°C
	Control Section	0 to 125	
	Power Transistor	0 to 150	
$T_{STG}$	Storage Temperature Range	-65 to +150	°C
$T_L$	Lead Temperature (Soldering, 10 second)	260	°C

## Electrical Characteristics

Unless otherwise noted these specifications apply over full temperature,  $V_{IN}=3.6V$ ,  $C_{IN}=1\mu F$ ,  $C_{OUT}=4.7\mu F$ ,  $\overline{SHDN}=V_{IN}$ ,  $T_J=0$  to  $125^\circ C$ . Typical values refer to  $T_J=25^\circ C$ .

Symbol	Parameter	Test Conditions	APL5901/2			Unit
			Min.	Typ.	Max.	
$V_{IN}$	Input Voltage		2.7		6	V
$V_{OUT}$	Output Voltage	$V_{OUT}+1.0V < V_{CC} < 6.0V$ , $0mA < I_{OUT} < I_{MAX}$	$V_{OUT}-2\%$	$V_{OUT}$	$V_{OUT}+2\%$	V
$I_{LIMIT}$	Circuit Current Limit	$V_{IN}=4.3V$		1.5		A
$I_{SHORT}$	Short Current	$V_{OUT}=0V$		200		mA
$I_{OUT}$	Load Current		900			mA
$REG_{LINE}$	Line Regulation	$V_{OUT}+0.5V < V_{CC} < 6.0V$ , $0mA < I_{OUT} < I_{MAX}$		4	10	mV
$REG_{LOAD}$	Load Regulation	$V_{IN} = V_{OUT}+1.0V$ , $0mA < I_{OUT} < I_{MAX}$		1	6	mV
$V_{DROP}$	Dropout Voltage <sup>(Note2)</sup> ( $V_{OUT}(\text{Nominal})=3.0V$ Version)	$I_{OUT} = 900mA$		210	300	mV
PSRR	Ripple Rejection	$F \leq 1kHz$ , 1Vpp at $V_{IN} = V_{OUT}+1.0V$	55	65		dB
$I_Q$	Quiescent Current	No load		50	100	$\mu A$
		$I_{OUT}=900mA$		370	450	
	Shutdown Supply Current <sup>(Note3)</sup>	Shutdown = low $I_{OUT}=0$ , $V_{CC} = 6.0V$		0.01	1	$\mu A$
	Noise <sup>(Note3)</sup>	100Hz<f<100kHz, typical load, $C_{BP}=0.01\mu F$ , $C_{OUT} = 1\mu F$		50		$\mu V_{rms}$
		100Hz<f<100kHz, typical load, $C_{BP}=0.1\mu F$ , $C_{OUT} = 1\mu F$		40		
	Shutdown Recovery Delay <sup>(Note3)</sup>	$C_{BP}=0.01\mu F, C_{OUT}=1\mu F$ , no load		7		ms
		$C_{BP}=0.1\mu F, C_{OUT}=1\mu F$ , no load		70		

## Electrical Characteristics (Cont.)

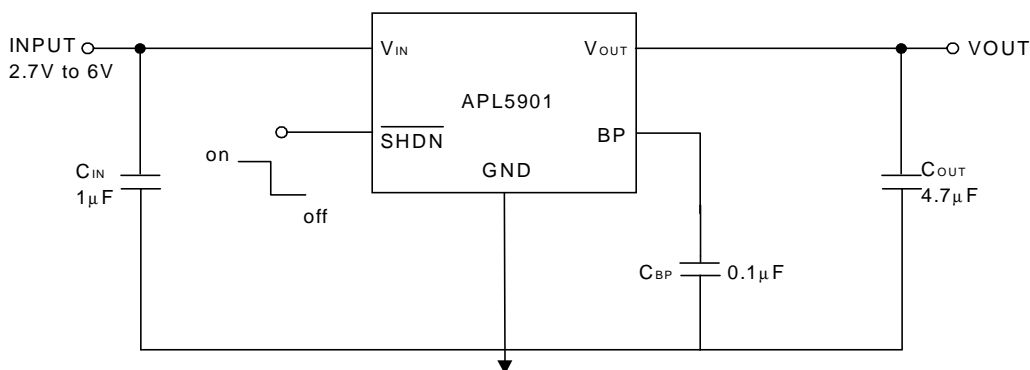
Unless otherwise noted these specifications apply over full temperature,  $V_{IN}=3.6V$ ,  $C_{IN}=1\mu F$ ,  $C_{OUT}=4.7\mu F$ ,  $\overline{SHDN}=V_{IN}$ ,  $T_J=0$  to  $125^\circ C$ . Typical values refer to  $T_J=25^\circ C$ .

Symbol	Parameter	Test Conditions	APL5901/2			Unit
			Min.	Typ.	Max.	
OTS	Over Temperature Shutdown			150		$^\circ C$
	Over Temperature Shutdown Hysteresis	Hysteresis		10		$^\circ C$
TC	Output Voltage Temperature Coefficient			50		ppm/ $^\circ C$
$C_{OUT}$	Output Capacitor		4.2	4.7	5.2	$\mu F$
	ESR		0.02	0.1	1	Ohm
	Shutdown Input Threshold <sup>(Note3)</sup>	$V_{OUT}+1.0V < V_{IN} < 6.0V$	0.4	0.7	1.6	V
$I_{\overline{SHDN}}$	Shutdown input Bias current <sup>(Note3)</sup>	$V_{\overline{SHDN}}=V_{IN}$		0.01	100	nA
	Input Reverse Leakage current	$V_{OUT}-V_{IN}=0.1V$		0.1	0.5	$\mu A$
	Reverse Protection Threshold			11	50	mV

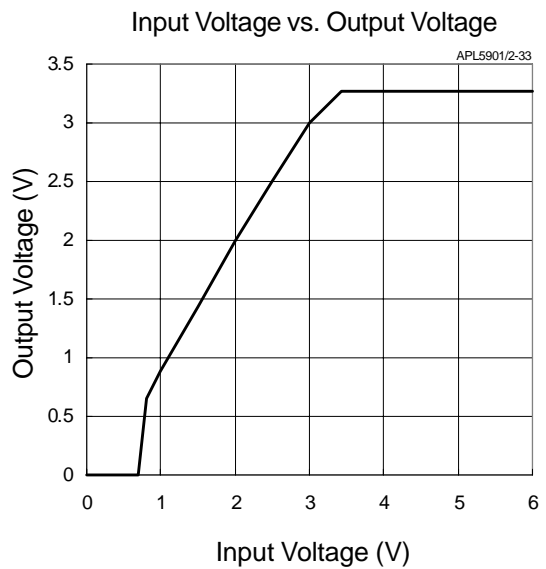
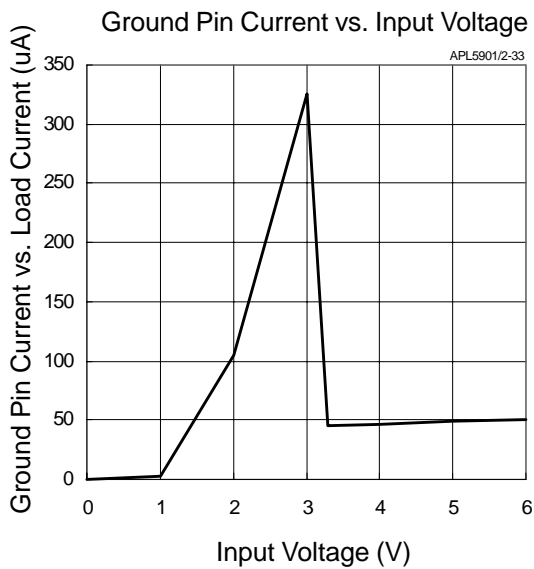
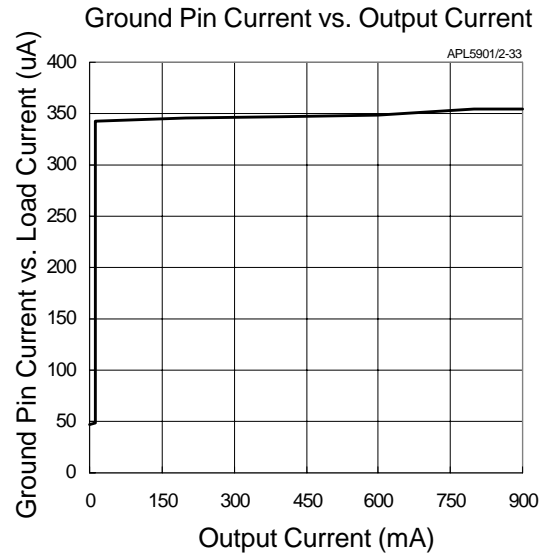
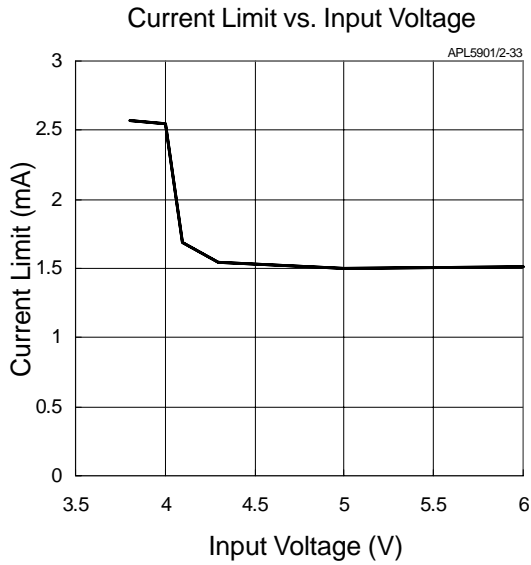
Note 2 : Dropout voltage definition :  $V_{IN}-V_{OUT}$  when  $V_{OUT}$  is 2% below the value of  $V_{OUT}$  for  $V_{IN} = V_{OUT} + 0.5V$

Note 3 : For 5-pin devices only.

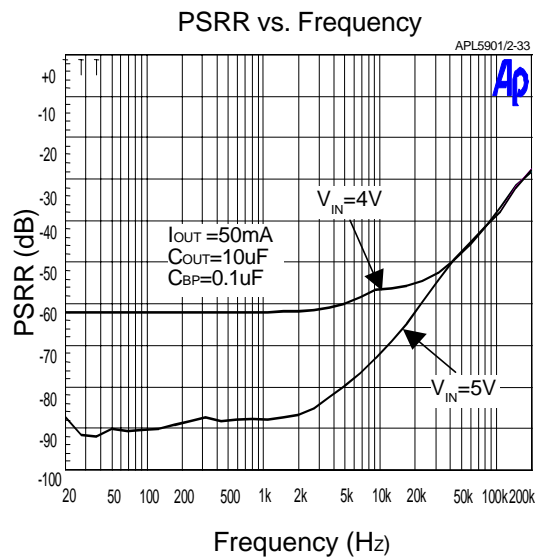
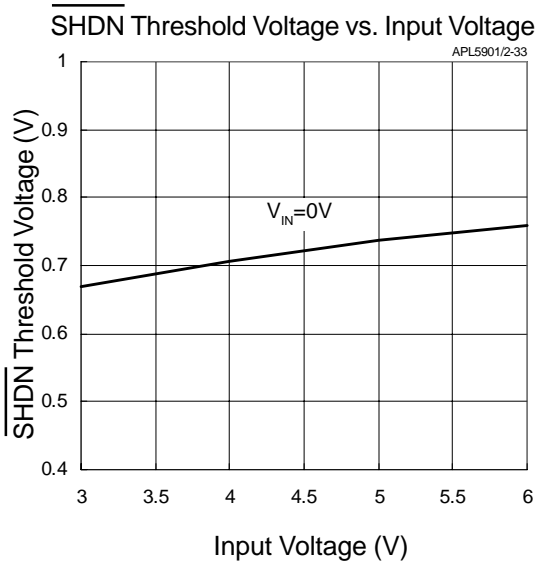
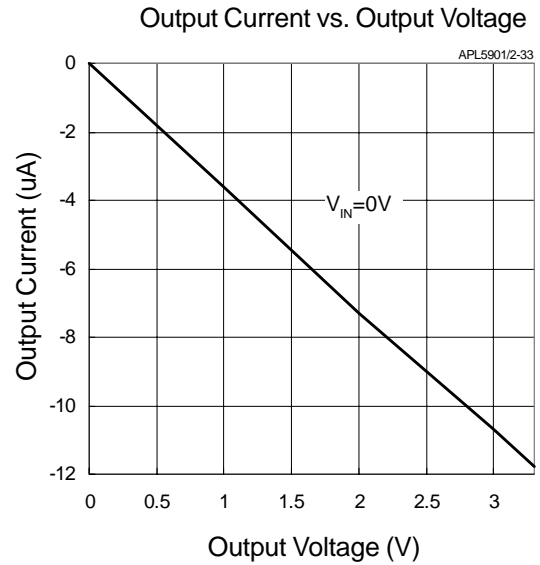
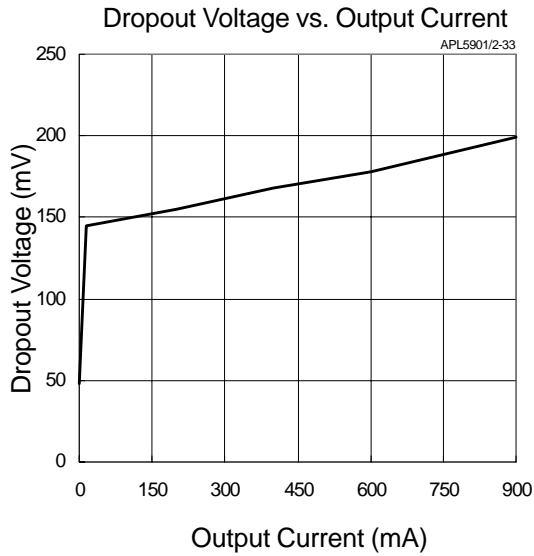
## Application Circuit



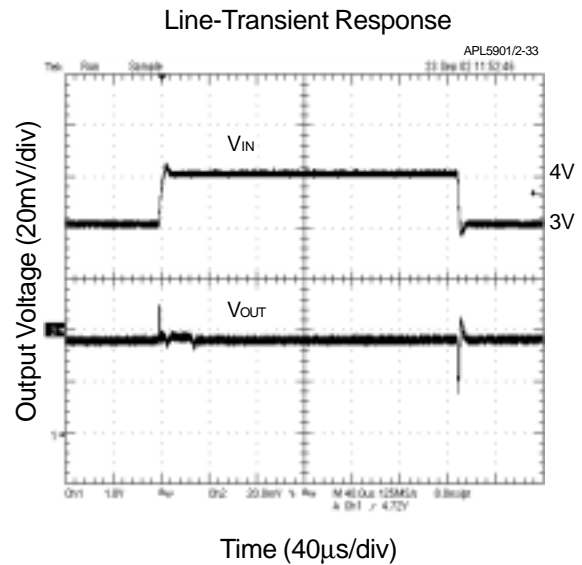
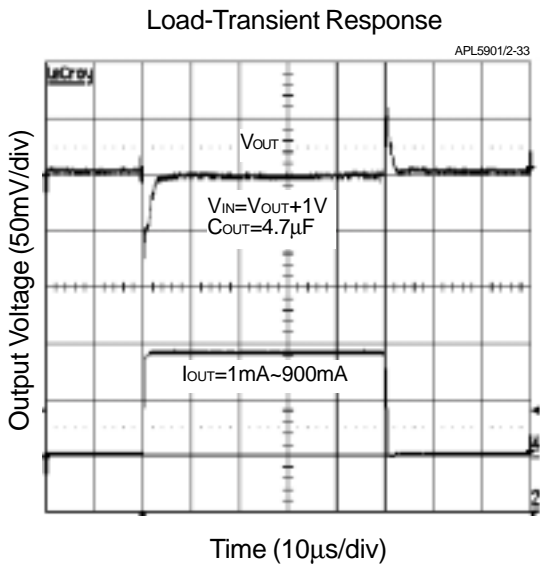
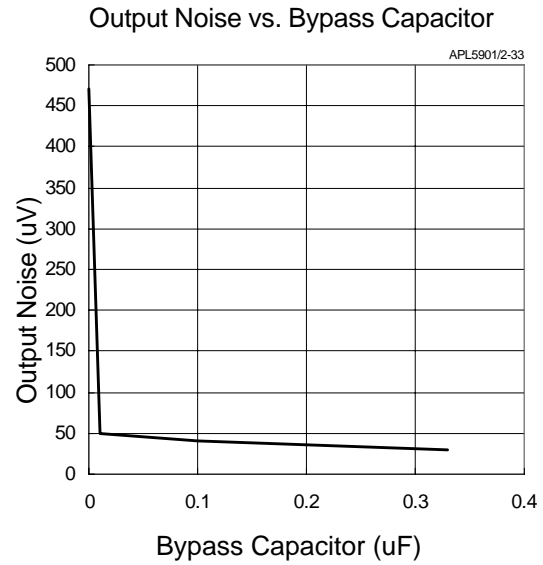
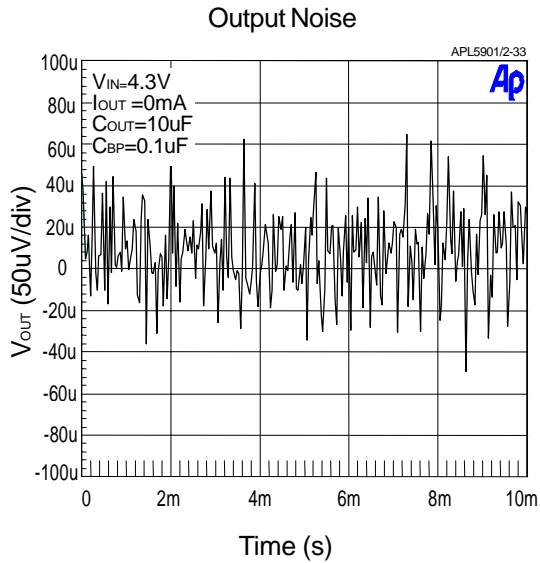
## Typical Characteristics



## Typical Characteristics

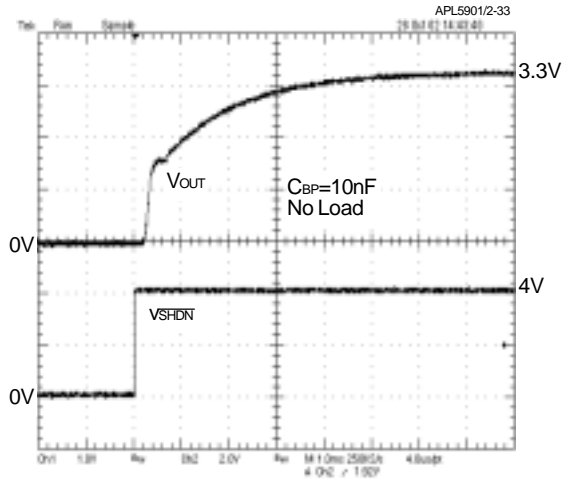


## Typical Characteristics

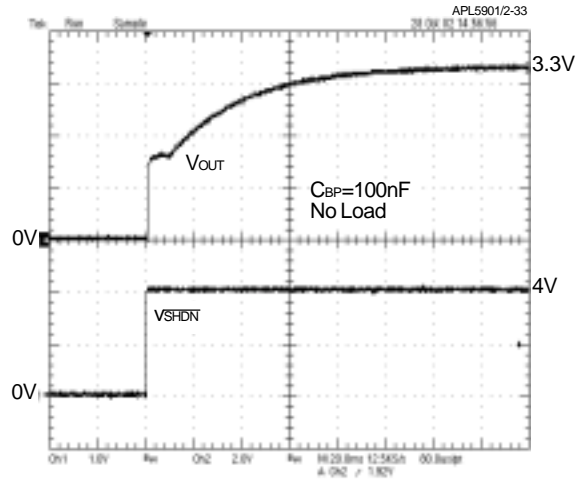


## Typical Characteristics

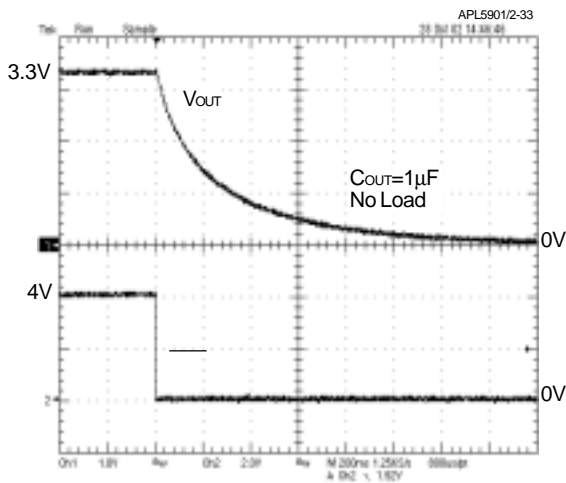
Shutdown Exit Delay



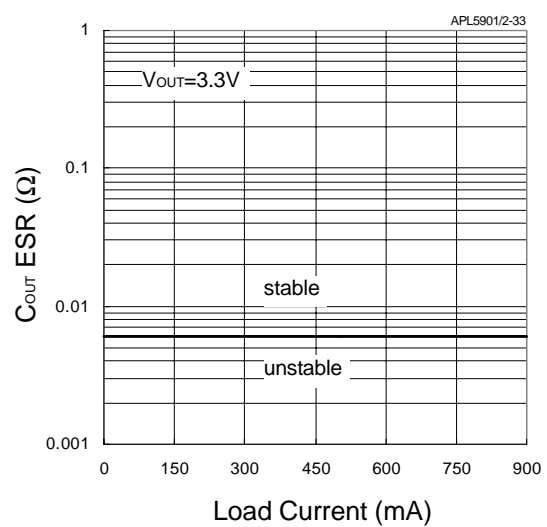
Shutdown Exit Delay



Entering Shutdown

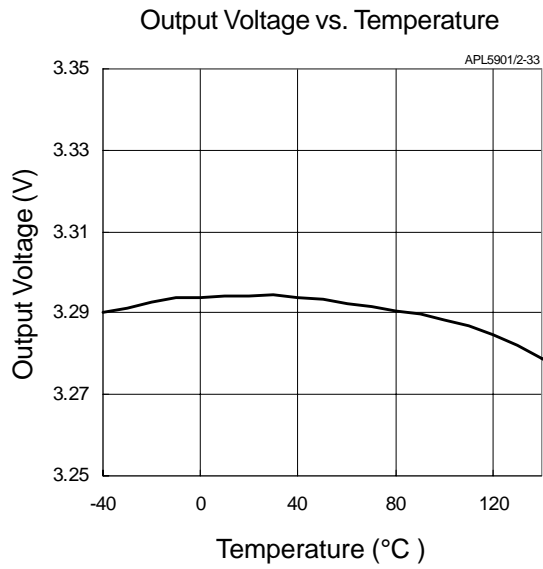


Region of Stable ESR vs. Load Current





## Typical Characteristics



## Application Information

### Capacitor Selection and Regulator Stability

The APL5901/2 use at least a 1 $\mu$ F capacitor on the input, and this capacitor can be Aluminum, Tantalum or Ceramic capacitor. The input capacitor with larger value and lower ESR provides better PSRR and line-transient response. The output capacitor also can use Aluminum, Tantalum or Ceramic capacitor, and a minimum value of 4.7 $\mu$ F and ESR above 0.02 $\Omega$  is recommended. A larger output capacitor can reduce noise and improve load-transient response, stability, and PSRR. Note that some ceramic dielectrics exhibit large capacitance and ESR variation with temperature. When using this capacitor, a minimum 10 $\mu$ F or more may be required to ensure the stability at low temperature operation. Use a bypass capacitor at BP pin for low output noise. Increasing the capacitance will slightly decrease the output noise, but increase the start-up time.

### Load-Transient Considerations

The APL5901/2 load-transient response graphs in typical characteristics show the transient response. A step change in the load current from 10mA to 900mA at 10 $\mu$ s will cause a 20mV transient spike. Larger output capacitor and lower ESR can reduce transient spike.

### Input-Output (Dropout)Voltage

The minimum input-output voltage difference (dropout) determines the lowest usable supply voltage. In battery-powered systems, this will determine the useful end-of-life battery voltage. Because the APL5901/2 use a p-channel MOSFET pass transistor, the dropout voltage is a function of drain-to-source on-resistance ( $R_{DS(ON)}$ ) multiplied by the load current.

### Reverse Current Protection

The APL5901/2 have an internal reverse protection, it does not need an external schottky diode to connect the regulator input and output. If the output voltage is forced above the input voltage by more than 11mV, the IC will be shutdown and the ground pin current is below 0.1 $\mu$ A.

### Current Limit

The APL5901/2 have a current limit protection. The output voltage will drop close to zero volt, when load current reaches the limit, and then the load current will be limited at 200mA after output voltage is below 0.7V. When the load current back to the value where limiting started, the output voltage and current will return to normal value. When output is shorted to ground, the APL5901/2 will keep short circuit current at 200mA .

## Thermal Protection

Thermal protection limits total power dissipation in the device. When the junction temperature exceeds  $T_J=+150^{\circ}\text{C}$ , the thermal sensor generates a logic signal to turn off the pass transistor and allows IC to cool. When the IC's junction temperature is down by  $10^{\circ}\text{C}$ , the thermal sensor will turn the pass transistor on again, resulting in a pulsed output during continuous thermal protection. Thermal protection is designed to protect the APL5901/2 in the event of fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature of  $T_J=+150^{\circ}\text{C}$ .

## Operating Region and Power Dissipation

The thermal resistance of the case to circuit board, and the rate of air flow all control the APL5901/2's maximum power dissipation. The power dissipation across the device is  $P_D = I_{OUT}(V_{IN}-V_{OUT})$  and the maximum power dissipation is:

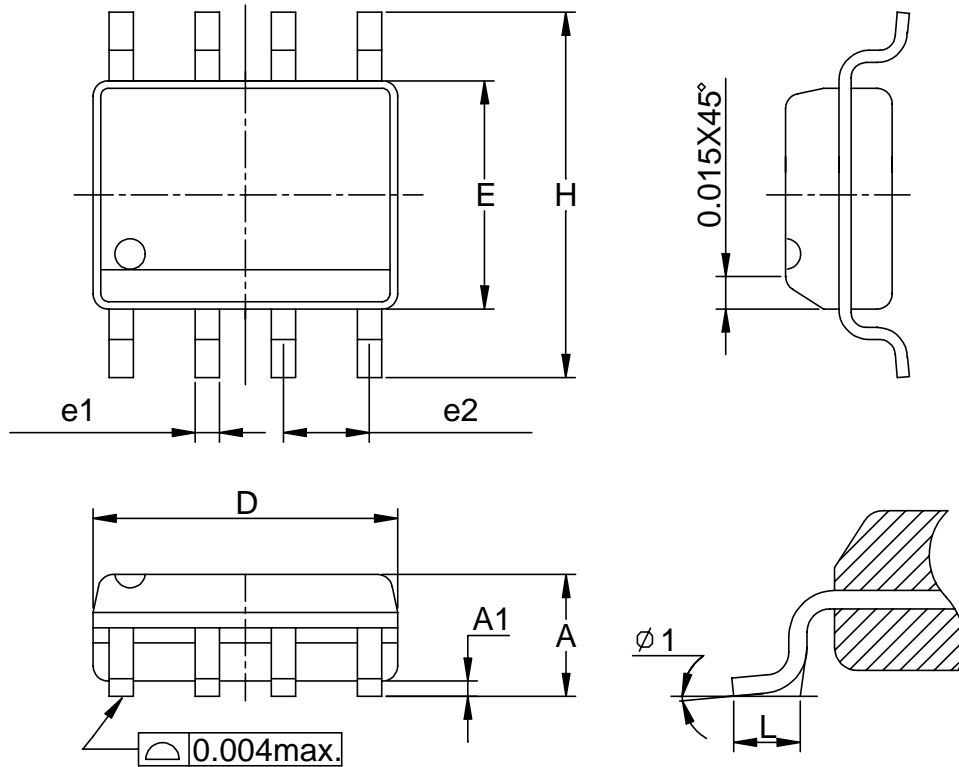
$$P_{DMAX} = (T_J - T_A) / (\theta_{JC} + \theta_{CA})$$

where  $T_J - T_A$  is the temperature difference between the junction and ambient air,  $\theta_{JC}$  is the thermal resistance of the package, and  $\theta_{CA}$  is the thermal resistance through the printed circuit board, copper traces, and other materials to the ambient air.

The GND pin of the APL5901 provide an electrical connection to ground and channeling heat away. If power dissipation is large, connect the GND pin to ground using a large pad or ground plane, can improve the problem of over heat of IC.

## Packaging Information

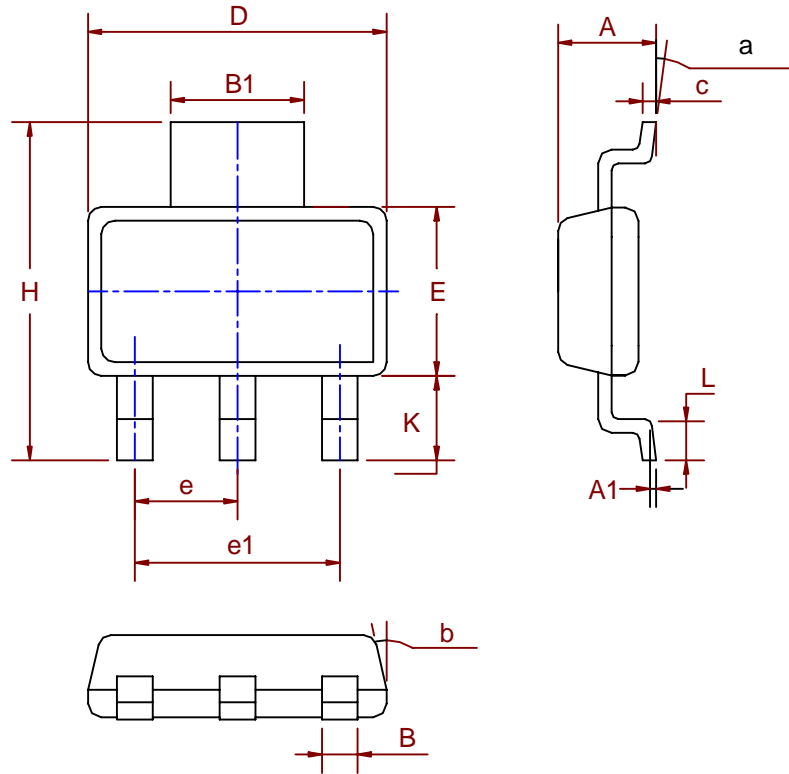
SOP-8 pin ( Reference JEDEC Registration MS-012)



Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	4.80	5.00	0.189	0.197
E	3.80	4.00	0.150	0.157
H	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
e1	0.33	0.51	0.013	0.020
e2	1.27BSC		0.50BSC	
φ 1	8°		8°	

## Packaging Information

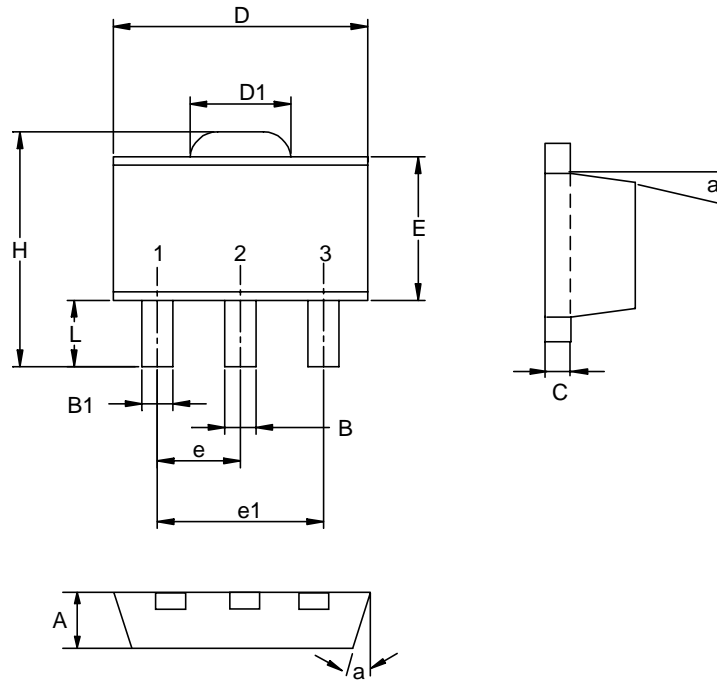
SOT-223( Reference JEDEC Registration SOT-223)



Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.50	1.80	0.06	0.07
A1	0.02	0.08		
B	0.60	0.80	0.02	0.03
B1	2.90	3.10	0.11	0.12
c	0.28	0.32	0.01	0.01
D	6.30	6.70	0.25	0.26
E	3.30	3.70	0.13	0.15
e	2.3 BSC		0.09 BSC	
e1	4.6 BSC		0.18 BSC	
H	6.70	7.30	0.26	0.29
L	0.91	1.10	0.04	0.04
K	1.50	2.00	0.06	0.08
α	0°	10°	0°	10°
β	13°		13°	

## Packaging Information

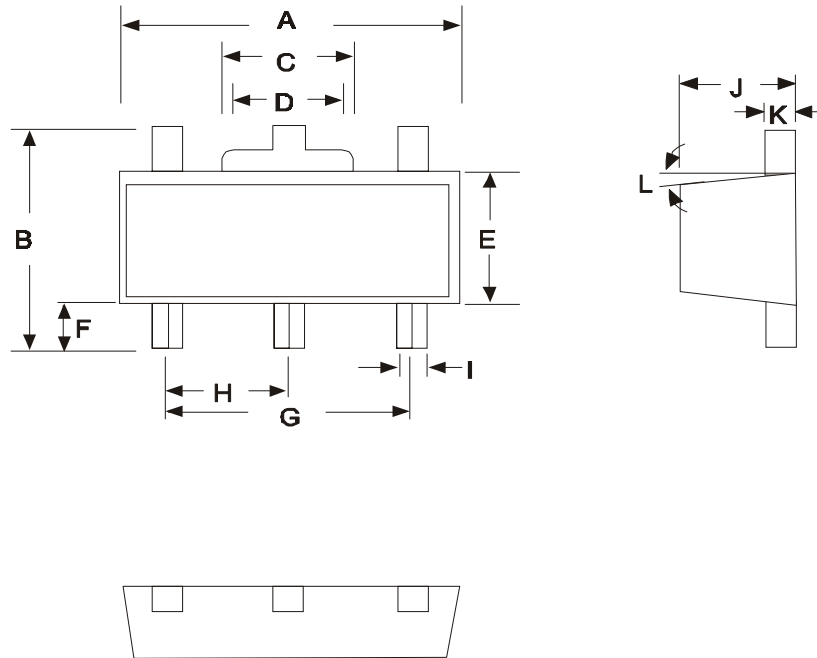
SOT-89 (Reference EIAJ ED-7500A Registration SC-62)



Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.40	1.60	0.055	0.063
B	0.40	0.56	0.016	0.022
B1	0.35	0.48	0.014	0.019
C	0.35	0.44	0.014	0.017
D	4.40	4.60	0.173	0.181
D1	1.35	1.83	0.053	0.072
e	1.50 BSC		0.059 BSC	
e1	3.00 BSC		0.118 BSC	
E	2.29	2.60	0.090	0.102
H	3.75	4.25	0.148	0.167
L	0.80	1.20	0.031	0.047
α		10°		10°

## Packaging Information

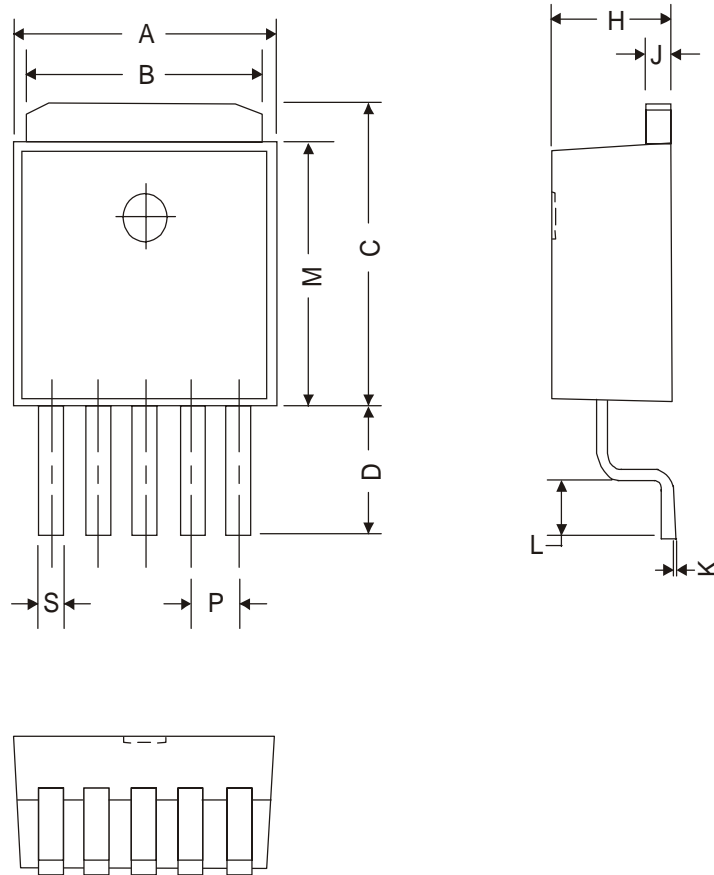
SOT-89-5



Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	4.40	4.60	0.17	0.18
B	4.05	4.25	0.16	0.17
C	1.50	1.70	0.06	0.07
D	1.30	1.50	0.05	0.06
E	2.40	2.60	0.09	0.1
F	0.80	-	0.03	-
G	3.00 REF		0.12 REF	
H	1.50 REF		0.06 REF	
I	0.40	0.52	0.01	0.02
J	1.40	1.60	0.05	0.06
K	0.35	0.41	0.01	0.02
L	5 TYP		0.2 TYP	

## Packaging Information

TO-252-5

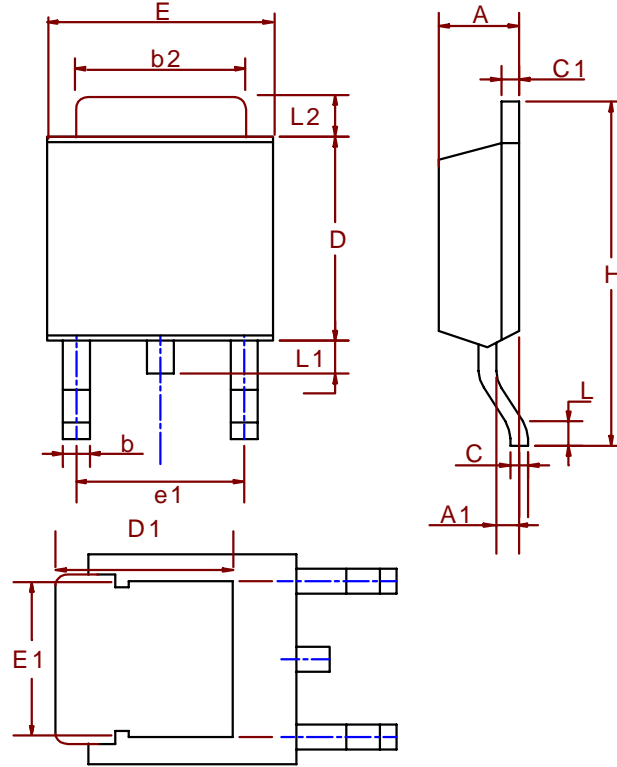


Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	6.40	6.80	0.25	0.26
B	5.20	5.50	0.20	0.21
C	6.80	7.20	0.26	0.27
D	2.20	2.80	0.08	0.11
P	1.27 REF		0.05 REF	
S	0.50	0.80	0.02	0.03
H	2.20	2.40	0.08	0.09
J	0.45	0.55	0.01	0.02
K	0	0.15	0	0.006
L	0.90	1.50	0.03	0.06
M	5.40	5.80	0.21	0.22



## Packaging Information

TO-252 (Reference JEDEC Registration TO-252)



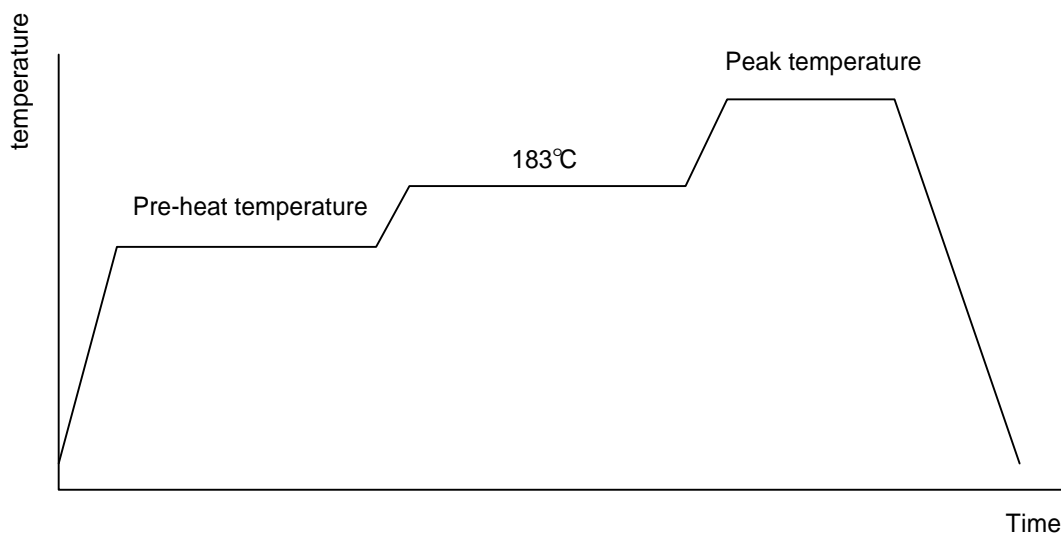
Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	2.18	2.39	0.086	0.094
A1	0.89	1.27	0.035	0.050
b	0.508	0.89	0.020	0.035
b2	5.207	5.461	0.205	0.215
C	0.46	0.58	0.018	0.023
C1	0.46	0.58	0.018	0.023
D	5.334	6.22	0.210	0.245
D1	5.2 REF		0.205 REF	
E	6.35	6.73	0.250	0.265
E1	5.3 REF		0.209 REF	
e1	3.96	5.18	0.156	0.204
H	9.398	10.41	0.370	0.410
L	0.51		0.020	
L1	0.64	1.02	0.025	0.040
L2	0.89	2.032	0.035	0.080

## Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb)
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.

## Reflow Condition (IR/Convection or VPR Reflow)

Reference JEDEC Standard J-STD-020A APRIL 1999



## Classification Reflow Profiles

	Convection or IR/ Convection	VPR
Average ramp-up rate(183°C to Peak)	3°C/second max.	10 °C /second max.
Preheat temperature 125 ± 25°C)	120 seconds max	
Temperature maintained above 183°C	60 – 150 seconds	
Time within 5°C of actual peak temperature	10 –20 seconds	60 seconds
Peak temperature range	220 +5/-0°C or 235 +5/-0°C	215-219°C or 235 +5/-0°C
Ramp-down rate	6 °C /second max.	10 °C /second max.
Time 25°C to peak temperature	6 minutes max.	

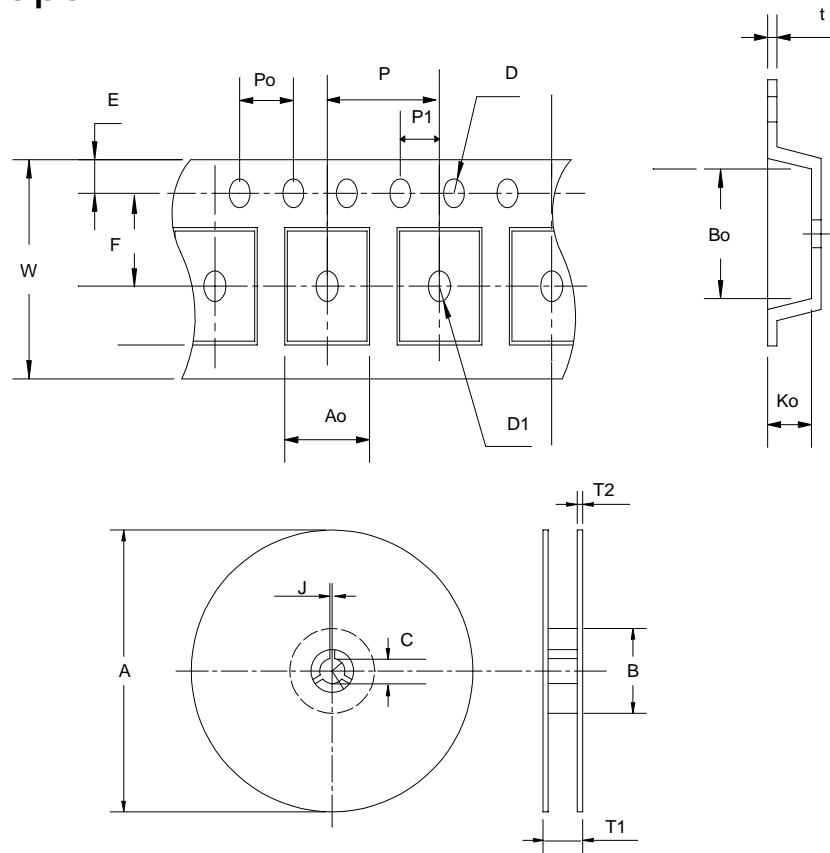
## Package Reflow Conditions

pkg. thickness ≥ 2.5mm and all bgas	pkg. thickness < 2.5mm and pkg. volume ≥ 350 mm <sup>3</sup>	pkg. thickness < 2.5mm and pkg. volume < 350mm <sup>3</sup>
Convection 220 +5/-0 °C		Convection 235 +5/-0 °C
VPR 215-219 °C		VPR 235 +5/-0 °C
IR/Convection 220 +5/-0 °C		IR/Convection 235 +5/-0 °C

## Reliability test program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C , 5 SEC
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @ 125 °C
PCT	JESD-22-B, A102	168 Hrs, 100 % RH , 121°C
TST	MIL-STD-883D-1011.9	-65°C ~ 150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms , I <sub>tr</sub> > 100mA

## Carrier Tape



## Reel Dimensions

Application	A	B	C	J	T1	T2	W	P	E
SOP- 8	330 ± 1	62 +1.5	12.75+ 0.15	2 ± 0.5	12.4 ± 0.2	2 ± 0.2	12± 0.3	8± 0.1	1.75±0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	5.5± 1	1.55 +0.1	1.55+ 0.25	4.0 ± 0.1	2.0 ± 0.1	6.4 ± 0.1	5.2± 0.1	2.1± 0.1	0.3±0.013
Application	A	B	C	J	T1	T2	W	P	E
SOT-89	178 ± 1	70 ± 2	13.5 ± 0.15	3 ± 0.15	14 ± 2	1.3 ± 0.3	12 + 0.3 12 - 0.1	8 ± 0.1	1.75 ± 0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	5.5 ± 0.05	1.5± 0.1	1.5± 0.1	4.0 ± 0.1	2.0 ± 0.1	4.8 ± 0.1	4.5± 0.1	1.80± 0.1	0.3±0.013
Application	A	B	C	J	T1	T2	W	P	E
SOT-223	330±1	62±1.5	12.75± 0.15	2 ± 0.6	12.4 +0.2	2± 0.2	12 ± 0.3	8 ± 0.1	1.75± 0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	5.5 ± 0.05	1.5+ 0.1	1.5+ 0.1	4.0 ± 0.1	2.0 ± 0.05	6.9 ± 0.1	7.5± 0.1	2.1± 0.1	0.3±0.05
Application	A	B	C	J	T1	T2	W	P	E
TO-252	330 ± 3	100 ± 2	13 ± 0.5	2 ± 0.5	16.4 + 0.3 -0.2	2.5± 0.5	16+ 0.3 - 0.1	8 ± 0.1	1.75± 0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	7.5 ± 0.1	1.5 +0.1	1.5± 0.25	4.0 ± 0.1	2.0 ± 0.1	6.8 ± 0.1	10.4± 0.1	2.5± 0.1	0.3±0.05

## Cover Tape Dimensions

Application	Carrier Width	Cover Tape Width	Devices Per Reel
SOP- 8	12	9.3	2500
SOT- 89	12	9.3	1000
SOT- 223	12	9.3	2500
TO- 252	16	13.3	2500

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