UNISONIC TECHNOLOGIES CO., LTD

VGA7S019　　　Preliminary　　　*TVS*

7-CHANNEL INTEGRATED ESD SOLUTION FOR VGA PORT WITH INTEGRATED LEVEL SHIFTER AND MATCHING IMPEDANCE

SSOP-16

■　DESCRIPTION

The UTC **VGA7S019** is an ESD solution for the VGA or DVI-I port connector. This device integrates ESD protection for all signals, level shifting for the DDC signals and buffering for the SYNC signals. ESD protection for the VIDEO, DDC and SYNC lines is implemented with low-capacitance current steering diodes.

Separate positive supply rails are provided for the VIDEO, DDC and SYNC channels to facilitate interfacing with low voltage video controller ICs to provide design flexibility in multi-supply-voltage environments.

Two non-inverting drivers provide buffering for the HSYNC and VSYNC signals from the video controller IC (SYNC1, SYNC2). These buffers accept TTL input levels and convert them to CMOS output levels that swing between Ground and VCC_SYNC, which is typically 5V. Additionally, each driver has a series termination resistor (RT) connected to the SYNC_OUT pin, eliminating the external termination resistors typically required for the HSYNC and VSYNC lines of the video cable. At the SYNC output the UTC **VGA7S019** offers 65-Ω, 55-Ω, or 15-Ω series termination resistor option to match different transmission line impedances.

Two N-channel MOSFETs provide the level shifting function required when the DDC controller is operated at a lower supply voltage than the monitor. The gate terminals for the MOSFETs (VCC_DDC) should be connected to the supply rail (typically 3.3V) that supplies power to the transceivers of the DDC controller.

The UTC **VGA7S019** confirms the IEC61000-4-2 (Level 4) system level ESD protection and ±15KV HBM ESD protection. This device is offered in space-saving SSOP-16 packages.

■　FEATURES

* 7 Channels of ESD protection for all VGA port connector pins meeting IEC-61000-4-2 Level 4 ESD requirements (±8kV contact discharge)
* Integrated impedance matching resistors on sync lines:
  - VGA7S019-15: 15Ω Termination
  - VGA7S019-55: 55Ω Termination
  - VGA7S019-65: 65Ω Termination
* Includes ESD protection, level-shifting, buffering and sync impedance matching

* 5V drivers for HSYNC and VSYNC lines
* Very low loading capacitance from ESD protection diodes on VIDEO lines (2.5pF)
* Bi-Directional level shifting N-Channel FETs provided for DDC_CLK and DDC_DATA channels
* Flow-Through single-in-line pin mapping ensures no additional board layout burden while placing the ESD protection chip near the connector
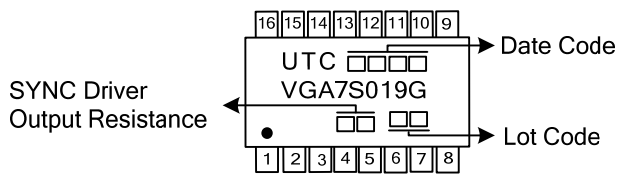
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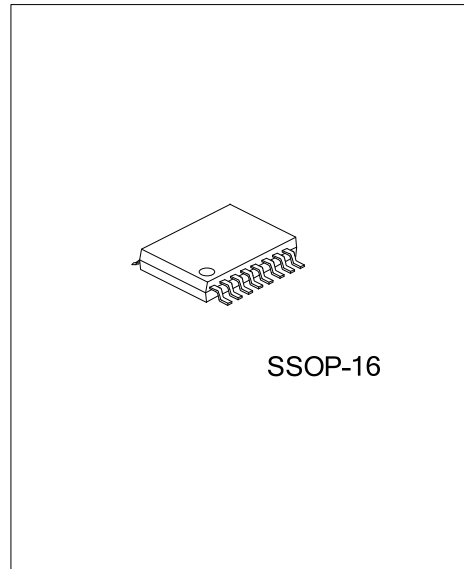
■ **ORDERING INFORMATION**

Ordering Number	Package	Packing
VGA7S019G-xx-R16-T	SSOP-16	Tube
VGA7S019G-xx-R16-R	SSOP-16	Tape Reel

Note: xx: Output Voltage, refer to Marking Information.
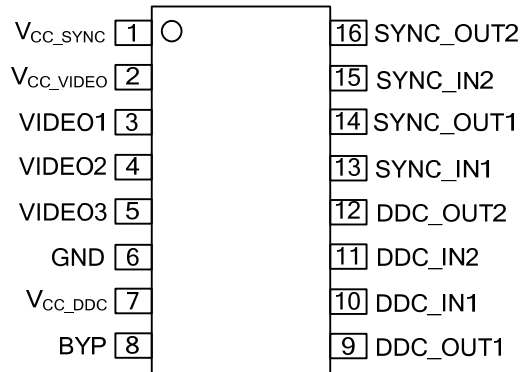
VGA7S019G-xx-R16-T	
(1)Packing Type	(1) T: Tube, R: Tape Reel
(2)Package Type	(2) R16: SSOP-16
(3)SYNC Driver Output Resistance	(3) xx: 15, 55, 65
(4)Green Package	(4) G: Halogen Free and Lead Free

■ **MARKING**

16 15 14 13 12 11 10 9

U T C ▭▭▭▭ → Date Code
VGA7S019G

SYNC Driver ← ▭▭ ▭▭
Output Resistance

● ▭▭ ▭▭ → Lot Code

1 2 3 4 5 6 7 8

■ **PIN CONFIGURATION**

```
V_CC_SYNC   [1]  O          [16] SYNC_OUT2
V_CC_VIDEO  [2]             [15] SYNC_IN2
VIDEO1      [3]             [14] SYNC_OUT1
VIDEO2      [4]             [13] SYNC_IN1
VIDEO3      [5]             [12] DDC_OUT2
GND         [6]             [11] DDC_IN2
V_CC_DDC    [7]             [10] DDC_IN1
BYP         [8]             [9]  DDC_OUT1
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■ **PIN DESCRIPTION**

PIN NO.	PIN NAME	DESCRIPTION
1	VCC_SYNC	Isolated supply input for the SYNC_1 and SYNC_2 level shifters and their associated ESD protection circuits
2	VCC_VIDEO	Supply pin specifically for the VIDEO_1, VIDEO_2 and VIDEO_3 ESD protection circuits
3	VIDEO1	High-speed ESD clamp input
4	VIDEO2	
5	VIDEO3	
6	GND	Ground
7	VCC_DDC	Isolated supply input for the DDC_1 and DDC_2 level-shifting N-FET gates
8	BYP	Bypass pin. Using a 0.2µF bypass capacitor will increase the ESD robustness of the system.
9	DDC_OUT1	DDC signal output. Connects to the video connector side of one of the sync lines.
10	DDC_IN1	DDC signal input. Connects to the VGA controller side of one of the sync lines.
11	DDC_IN2	
12	DDC_OUT2	DDC signal output. Connects to the video connector side of one of the sync lines.
13	SYNC_IN1	Sync signal buffer input. Connects to the VGA controller side of one of the sync lines.
14	SYNC_OUT1	Sync signal buffer output. Connects to the video connector side of one of the sync lines
15	SYNC_IN2	Sync signal buffer input. Connects to the VGA controller side of one of the sync lines.
16	SYNC_OUT2	Sync signal buffer output. Connects to the video connector side of one of the sync lines

■ **BLOCK DIAGRAM**
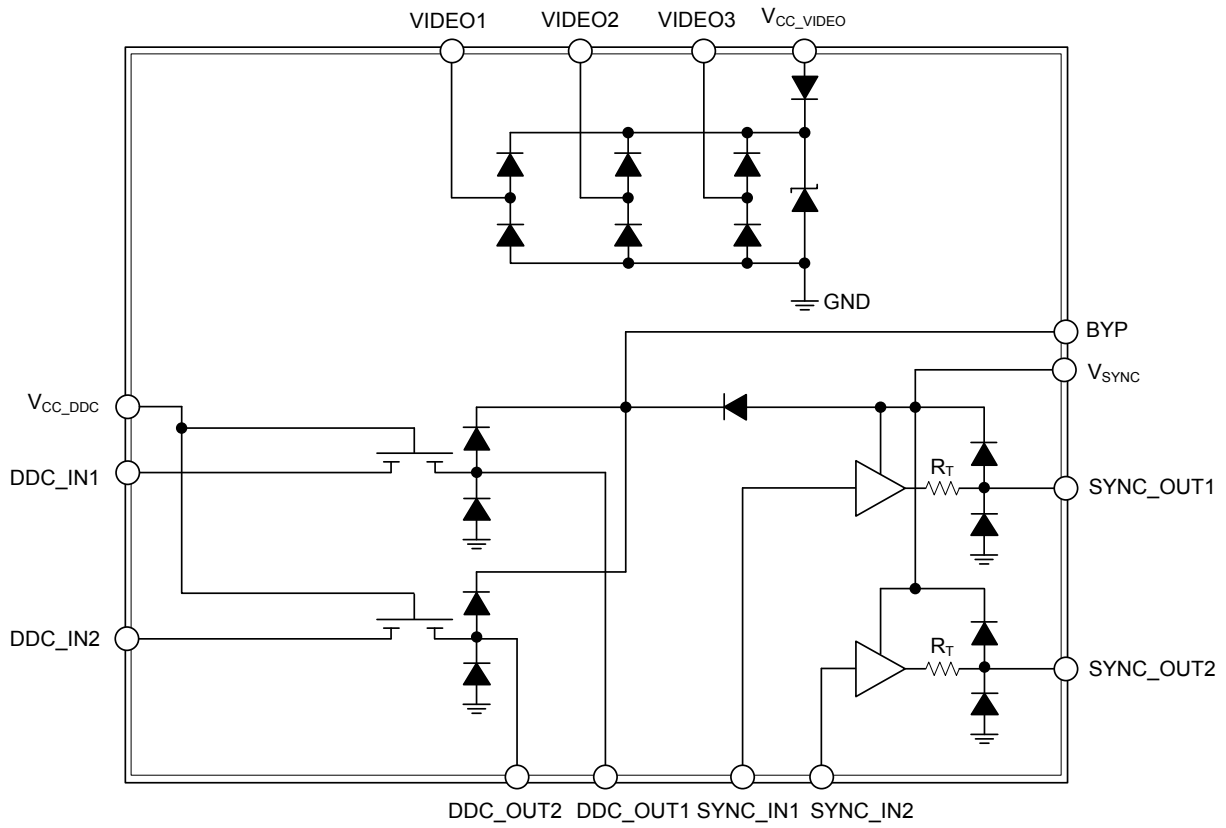
■ **ABSOLUTE MAXIMUM RATING** over operating free-air temperature range (unless otherwise noted)

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage		V_{CC_VIDEO}, V_{CC_DDC}, V_{CC_SYNC}	-0.5~6.0	V
IO Voltage	VIDEOx Pins	$V_{IO(VIDEO)}$	-0.5~V_{CC_VIDEO}	V
Input Voltage	SYNC Pins	$V_{I(SYNC)}$	-0.5~V_{CC_SYNC}	V
Input Voltage	DDC_INx Pins	$V_{I(DDC)}$	-0.5~6.0	V
Output Voltage	DDC_INx Pins	$V_{O(DDC)}$	-0.5~6.0	V
IEC 61000-4-2 Contact Discharge	VIDEO, DDC_OUT, SYNC_OUT Pins		±8	kV
HBM ESD	VIDEO, DDC_OUT, SYNC_OUT Pins		±15	kV
	VCC, DDC_IN, SYNC_IN, BYP Pins		±2	kV
Storage Temperature		T_{STG}	-55~125	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ **RECOMMENDED OPERATING CONDITIONS**

over operating free-air temperature range (unless otherwise noted)

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage		V_{CC_VIDEO}, V_{CC_DDC}, V_{CC_SYNC}	0		5.5	V
IO Voltage	VIDEOx Pins	$V_{IO(VIDEO)}$	0		V_{CC_VIDEO}	V
Input Voltage	SYNC Pins	$V_{I(SYNC)}$	0		V_{CC_SYNC}	V
Input Voltage	DDC_INx Pins	$V_{I(DDC)}$	0		5.5	V
Output Voltage	DDC_INx Pins	$V_{O(DDC)}$	0		5.5	V
Operating temperature		T_A	-40		85	°C

■ **ELECTRICAL CHARACTERISTICS**

over operating free-air temperature range (unless otherwise noted)

PARAMETER		SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{CC_VIDEO} Supply Current		I_{CC_VIDEO}	V_{CC_VIDEO}=5V, VIDEO Inputs at V_{CC_VIDEO} or GND			1	10	µA
V_{CC_DDC} Supply Current		I_{CC_DDC}	V_{CC_DDC}=5V			1	10	µA
V_{CC_SYNC} Supply Current		I_{CC_SYNC}	V_{CC_SYNC}=5V,	SYNC Inputs at GND or V_{CC_SYNC}, SYNC Outputs Unloaded		1	50	µA
				SYNC Inputs at 3V; SYNC Outputs Unloaded			2.0	mA
VIDEO Input/Output Pins		I_{IO_VIDEO}	V_{IO_VIDEO}=3V			0.01	1.0	µA
DDC Pin Power Down Leakage Current		I_{OFF}	V_{CC_DDC}≤0.4V, V_{DDC_OUT}=5V			0.01	1.0	µA
Diode Forward Voltage for Lower Clamp of VIDEO, DDC, SYNC Output Pins		V_D	I_D=8mA, Lower Clamp Diode		-0.6	-0.8	-0.95	V
Dynamic Resistance (VIDEO Pins)		R_{DYN_VIDEO}	I=1A			1.0		Ω
High-Level SYNC Logic Input Voltage		V_{IH}	V_{CC_SYNC}=5V		2.0			V
Low-Level SYNC Logic Input Voltage		V_{IL}	V_{CC_SYNC}=5V				0.6	V
High-Level SYNC Logic Output Voltage		V_{OH}	I_{OH}=0mA, V_{CC_SYNC}=5V		4.85			V
High-Level SYNC Logic Output Voltage	VGA7S019-15	V_{OH-15}	I_{OH}=24mA, V_{CC_SYNC}=5V		2			V
Low-Level SYNC Logic Output Voltage		V_{OL}	I_{OH}=0mA, V_{CC_SYNC}=5V				0.15	V
Low-Level SYNC Logic Output Voltage	VGA7S019-15	V_{OL-15}	I_{OH}=24mA, V_{CC_SYNC}=5V				0.8	V
SYNC Driver Output Resistance	VGA7S019-15	R_T	V_{CC_SYNC}=5V, SYNC Inputs at GND or 3V			15		Ω
	VGA7S019-55					55		Ω
	VGA7S019-65					65		Ω
IO Capacitance of VIDEO Pins		C_{IO_VIDEO}	V_{IO}=2.5V			2.5	4	pF
SYNC Driver L =>H Propagation Delay		t_{PLH}	C_L=50pF; V_{CC}=5V, input t_R and t_F≤5ns				12	ns
SYNC Driver H =>L Propagation Delay		t_{PHL}	C_L=50pF; V_{CC}=5V, input t_R and t_F≤5ns				12	ns
SYNC Driver Output Rise & Fall Times		t_R, t_F	C_L=50pF; V_{CC}=5V, input t_R and t_F≤5ns			4		ns
VIDEO ESD Diode Break-Down Voltage		V_{BR}	I_{IO}=1mA		9			V

■ **TYPICAL APPLICATION CIRCUIT**
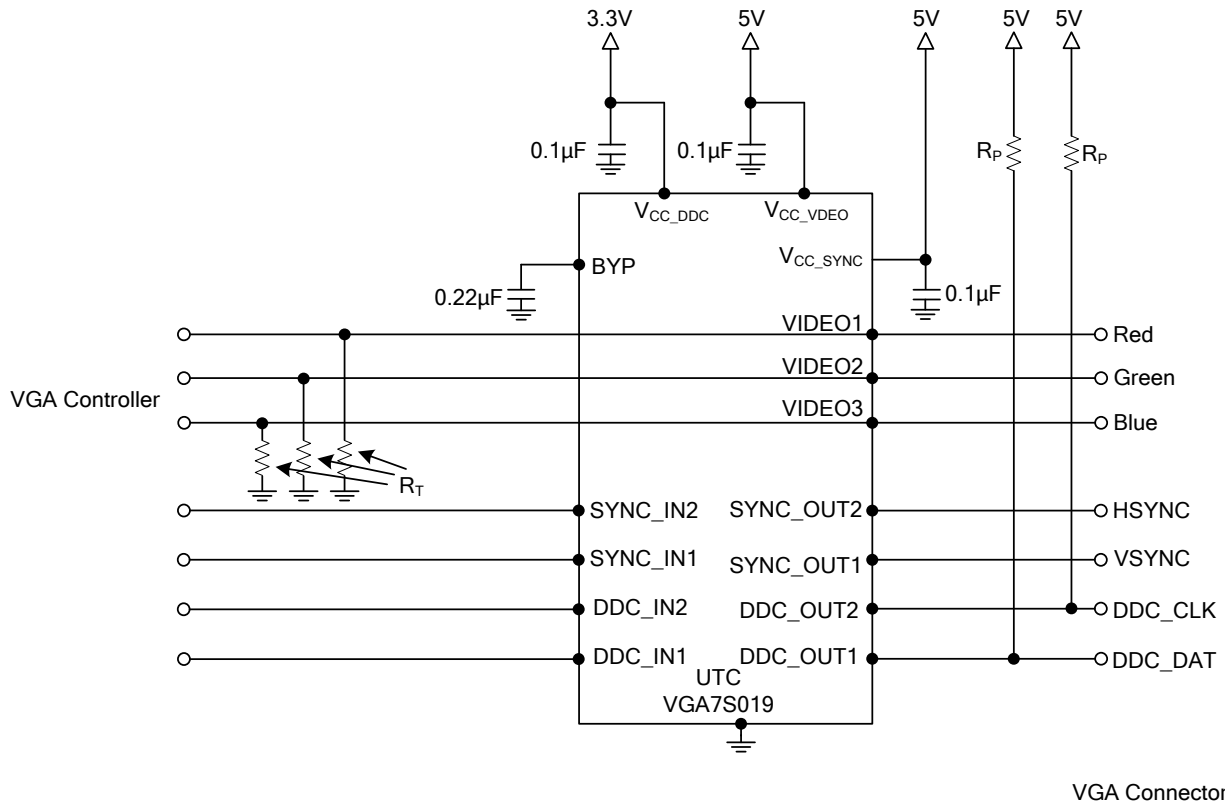
R_P: Pullup resistor for the DDC data and clock lines. Typically system designer selects 47kΩ pullup values

R_T: Line termination resistor for the RGB lines. RT is selected to match the transmission line. For a single-ended transmission line, RT can be anywhere from 50Ω to 75Ω depending on board trace impedance.

Some systems may require additional filters at the SYNC and RGB lines.

The UTC **VGA7S019** should be placed as close to the VGA port as possible.

The ESD protection channels VIDEO1, VIDEO2, VIDEO3 are identical circuits, they can be used interchangeably between the R, G, B signals.