Product Specification

PE97632

3.5 GHz Delta-Sigma modulated Fractional-N Frequency Synthesizer for Low Phase Noise Applications

Features

- 3.5 GHz operation
- ÷10/11 dual modulus prescaler
- Phase detector output
- Serial or direct hardwired mode
- Frequency selectivity: Comparison frequency / 2^{18}
- Low power - 40 mA at 3.3 V
- Rad-Hard
- Ultra-low phase noise
- 68-lead CQFJ
- Pin compatible with the PE9763 *(reference application note AN24 at www.psemi.com)*

Product Description

Peregrine's PE97632 is a high performance fractional-N PLL capable of frequency synthesis up to 3.5 GHz. The device is designed for superior phase noise performance while providing an order of magnitude reduction in current consumption, when compared with existing commercial space PLLs.

The PE97632 features a ÷10/11 dual modulus prescaler, counters, a delta sigma modulator, and a phase comparator as shown in *Figure 1*. Counter values are programmable through a serial or direct hardwired mode.

The PE97632 is optimized for commercial space applications. Single Event Latch up (SEL) is physically impossible and Single Event Upset (SEU) is better than 10^{-9} errors per bit / day. Fabricated in Peregrine's patented UltraCMOS™ technology, the PE97632 offers excellent RF performance and intrinsic radiation tolerance.

Figure 1. Block Diagram

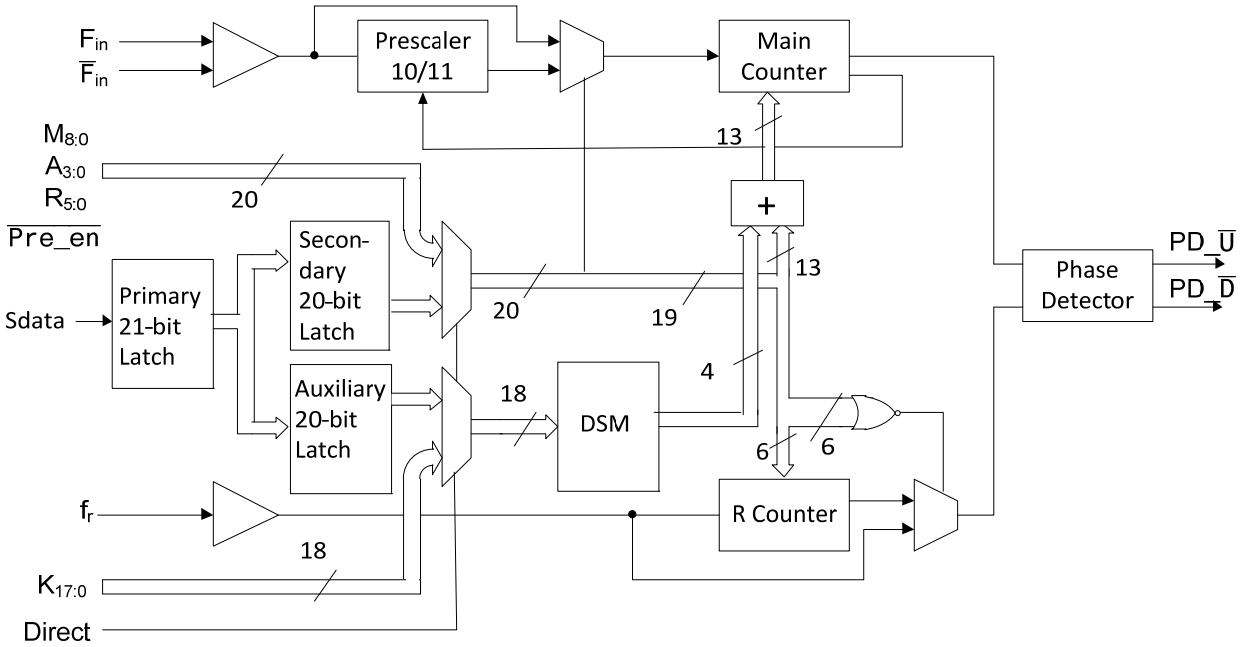


Figure 2. Pin Configurations (Top View)

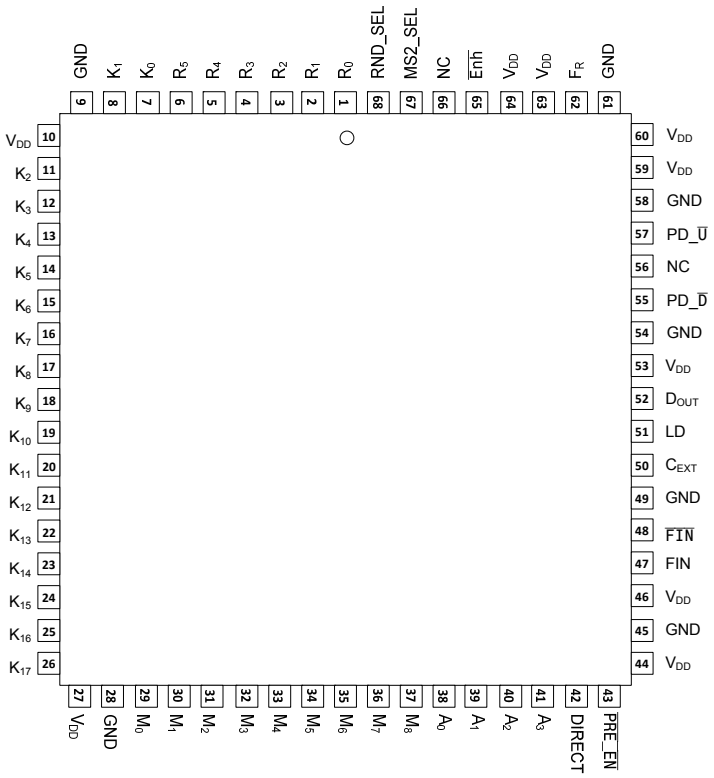


Figure 3. Package Type

68-lead CQFJ

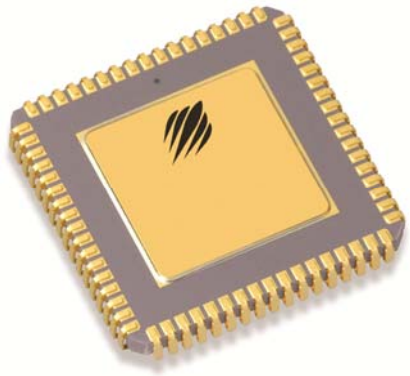


Table 1. Pin Descriptions

Pin No.	Pin Name	Valid Mode	Type	Description
1	R_0	Direct	Input	R Counter bit0 (LSB).
2	R_1	Direct	Input	R Counter bit1.
3	R_2	Direct	Input	R Counter bit2.
4	R_3	Direct	Input	R Counter bit3.
5	R_4	Direct	Input	R Counter bit4.
6	R_5	Direct	Input	R Counter bit5 (MSB).
7	K_0	Direct	Input	K Counter bit0 (LSB).
8	K_1	Direct	Input	K Counter bit1.
9	GND		Downbond	Ground
10	V_{DD}		(Note 1)	Digital core V_{DD}.
11	K_2	Direct	Input	K Counter bit2.
12	K_3	Direct	Input	K Counter bit3.
13	K_4	Direct	Input	K Counter bit4.
14	K_5	Direct	Input	K Counter bit5.
15	K_6	Direct	Input	K Counter bit6.

Pin No.	Pin Name	Valid Mode	Type	Description
16	K_7	Direct	Input	K Counter bit7.
17	K_8	Direct	Input	K Counter bit8.
18	K_9	Direct	Input	K Counter bit9.
19	K_{10}	Direct	Input	K Counter bit10.
20	K_{11}	Direct	Input	K Counter bit11.
21	K_{12}	Direct	Input	K Counter bit12.
22	K_{13}	Direct	Input	K Counter bit13.
23	K_{14}	Direct	Input	K Counter bit14.
24	K_{15}	Direct	Input	K Counter bit15.
25	K_{16}	Direct	Input	K Counter bit16.
26	K_{17}	Direct	Input	K Counter bit17 (MSB).
27	V_{DD}		(Note 1)	Digital core V_{DD}.
28	GND		Downbond	Ground
29	M_0	Direct	Input	M Counter bit0 (LSB).
30	M_1	Direct	Input	M Counter bit1.
31	M_2	Direct	Input	M Counter bit2
32	M_3	Direct	Input	M Counter bit3.
33	M_4	Direct	Input	M Counter bit4.
	S_WR	Serial	Input	Serial load enable input. While S_WR is “low”, Sdata can be serially clocked. Primary register data are transferred to the secondary register on S_WR rising edge.
34	M_5	Direct	Input	M Counter bit5.
	SDATA	Serial	Input	Binary serial data input. Input data entered MSB first.
35	M_6	Direct	Input	M Counter bit6.
	SCLK	Serial	Input	Serial clock input. SDATA is clocked serially into the 21-bit primary register (E_WR “low”) or the 8-bit enhancement register (E_WR “high”) on the rising edge of Sclk.
36	M_7	Direct	Input	M Counter bit7.
37	M_8	Direct	Input	M Counter bit8 (MSB).
38	A_0	Direct	Input	A Counter bit0 (LSB).
39	A_1	Direct	Input	A Counter bit1.
	E_WR	Serial	Input	Enhancement register write enable. While E_WR is “high”, Sdata can be serially clocked into the enhancement register on the rising edge of Sclk.
40	A_2	Direct	Input	A Counter bit2.
41	A_3	Direct	Input	A Counter bit3 (MSB).
42	DIRECT	Both	Input	Direct mode select. “High” enables direct mode. “Low” enables serial mode.
43	$\overline{\text{Pre\_en}}$	Direct	Input	Prescaler enable, active “low”. When “high”, Fin bypasses the prescaler.
44	V_{DD}		(Note 1)	Digital core V_{DD}.
45	GND		Downbond	Ground

Pin No.	Pin Name	Valid Mode	Type	Description
46	V_{DD}		(Note 1)	Prescaler V_{DD}.
47	F_{in}	Both	Input	Prescaler input from the VCO, 3.5 GHz max frequency. A 22 pF coupling capacitor should be placed as close as possible to this pin and terminated with a 50 Ω resistor to ground.
48	$\overline{F}_{in}$	Both	Input	Prescaler complementary input. A 22pF bypass capacitor should be placed as close as possible to this pin and be connected in series with a 50 Ω resistor to ground.
49	GND		Downbond	Ground
50	CEXT	Both	Output	Logical “NAND” of PD_$\overline{U}$ and PD_$\overline{D}$ terminated through an on chip, 2 kΩ series resistor. Connecting Cext to an external capacitor will low pass filter the input to the inverting amplifier used for driving LD.
51	LD	Both	Output	Lock detect and open drain logical inversion of CEXT. When the loop is in lock, LD is high impedance, otherwise LD is a logic low (“0”).
52	D_{OUT}	Both	Output	Data out function, enabled in enhancement mode.
53	V_{DD}		(Note 1)	Output driver/V_{DD}.
54	GND		Downbond	Ground
55	PD_$\overline{D}$	Both	Output	PD_$\overline{D}$ pulses down when f_p leads f_c.
56	NC	Both	(Note 3)	No Connect
57	PD_$\overline{U}$	Both	Output	PD_$\overline{U}$ pulses down when f_c leads f_p.
58	GND		Downbond	Ground
59	V_{DD}		(Note 1)	Output driver/V_{DD}.
60	V_{DD}		(Note 1)	Phase detector V_{DD}.
61	GND		Downbond	Ground
62	f_r	Both	Input	Reference frequency input.
63	V_{DD}		(Note 1)	Reference V_{DD}.
64	V_{DD}		(Note 1)	Digital core V_{DD}.
	GND		Downbond	Ground
65	$\overline{Enh}$	Both	Input	Enhancement mode. When asserted low (“0”), enhancement register bits are functional.
66	NC	Both	(Note 3)	No Connect
67	MS2_SEL	Both	Input	MASH 1-1 select. “High” selects MASH 1-1 mode. “Low” selects the MASH 1-1-1 mode.
68	RND_SEL	Both	Input	K register LSB toggle enable. “1” enables the toggling of LSB. This is equivalent to having an additional bit for the LSB of K register. The frequency offset as a result of enabling this bit is the phase detector comparison frequency / 2^{19}.

Notes 1. All V_{DD} pins are connected by diodes and must be supplied with the same positive voltage level.
2. All digital input pins have 70 kΩ pull-down resistors to ground.
3. No Connect pins can be left open or floating.

Table 2. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Supply voltage	-0.3	4.0	V
V_I	Voltage on any input	-0.3	V_{DD} + 0.3	V
I_I	DC into any input	-10	+10	mA
I_O	DC into any output	-10	+10	mA
θ_{JC}	Theta JC		12	°C/W
T_{stg}	Storage temperature range	-65	150	°C

Table 3. Operating Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Supply voltage	2.85	3.45	V
T_A	Operating ambient temperature range	-40	85	°C

Table 4. ESD Ratings

Symbol	Parameter/Conditions	Level	Units
V_{ESD}	ESD Voltage Human Body Model on all pins except pin 52[1]	1000	V
	ESD Voltage Human Body Model on pin 52[1,2]	300	V

Notes 1. Periodically sampled, not 100% tested. Tested per MIL-STD-883, M3015 C2.
2. Pin 52 is a test pin only. It is not used in normal operation.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in *Table 4*.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Table 5. DC Characteristics: V_{DD} = 3.30 V -40 °C < TA < 85 °C, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD}	Operational supply current;	V_{DD} = 2.85 to 3.45 V				
	Prescaler enabled			40		mA
I_{DD}	Operational supply current;	V_{DD} = 2.85 to 3.45 V		15		mA
	Prescaler disabled					
All Digital inputs: K[17:0], R[5:0], M[8:0], A[3:0], Direct, $\overline{Pre\_en}$, RND_SEL, MS2_SEL, $\overline{Enh}$ (contains a 70 kΩ pull-down resistor)						
V_{IH}	High level input voltage	V_{DD} = 2.85 to 3.45 V	0.7 x V_{DD}			V
V_{IL}	Low level input voltage	V_{DD} = 2.85 to 3.45 V			0.3 x V_{DD}	V
I_{IH}	High level input current	V_{IH} = V_{DD} = 3.45 V			100	µA
I_{IL}	Low level input current	V_{IL} = 0, V_{DD} = 3.45 V	-1			µA
Reference Divider input: f_r						
I_{IHR}	High level input current	V_{IH} = V_{DD} = 3.45 V			100	µA
I_{ILR}	Low level input current	V_{IL} = 0, V_{DD} = 3.45 V	-100			µA
Counter and phase detector outputs: PD_$\overline{D}$, PD_$\overline{U}$						
V_{OLD}	Output voltage LOW	I_{out} = 6 mA			0.4	V
V_{OHD}	Output voltage HIGH	I_{out} = -3 mA	V_{DD} - 0.4			V
Digital test outputs: Dout						
V_{OLD}	Output voltage LOW	I_{out} = 200 µA			0.4	V
V_{OHD}	Output voltage HIGH	I_{out} = -200 µA	V_{DD} - 0.4			V
Lock detect outputs: (Cext, LD)						
V_{OLC}	Output voltage LOW, Cext	I_{out} = 0.1 mA			0.4	V
V_{OHC}	Output voltage HIGH, Cext	I_{out} = -0.1 mA	V_{DD} - 0.4			V
V_{OLLD}	Output voltage LOW, LD	I_{out} = 1 mA			0.4	V

Table 6. AC Characteristics

V_{DD} = 3.30 V -40 °C < TA < 85 °C, Unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Control Interface and Latches (see *Figure 10*)						
f_{Clk}	Serial data clock frequency	(Note 1)			10	MHz
t_{ClkH}	Serial clock HIGH time		30			ns
t_{ClkL}	Serial clock LOW time		30			ns
t_{DSU}	Sdata set-up time to Sclk rising edge		10			ns
t_{DHLD}	Sdata hold time after Sclk rising edge		10			ns
t_{PW}	S_WR pulse width		30			ns
t_{CWR}	Sclk rising edge to S_WR rising edge		30			ns
t_{CE}	Sclk falling edge to E_WR transition		30			ns
t_{WRC}	S_WR falling edge to Sclk rising edge		30			ns
t_{EC}	E_WR transition to Sclk rising edge		30			ns
Main Divider (Prescaler Enabled)[4]						
P_{Fin}	Input level range	External AC coupling 275 MHz ≤ Freq ≤ 3200 MHz	-5		5	dBm
		External AC coupling 3.2 GHz < Freq ≤ 3.5 GHz 3.15 V ≤ V_{DD} ≤ 3.45 V	0		5	dBm
Main Divider (Prescaler Bypassed)[4]						
F_{in}	Operating frequency		50		300	MHz
P_{Fin}	Input level range	External AC coupling	-5		5	dBm
Reference Divider						
f_r	Operating frequency	(Note 3)			100	MHz
P_{fr}	Reference input power[2]	Single ended input	-2			dBm
Phase Detector						
f_c	Comparison frequency	(Note 3)			50	MHz
SSB Phase Noise (F_{in} = 1.9 GHz, f_r = 20 MHz, f_c = 20 MHz, LBW = 50 kHz, V_{DD} = 3.3 V, Temp = 25 °C)[4]						
Φ_N	Phase Noise	100 Hz Offset		-89		dBc/Hz
Φ_N	Phase Noise	1 kHz Offset		-96		dBc/Hz
Φ_N	Phase Noise	10 kHz Offset		-101		dBc/Hz
SSB Phase Noise (F_{in} = 1.9 GHz, f_r = 20 MHz, f_c = 20 MHz, LBW = 50 kHz, V_{DD} = 3.0 V, Temp = 25 °C)[4]						
Φ_N	Phase Noise	100 Hz Offset		-84		dBc/Hz
Φ_N	Phase Noise	1 kHz Offset		-92		dBc/Hz
Φ_N	Phase Noise	10 kHz Offset		-100		dBc/Hz

Notes: 1. f_{Clk} is verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10 MHz to verify f_{Clk} specification.
2. CMOS logic levels can be used to drive the reference input. If the V_{DD} of the CMOS driver matches the V_{DD} of the PLL IC, then the reference input can be DC coupled. Otherwise, the reference input should be AC coupled. For Sin wave inputs, the minimum amplitude needs to be 0.5Vpp. The maximum level should be limited to prevent ESD diodes at the pin input from turning on. Diodes will turn on at one forward-bias diode drop above VDD or below GND. The DC voltage at the Reference input is V_{DD}/2.
3. Parameter is guaranteed through characterization only and is not tested.
4. Parameter below are not tested for die sales. These parameters are verified during the element

Figure 4. Typical Spurious Plot

Test Conditions: MASH 1-1 mode. F_{OUT} = 1.9204 GHz, $f_{COMPARISON}$ = 20 MHz, Frequency Step = 400 KHz, V_{DD} = 3.3 V, Temp = 25C , Loop Bandwidth = 50 kHz.

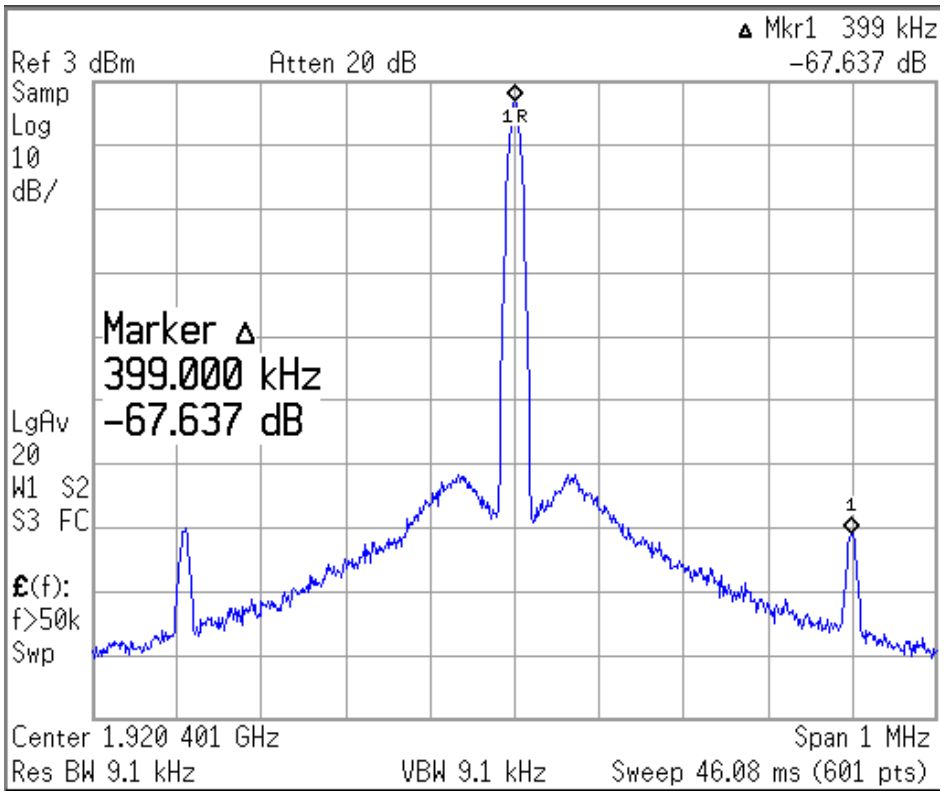


Figure 5. RF Sensitivity versus Frequency (typical device at temperature = 25 °C)

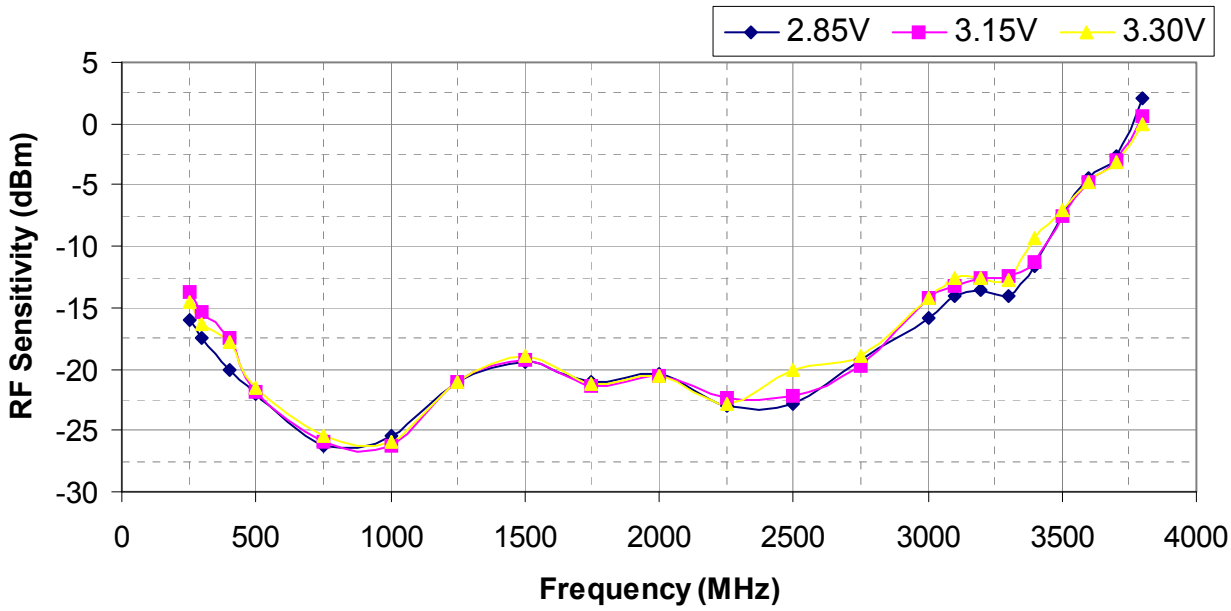


Figure 6. Equivalent Input Diagram: Reference Input

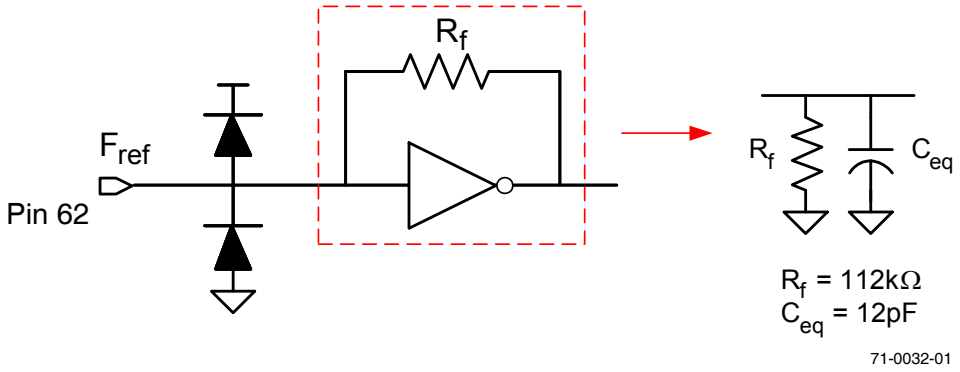


Figure 7. Equivalent Input Diagram: Main Input

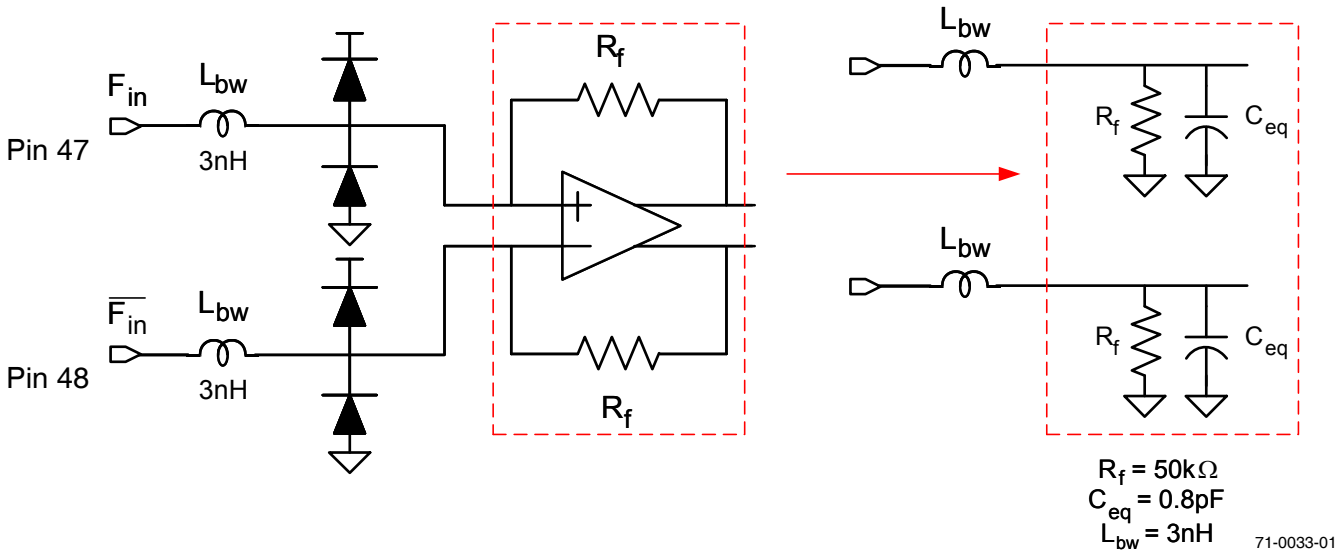
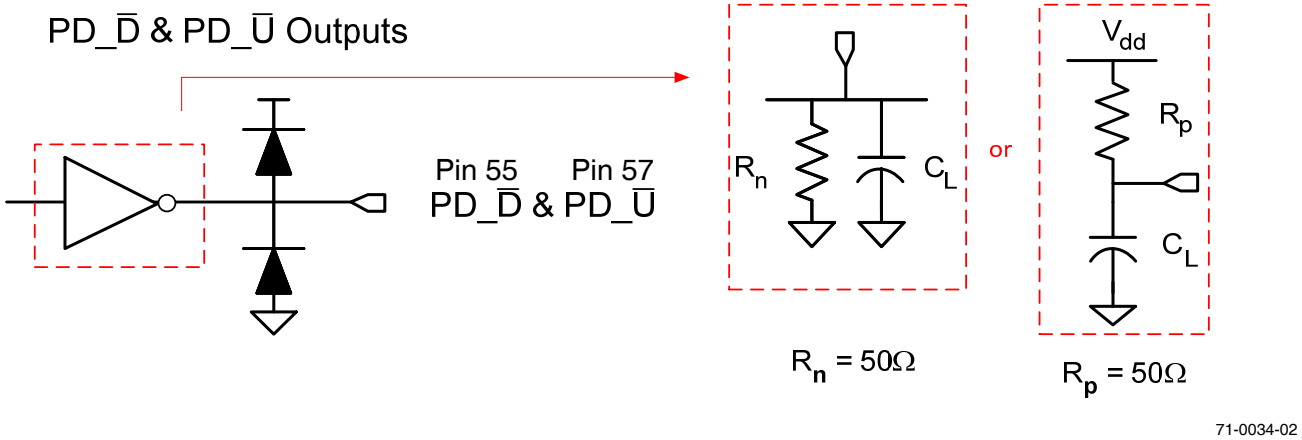


Figure 8. Equivalent Output Diagram: PD_D̄ & PD_Ū Outputs

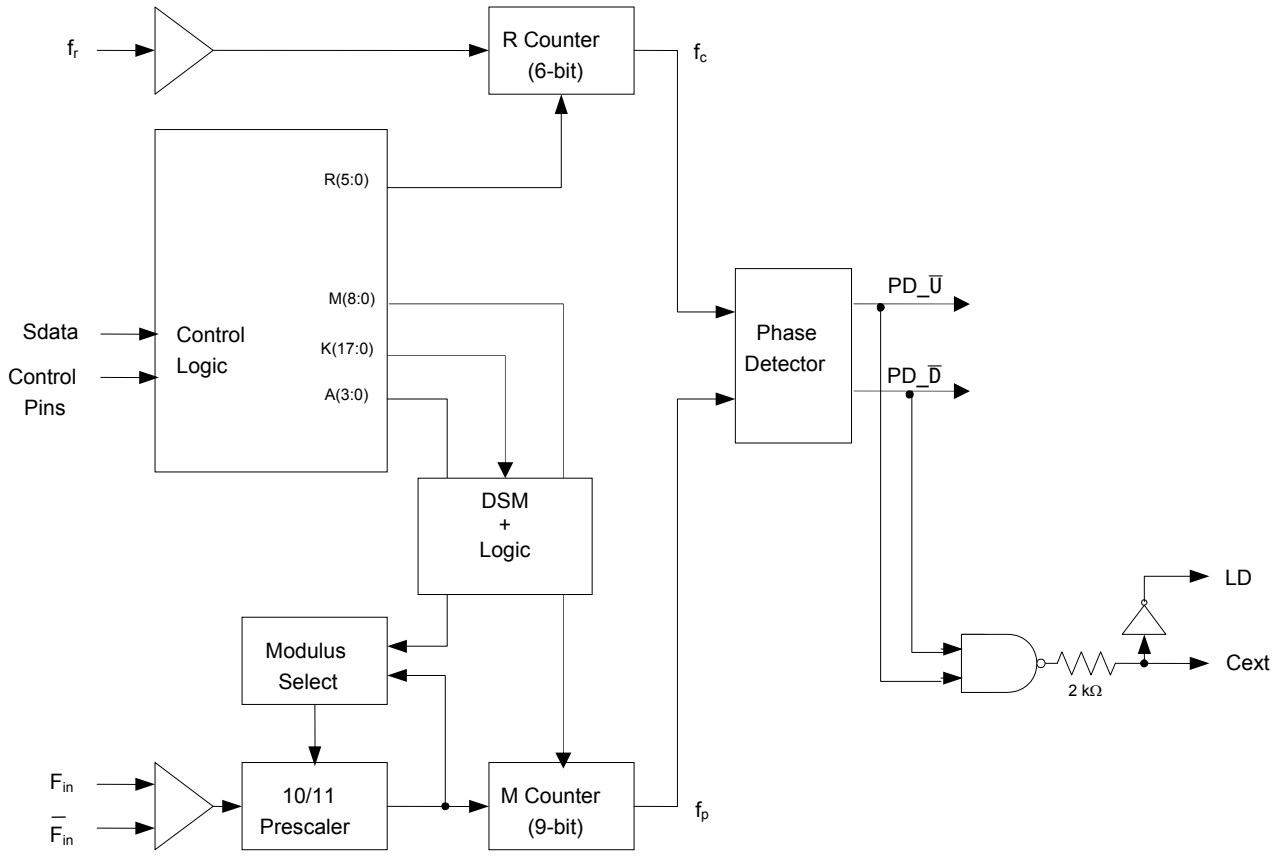


Functional Description

The PE97632 consists of a prescaler, counters, an 18-bit delta-sigma modulator (DSM) and a phase detector. The dual modulus prescaler divides the VCO frequency by either 10 or 11, depending on the value of the modulus select. Counters “R” and “M” divide the reference and prescaler output, respectively, by integer values stored in a 20-bit register. An additional counter (“A”) is used in the modulus select logic. The DSM modulates the “A” counter outputs in order to achieve the desired fractional step.

The phase-frequency detector generates up and down frequency control signals. Data is written into the internal registers via the three wire serial bus. There are also various operational and test modes and a lock detect output.

Figure 9. Functional Block Diagram



Main Counter Chain

Normal Operating Mode

The PE97632 can be operated in Integer-N mode or either Fractional-N mode. The main counter chain divides the RF input frequency (Fin) by an integer or fractional number derived from the values in the "M", "A" counters and the DSM input word K. Setting the $\overline{\text{Pre\_en}}$ control bit "high" operates the part only in Integer-N mode. In addition, even if $\overline{\text{Pre\_en}}$ is "low" if K=0 the part is operated in Integer-N mode.

The Fractional-N modes use a MASH (**M**ulti-st**A**ge noise **SH**aping) decimation structure. The MS2_SEL pin sets the MASH mode.

MASH-1-1 mode is a 2nd order fractional dithering using four (2^2) N values: N-1, N, N+1, N+2.

MASH 1-1-1 mode is a 3rd order fractional dithering using eight (2^3) N values: N-3, N-2, N-1, N, N+1, N+2, N+3, N+4.

Using the part in MASH-1-1 or MASH-1-1-1 mode will yield spurs at frequency offsets equal to

Fspur =

$$\pm[(2K + RND\_SEL)/(2^{19})] \times f_c \qquad 1 \le K \le 131072 \qquad (1)$$

$$\pm[1-(2K + RND\_SEL)/(2^{19})] \times f_c \qquad 131073 \le K \le 262143$$

where f_c is the Phase Detector (comparison) frequency, K is the DSM input word, and RND_SEL is the K register LSB toggle enable.

MASH-1-1-1 mode reduces these spurs for an increase in the phase noise and a decrease in the number of valid programming frequencies.

The 18-bit DSM accumulator fixes the fractional value of N from the ratio $K/2^{18}$ and the frequency step size as $f_c/2^{18}$. There is an additional bit in the DSM that acts like an extra bit (19th bit). This bit is enabled by asserting the pin RND_SEL to "high". Enabling this bit has the benefit of reducing the spur levels. This is especially beneficial for large K-counter values that do not use any lower bits, causing an accumulation of random values in these bits and additional spurs.

The side effect of asserting RND_SEL is that a small frequency offset will occur. This positive frequency offset is calculated with the following equation:

$$f_{offset} = (f_r / (R + 1)) / 2^{19} \qquad (2)$$

All of the following equations do not take into account this frequency offset. If this offset is important to a specific frequency plan, it should be taken into account accordingly.

In addition, K-counter values at the minimum, maximum and midpoint have higher spur levels that may not be reduced by enabling RND_SEL. If the PD comparison frequency is slightly shifted, the K value can be experimented with to move away from the suboptimal values.

During normal operation, the output from the main counter chain (f_p) is related to the VCO frequency (F_{in}) by the following equation:

$$f_p = F_{in} / N \qquad (3)$$

where

$$N = 10 \times (M+1) + A + (2K + RND\_SEL)/2^{19}$$

$$A \le M + 1,\ 1 \le M \le 511$$

When the loop is locked, F_{in} is related to the reference frequency (f_r) by the following equation:

$$F_{in} = N \times (f_r / (R+1)) \qquad (4)$$

where

$$N = 10 \times (M+1) + A + (2K + RND\_SEL)/2^{19}$$

$$A \le M + 1,\ 1 \le M \le 511$$

A consequence of the upper limit on A is that:

In Integer-N mode, F_{in} must be ≥ 90 x (f_r / (R+1)) to obtain contiguous channels.

In MASH-1-1 mode, F_{in} must be ≥ 91 x (f_r / (R+1)) to obtain contiguous channels.

In MASH-1-1-1 mode, F_{in} must be ≥ 93 x (f_r / (R+1)) to obtain contiguous channels.

The A counter can accept values as high as 15, but in typical operation it will cycle from 0 to 9 in increments of M. Programming the M counter with the minimum allowed value of "1" will result in a minimum M counter divide ratio of "2".

Prescaler Bypass Mode (*)

Setting the frequency control register bit $\overline{\texttt{Pre\_en}}$ "high" allows F_{in} to bypass the ÷10/11 prescaler. In this mode, the prescaler and A counter are powered down, and the input VCO frequency is divided by the M counter directly. The following equation relates F_{in} to the reference frequency f_r:

$$\mathbf{F_{in} = (M + 1) \times (f_r / (R+1))} \qquad \mathbf{(5)}$$

where $1 \leq M \leq 511$

(*) Only Integer-N mode

In frequency bypass mode, neither A counter or K counter is used. Therefore, only Integer-N operation is possible.

Reference Counter

The reference counter chain divides the reference frequency f_r down to the phase detector comparison frequency f_c.

The output frequency of the 6-bit R Counter is related to the reference frequency by the following equation:

$$\mathbf{f_c = f_r / (R + 1)} \qquad \mathbf{(6)}$$

where $0 \leq R \leq 63$

Note that programming R with "0" will pass the reference frequency (f_r) directly to the phase detector.

Register Programming

Serial Interface Mode

While the E_WR input is "low" and the S_WR input is "low", serial input data (Sdata input), B_0 to B_{20}, are clocked serially into the primary register on the rising edge of Sclk, MSB (B_0) first. The LSB is used as an address bit. When "0", the contents from the primary register are transferred into the secondary register on the rising edge of either S_WR according to the timing diagrams shown in *Figure 10*. When "1", data is transferred to the auxiliary register according to the same timing diagram. The secondary register is used to program the various counters, while the auxiliary register is used to program the DSM.

Data are transferred to the counters as shown in *Table 8*.

While the E_WR input is "high" and the S_WR input is "low", serial input data (Sdata input), B_0 to B_7, are clocked serially into the enhancement register on the rising edge of Sclk, MSB (B_0) first. The enhancement register is double buffered to prevent inadvertent control changes during serial loading, with buffer capture of the serially entered data performed on the falling edge of E_WR according to the timing diagram shown in *Figure 10*. After the falling edge of E_WR, the data provide control bits as shown in *Table 9* on page 10 will have their bit functionality enabled by asserting the $\overline{\text{Enh}}$ input "low".

Direct Interface Mode

Direct Interface Mode is selected by setting the "Direct" input "high".

Counter control bits are set directly at the pins as shown in *Table 7* and *Table 8*.

Table 7. Secondary Register Programming

Interface Mode	$\overline{\text{Enh}}$	R_5	R_4	M_8	M_7	$\overline{\text{Pre\_en}}$	M_6	M_5	M_4	M_3	M_2	M_1	M_0	R_3	R_2	R_1	R_0	A_3	A_2	A_1	A_0	Addr
Direct	1	R_5	R_4	M_8	M_7	$\overline{\text{Pre\_en}}$	M_6	M_5	M_4	M_3	M_2	M_1	M_0	R_3	R_2	R_1	R_0	A_3	A_2	A_1	A_0	X
Serial*	1	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	B_9	B_{10}	B_{11}	B_{12}	B_{13}	B_{14}	B_{15}	B_{16}	B_{17}	B_{18}	B_{19}	0

*Serial data clocked serially on Sclk rising edge while E_WR "low" and captured in secondary register on S_WR rising edge.

↑ MSB (first in)

(last in) LSB ↑

Table 8. Auxiliary Register Programming

Interface Mode	$\overline{\text{Enh}}$	K_{17}	K_{16}	K_{15}	K_{14}	K_{13}	K_{12}	K_{11}	K_{10}	K_9	K_8	K_7	K_6	K_5	K_4	K_3	K_2	K_1	K_0	Rsrv	Rsrv	Addr
Direct	1	K_{17}	K_{16}	K_{15}	K_{14}	K_{13}	K_{12}	K_{11}	K_{10}	K_9	K_8	K_7	K_6	K_5	K_4	K_3	K_2	K_1	K_0	X	X	X
Serial*	1	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	B_9	B_{10}	B_{11}	B_{12}	B_{13}	B_{14}	B_{15}	B_{16}	B_{17}	B_{18}	B_{19}	1

*Serial data clocked serially on Sclk rising edge while E_WR "low" and captured in secondary register on S_WR rising edge.

↑ MSB (first in)

(last in) LSB ↑

Table 9. Enhancement Register Programming

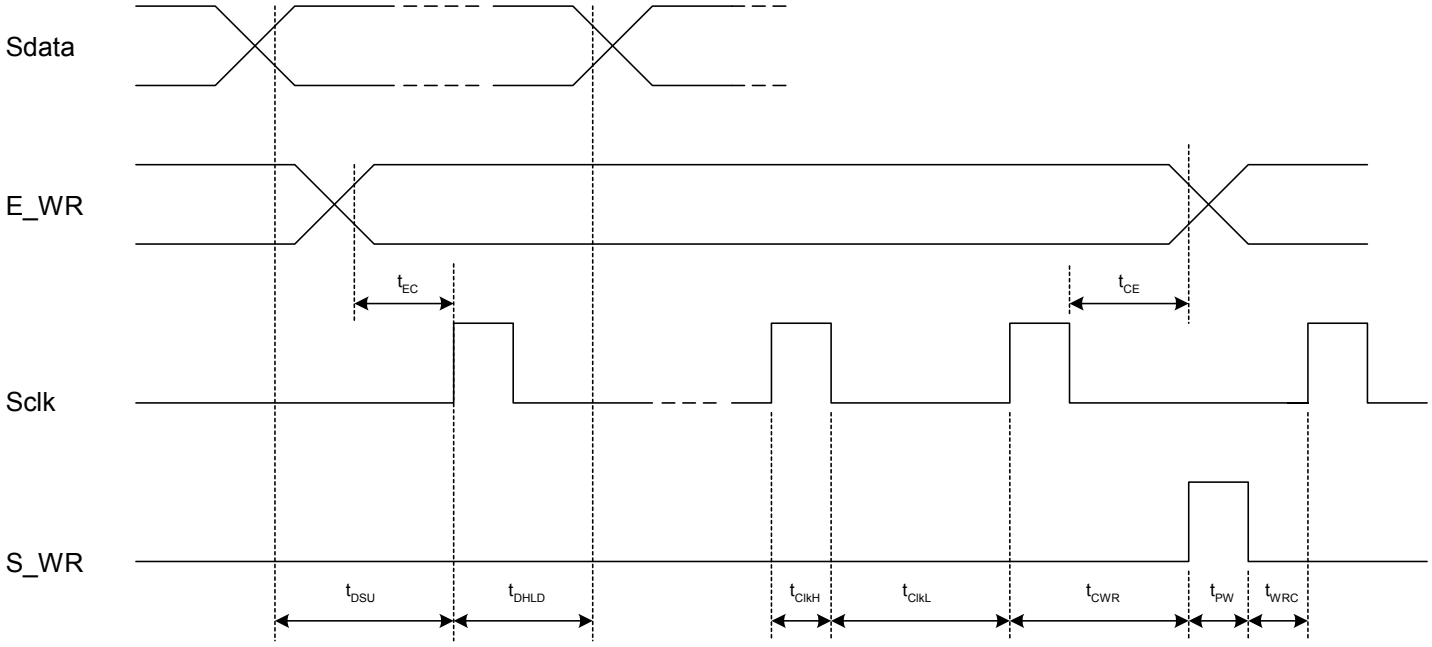
Interface Mode	$\overline{\text{Enh}}$	Reserved	Reserved	f_p output	Power Down	Counter load	MSEL output	f_c output	LD Disable
Serial*	0	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7

*Serial data clocked serially on Sclk rising edge while E_WR "high" and captured in the double buffer on E_WR falling edge.

↑ MSB (first in)

(last in) LSB ↑

Figure 10. Serial Interface Mode Timing Diagram



Enhancement Register

The functions of the enhancement register bits are shown below with all bits active “high”.

Table 10. Enhancement Register Bit Functionality

Bit Function		Description
Bit 0	Reserve **	Reserved.
Bit 1	Reserve **	Reserved.
Bit 2	f_p output	Drives the M counter output onto the Dout output.
Bit 3	Power down	Power down of all functions except programming interface.
Bit 4	Counter load	Immediate and continuous load of counter programming.
Bit 5	MSEL output	Drives the internal dual modulus prescaler modulus select (MSEL) onto the Dout output.
Bit 6	f_c output	Drives the reference counter output onto the Dout output.
Bit 7	LD Disable	Disables the LD pin for quieter operation.

** Program to 0

Phase Detector

The phase detector is triggered by rising edges from the main Counter (f_p) and the reference counter (f_c). It has two outputs, namely PD_$\overline{U}$, and PD_$\overline{D}$. If the divided VCO leads the divided reference in phase or frequency (f_p leads f_c), PD_$\overline{D}$ pulses "low". If the divided reference leads the divided VCO in phase or frequency (f_c leads f_p), PD_$\overline{U}$ pulses "low". The width of either pulse is directly proportional to phase offset between the two input signals, f_p and f_c.

For the UP and DOWN mode, PD_$\overline{U}$ and PD_$\overline{D}$ drive an active loop filter which controls the VCO tune voltage. The phase detector gain is equal to VDD / 2 π.

PD_$\overline{U}$ pulses cause an increase in VCO frequency and PD_$\overline{D}$ pulses cause a decrease in VCO frequency, for a positive Kv VCO.

A lock detect output, LD is also provided, via the pin Cext. Cext is the logical "NAND" of PD_$\overline{U}$ and PD_$\overline{D}$ waveforms, which is driven through a series 2 kΩ resistor. Connecting Cext to an external shunt capacitor provides low pass filtering of this signal. Cext also drives the input of an internal inverting comparator with an open drain output. Thus LD is an "AND" function of PD_$\overline{U}$ and PD_$\overline{D}$.

Figure 11. Typical Phase Noise

A typical phase noise plot is shown below. "Trace 1" is the smoothed average, and "Trace 2" is the raw data.

Test Conditions: MASH-1-1 mode. F_{OUT} = 1.9204 GHz, $f_{COMPARISON}$ = 20 MHz, V_{DD} = 3.3 V, Temp = 25 °C, Loop Bandwidth = 50 kHz.

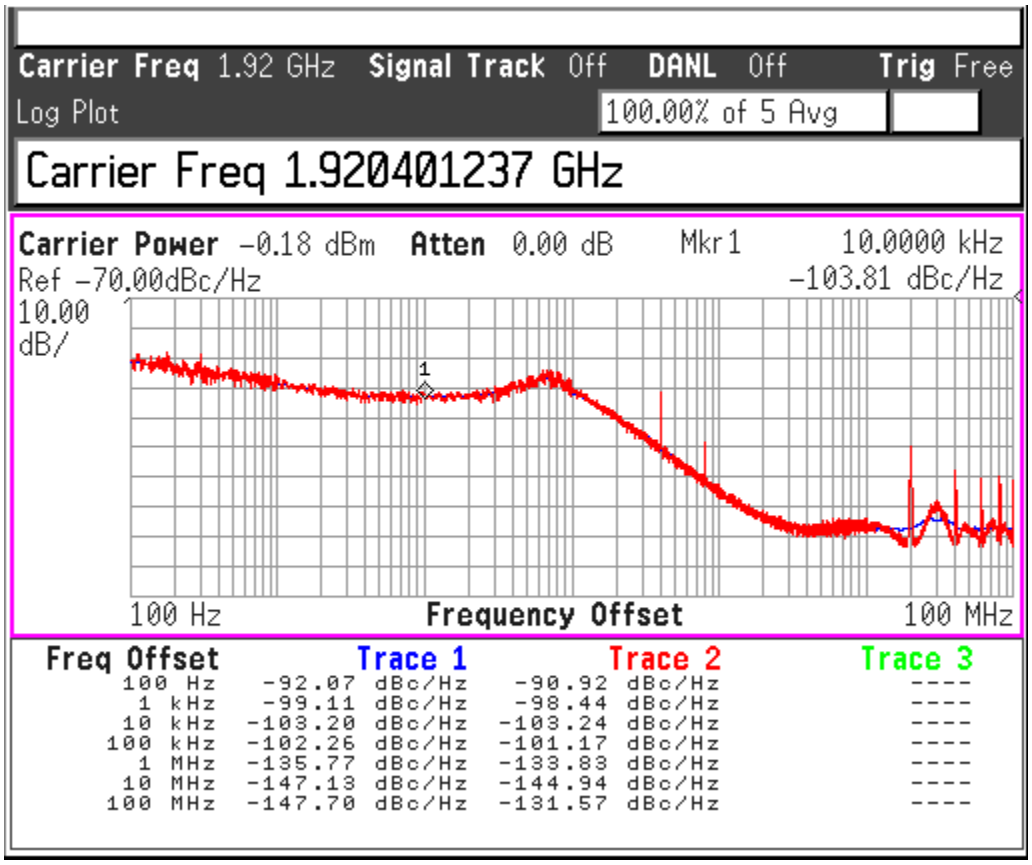


Figure 12. Package Drawing

Package dimensions: 68-lead CQFJ

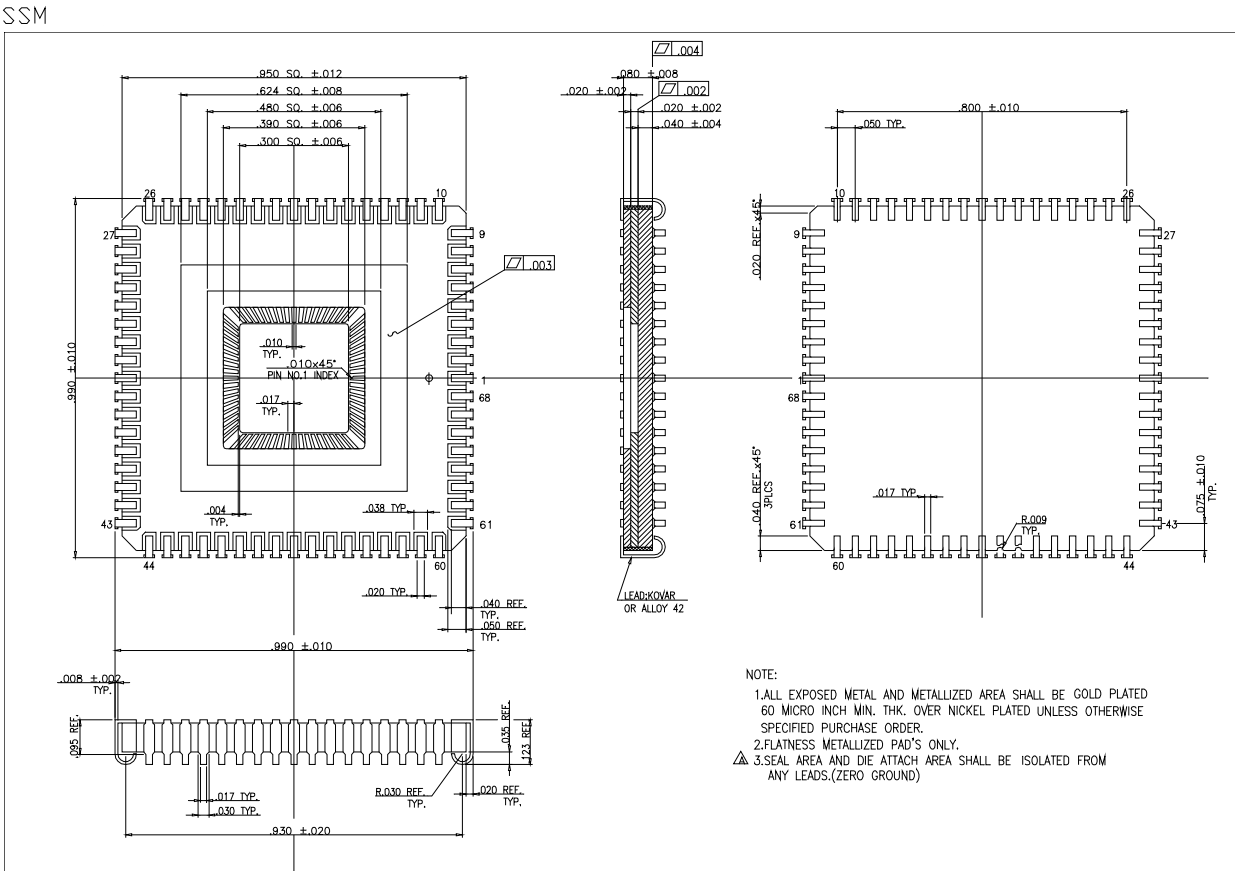


Table 11. Ordering Information

Order Code	Part Marking	Description	Packaging	Shipping Method
97632-01	PE97632 ES	Engineering Samples	68-lead CQFJ	Tray
97632-11	PE97632	Flight Units	68-lead CQFJ	Tray
97632-99	FA97632	Die	Waffle Pack	100 units / waffle pack
97632-00	PE97632 EK	Evaluation Kit		1/Box

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