AN2523
Application note

Migrating from STR91xF to STR91xFA

Introduction

STR9 microcontrollers have two major salestype groups, as follows:

- The initial group consist of devices STR91xFxxxxx, for example STR912FW44X6, with silicon revisions B, and D. Revision D is in production. Detailed technical information for these devices may be found in the STR91xF datasheet, STR91xF reference manual, and STR91xF errata documents.
- The second group consists of devices STR91xFAxxxxx, for example STR912FAW44X6, with revisions E and G. Revision G is in production. Detailed technical information for these devices may be found in the STR91xFA datasheet and STR91xFA reference manual documents.

This document describes at the system level the feature enhancements and silicon fixes incorporated in the new STR91xFA devices, compared to the original STR91xF devices.

It also describes what are the impacts when the STR91xF is replaced with the STR91xFA in your design.

The changes in the STR91xFA can be grouped into two categories:

- changes that are needed to fix the functional issues in the STR91xF
- changes that are feature enhancements to the STR91xF

The enhancements are new features and will have no impact in your existing STR91xF design. You have the option to add these new features to your design or not using it at all. The functional or silicon fixes in the STR91xFA are targeted at solving the problems that are documented in the STR91xF Errata Sheet. If you have implemented software workaround on some of the issues, the workarounds will work fine with the STR91xFA and no software change is required. Below is a summary of the changes, followed by detail descriptions.

Contents

1 Summary of pin functional changes and new pins

The STR91xFA pin assignments are exactly the same as the STR91xF. Two of the pins, JRTCK and P4.7, have additional functions to support the external ADC trigger input and RTC clock calibration. No action is needed if you do not plan to use the new features.

The STR91xFA has a new 144 ball BGA package. The additional pins allow the STR91xFA to expand the EMI function and add new bus control signals to support the PSRAM interface. Unless you use the new EMI pins in the BGA package, there is no need to change your PCB board layout.

Table 1. Changes in Pin Function

Item	Peripheral	Pin Name	Pin assignment	Functional Change
1	RTC	JRTCK	80 pin LQFP -61 128 pin LQFP-97 BGA-B11	JRTCK pin can be configured as RTC calibration clock output. The output clock frequency has been changed from 4.096 kHz in STR91xF to 32.768KHz in STR91xFA
2	ADC	P4.7	80 pin LQFP -77 128 pin LQFP-124 BGA-D5	P4.7 is the ADC Channel 7 input. In STR91xFA, the pin can also be configured as the External Trigger input for ADC conversion.
3	EMI Bus	EMI_LBn	BGA-G4	Lower Byte Select signal in 16-bit EMI bus mode. New signal, STR91xFA BGA package only.
		EMI_UBn	BGA-H1	Upper Byte Select signal in 16-bit EMI bus mode New signal, STR91xFA BGA package only
		EMI_WEn	BGA-A12	Write Enable signal in 16-bit EMI bus mode New signal, STR91xFA BGA package only.
		EMI_BCLK	BGA-M8	EMI bus clock signal New signal, STR91xFA BGA package only.
		EMI_WAITn	BGA-K8	WAIT input signal in 16-bit EMI burst mode New signal, STR91xFA BGA package only
		EMI_BAAn	BGA-H8	Burst Address Advance signal in 16-bit EMI burst mode New signal, STR91xFA BGA package only

2 Register bit definition changes

A few of the STR91xF control register bits have been become "don't care" bits as their function are hardwired in the STR91xFA. You can keep the "don't care" configuration bits in your code, they no longer has any impact on the device operation.

Many of the reserved bits in the EMI_BCRx register and the SCU_GPIOEMI register have been activated to support the PSRAM (synchronous) mode of the enhanced EMI bus. If you have kept these bits in the default reset value, there will be no impact when you switch to the STR91xFA devices.

Table 2. Register Bit Changes

Item	Peripheral/ Function	STR91xF	STR91xFA
1	FMI Bus Control/PFQ configuration	FMI_CR Register bit 0 - configure PFQ_FIFO size 0: PFQ FIFO size is 4 words 1: PFQ FIFO size is 8 words reset to 0	FMI_CR Register bit 0 - configurePFQ_FIFO size The bit becomes "don't care" in STR91xFA, the FIFO size defaults to 8 words and cannot be changed.
2	System Controller/PLL Configuration	SCU_PLLCONF Register: P, N and M reset values are: P = 0, N = 18h M = 19h (P, N, M configure the PLL clock frequency to 48 MHz)	SCU_PLLCONF Register: P, N and M reset values are: P = 03h,N = C0h M = 19h (The new P, N, M values generate the most stable 48 MHz PLL clock frequency)
3	Watch Dog Timer	SCU_PCGR1 Register bit 12 - 0: Clock to the Watchdog Block is stopped (default) 1: Clock to the Watchdog Block is running	SCU_PCGR1 Register bit 12 - This bit becomes "don't care". The system clock to the Watchdog Block is always running. (Note: this is not the Watch Dog timer clock)
		SCU_PRR1 Register bit 12 - 0: The Watchdog Block is held in reset (default) 1: The Watchdog Block is not held in reset	SCU_PRR1 Register bit 12 - This bit becomes "don't care". The Watchdog Block can not be held in reset.

Table 2. Register Bit Changes

Item	Peripheral/ Function	STR91xF	STR91xFA
4	EMI Bus	EMI_BCRx Registers: EMI Burst mode is not supported.	Add PSRAM (burst) mode new control bits in the Bus Control registers: Bit 0 - BLE: Byte Lane Enable Bit 8 - BPM: Burst and Page Mode Read Selection Bit 9 - SyncReadDev : Synchronous read access device Bit 11:10 - BRLEN[1:0]: Burst Read Transfer Length Bit 16 - BMWrite : Burst mode write: Bit 17 - SyncWriteDev: Synchronous write access device. Bit 19:18 - BWLen : Burst write transfer length
		SCU_GPIOEMI	Bit 1 - Enable EMI_BCLK clock pin (BGA package) Bit 2 - Enable EMI signals: WE/UB/LB configuration (BGA package)

3 New registers

Three key functional blocks, ADC, Motor Control and EMI bus in the STR91xF have been modified to provide additional features. The new registers, listed in the *Table 3* below, are added to control the new functions. Please refer to the STR91xFA Reference Manual (UM0388) for the detailed register definition. The default value of these registers in the STR91xFA will have no impact in your existing design.

Table 3. New Registers

Item	Peripheral	Register Name	Register Address offset	Functional Description
1	ADC	ADC_DDR	38h	ADC DMA Data Register - stores converted data of the selected channel for DMA transfer.
		ADC_CR2	3Ch	ADC Control Register 2 - this is the 2nd control register in the ADC that supports conversion trigger from pin, timer and PWM.
2	Motor Control	MC_ECR	48h	Enhanced Control Register - supports the new IMC features, including: Double Update mode, 16 bit PWM counter, 10 bit Dead Time counter, ADC trigger and output polarity.
		MC_LOK	4Ch	Lock Register - some of the IMC control bits can be "locked" from being inadvertently modified.
3	EMI Bus	EMI_BRDCRx	1Ch - FCh	Burst Read Wait Delay Register - define wait state in a read burst cycle (BGA package)
		EMI_CCR	204h	Clock Control Register - Enable the BCLK clock and clock frequency divide ratio.

3.1 Product ID and Silicon Revision Indicator

STR91xF and STR91xFA devices contain 32 One-Time-Programmable (OTP) bytes. Two of these bytes contain product identification and a silicon revision indicator. Firmware may read these bytes to become aware of the silicon revision on which it is operating, and optionally act on this information. For example, you may want to create a single firmware application that can operate on either the STR91xF or the STR91xFA, taking advantage of the new features of STR91xFA if applicable. See the "One Time Programmable Memory" section of the STR91xFA datasheet for the values of these dedicated OTP bytes for all the silicon revisions.

4 List of functional changes and silicon fixes

The STR91xF has some minor functional problems that are fixed in the STR91xFA. The following is a list of the fixes; the details are described in *Section 6 on page 10*.

1. I2C bus error conditions
2. PLL default value
3. RTC calibration clock output changed from 4.096 KHz to 32.768 kHz
4. Idle Mode Dependence on RTC
5. Exit from Sleep and Idle mode
6. Clock Switching Problem/PLL configuration
7. UART FIFO overflow flag
8. LVD and VDD fall time requirement
9. LVD logic may hold reset active inappropriately
10. Watchdog disable control logic
11. Motor Control output polarity

5 List of enhancements

The following is a list of the enhancements on the four STR9 functional blocks: PFQ/BC, ADC, Motor Control and EMI bus. The Prefetch Queue / Branch Cache performance have been improved by increasing the PFQ/Cache size to reduce the time on non-sequential instruction fetch. The ADC, Motor Control and EMI bus all have added new features and options that will extend the peripherals' capability. The details of the enhancements are described in *Section 7 on page 15*.

1. Prefetch Queue / Branch Cache Enhancement
   - 16 Cache entries
   - 8 words deep per entry
2. ADC enhancement
   - Add ADC conversion trigger input:
     External pin input trigger
     Timer Trigger
     PWM Trigger
   - DMA support
3. Motor Control Enhancement
   - Double Update Mode
   - Lock Bits
   - Trigger ADC conversion with PWM
   - 16-bit PWM Counter and Compare Registers
   - 10-bit Dead Time Counter
   - Output values in ES and debug modes
   - Hardware reset of ESC Register
4. EMI Bus Enhancement (BGA package only)
   - Add new signals EMI_BCLK, EMI_BAA, EMI_WE, EMI_WAIT
   - Support EMI PSRAM (burst) mode
   - Add WE, UB/LB byte selection signal for 16 bit write configuration

6 Functional changes and silicon fixes in STR91xFA

6.1 I2C bus

Functional Fix: I2C bus error conditions

Description: Certain bus error conditions were not always reported correctly in the status registers of the I2C controller. The specific conditions were: (1) failure to set the ARLO bit when bus contention is detected in the acknowledge pulse in reception mode; (2) failure to set the BERR bit if a misplaced START or STOP condition occurs on the first data pulse of a master transmission; and (3) the BUSY bit does not correctly report bus activity if the I2C controller is not enabled. These bugs have been fixed on STR91xFA.

Impact: Probably none. Since no software workarounds were identified or recommended for the bugs that were fixed, no changes should be needed in response to the fixes. However, error recovery software designed according to the I2C protocol specification will now see correct settings for the ARLO, BERR, and BUSY bits in rare cases where they would previously have been incorrect.

6.2 PLL

Functional Fix: Configuration Register default value

Description: Default values in the SCU_PLL configuration register after reset were incorrect for the intended behavior in STR91xF. Defaults have been changed to P=3, N = 0xC0, M = 0x19 (PLL Clock = 48 MHz, assuming 25 MHz main crystal) in STR91xFA.

Impact: Software workaround to set the correct value at startup is no longer required, but harmless if present.

6.3 RTC

Functional Change: RTC Calibration Frequency

Description: In STR91xF devices, the RTC calibration clock on pin JRTCK was a nominal 4.096 kHz signal, obtained by dividing the 32.768 KHz RTC by eight. In STR91xFA, the divide by eight is bypassed, and JRTCK is driven 1:1 by the RTC input.

Impact: Speeds up the calibration procedure and provides a digital copy of the RTC for use by other chips.

6.4 Low power modes

Functional Fix: Idle Mode Dependence on RTC

Description: When entering Idle Mode in STR91xF, the RTC clock must be present for the internal state machine to switch to low power mode. In the STR91xFA, the RTC clock is no longer needed. (Note: RTC clock is needed to enter the Sleep mode in both the STR91xF and STR91xFA device)

Impact: RTC crystal is not required for Idle mode and can be removed if all other RTC related functionality is not needed.

Functional Fix: Exit from Sleep and Idle Mode

Description: The STR91xF may fetch incorrect instruction from the Flash memory after a wake up interrupt from low power mode. The work around is to execute the power mode switching routine in the SRAM instead of the Flash memory. This problem is fixed in STR91xFA and the CPU can fetch the correct instruction from Flash memory.

Impact: The workaround solution for the STR91xF is still good. Option: the power mode switching routine can be moved back to the Flash memory in the STR91xFA.

Functional Fix: Entering Idle and Sleep Mode

Description: After the Sleep mode or Idle mode bit is set in the SCU_PWRMNG register, the Power Management Unit requires a period of time to switch off all the CPU and peripheral clocks safely before entering low power mode. Any wake up event occurring within this period of time is ignored. In STR91xFA device, this problem is fixed in Idle mode.

The Sleep mode will still require a period of time to enter the mode. This time period is depending on the frequency of the CPU clock and the slowest Peripheral clock. Please refer to the reference manual for the Sleep Mode timing calculation.

Impact: A wake up event that is activated during the Sleep Mode entry time will be ignored by the CPU.

6.5 Clock control

Functional Fix: Clock Switching Problem/PLL configuration

Description: Disabling the PLL when it was driving the CPU clock or doing so too soon after switching clock sources could cause the CPU to enter a hung state. Recovery was not possible with a system reset; a full power down and restart was needed. This problem has been fixed in STR91xFA. The state machine controlling system clock generation now guarantees smooth clock switching. It disallows disabling of the PLL or updating the SCU_PLLCONF register while the PLL is driving the system clock. The PLL is updated only after the CPU clock is switched over to the OSC.

Impact: If software workarounds (as stated in the STR91xF Errata Sheet, section 1.14) to avoid clock switching problems are already implemented in your software, no change is needed for STR91xFA. Otherwise, follow the steps below to change PLL clock configuration while the CPU is running on the PLL clock:

1. Switch the CPU Master clock source to the OSC by setting bits [1:0] in the SCU_CLKCNTR register to "10".
2. Write the new configuration to the SCU_PLLCONF register (write the new P, N and M values with the PLL_EN enable bit set to "0").
3. The SCU_PLLCONF register will be updated after the clock has been switched to the OSC.
4. If you need the CPU to run at the new PLL clock frequency, write to the SCU_PLLCONF register again with the new P, N and M values AND the PLL_EN bit set to "1".
5. Switch the CPU clock source back to the PLL clock by setting bit[1:0] in the SCU_CLKCNTR register to "00".
6. The CPU Master clock will switch automatically from the OSC to the PLL once the LOCK bit is set. Do not initiate another SCU_PLLCONF register change before the LOCK bit is set.

6.6 UART

Functional Fix: UART FIFO Overflow Flag

Description: In STR91xF devices, there was a condition in which received data could be lost due to FIFO overflow, but no indication of the FIFO having overflowed was given. The condition arose when the FIFO was full, and there was a simultaneous read from the data register and arrival of new data. In that case the arriving data was not stored, but neither was an overflow signaled. This has been fixed in STR91xFA.

Impact: Overflow is now properly signaled in all cases where data is lost.

6.7 LVD (Low Voltage Detector)

Functional Fix: LVD and VDD fall time requirement

Description: The STR91xF generates an internal reset signal when the VDD power supply drops below the LVD (Low Voltage Detect) threshold level. If the rate of fall of VDD voltage is less than 100 µs as VDD drops from 1.8 V through the 1.4 V threshold, the Low Voltage Detector logic will not generate the internal reset signal. A workaround solution is to use an external reset supervisor device to drive the RESET_INn input pin. This problem is fixed in STR91xFA devices

Impact: If an external reset supervisor device is used as a workaround solution, there is no need to make any changes and no impact on the STR91xFA.

Functional Fix: LVD logic may hold reset active inappropriately

Description: The LVD logic in STR91xF is able to detect the first occurrence of a VDD or VDDQ voltage drop that goes below the threshold voltage and it correctly generates an internal reset signal to the CPU and system. However, for subsequent drops of VDD or VDDQ voltage below threshold, the LVD logic generates an active internal reset signal, but the signal remains active (is stuck) even after VDD or VDDQ rises above the threshold again.

The CPU is hung in a state of reset. A power cycle is needed on VDD to clear the stuck reset and release the CPU. The problem is fixed in STR91xFA.

Impact: The workaround solution for STR91xF is to use an external reset supervisor device. The STR91xFA will work fine if an external supervisor device is used, it will also work fine if the device is removed.

6.8 Watchdog

Functional Fix: SCU Control Register control bits will not disable the Watchdog

Description: Watchdog Mode is enabled by setting the WE bit in the WDG_CR register. Once enabled the Watchdog cannot be disabled by software by clearing the WE bit. In the System Control Unit, the SCU_PCGR1 and SCU_PRR1 registers also control the clocking and reset operation of the peripherals, including the Watchdog.

By setting bit 12 of either of the two registers in STR91xF, the Watchdog will lose its clock or go into reset state and become disabled. This is in contradiction to the Watchdog specification that once it is enabled, it cannot be disabled by software.

Impact: This problem is fixed on the STR91xFA. There is no need to modify your software as bit 12 of the two registers become "don't care" bit. Once the Watchdog timer is enabled, cannot be disabled in the STR91xFA through software control.

If for any reason there is a need to temporarily prevent the watchdog from timing out (example: EEPROM emulation Flash bank erase), you can change the watchdog configuration in the STR91xFA to provide a period of time of no watchdog activity. This can be achieved by switching from the fast 48 MHz PCLK to the slow 32 kHz RTC clock as the watchdog counter clock source. With the RTC clock, the CPU only needs to update the watchdog once every ten seconds. Please note once the RTC clock is selected as the Watchdog counter clock, you cannot switch the clock source to the PCLK as long as the Watchdog is enabled.

6.9 Motor Control

Functional Fix: PWM Output Polarity

Description: The Motor Control (MC) drives 3-Phase PWM signals and complementary signals (UH, UL, VH, VL, WH, WL). There are two situations where the MC outputs remain a constant:

1. When the Compare register (MC_CMPx) value is greater than the Compare 0 Register (MC_CMP0), the corresponding PWM output signal is held at '1'.
2. When the Compare register (MC_CMPx) value is 0, the corresponding PWM output signal is held at '0'.

The output is a constant at "1" and "0" for the above two configurations when the polarity bits in the MC_PSR register are set to "0".

The MC outputs (UH and UL, for example) are complementary to each other. But for the above two configurations in STR91xF the outputs are not complementary and both signals stay at the same level. This problem is fixed in STR91xFA.

Impact: This problem is fixed in STR91xFA.

6.10 Flash memory

Functional Fix: Flash erase and programming

Description: The Dual Bank Flash architecture in the STR91x supports the modification (erase or programming) of one Flash bank while the CPU is fetching codes from the other bank (RWW - read while write operation). This feature in the STR91x is functional only when the Flash bus clock (FMI Clock) frequency is 25 MHz or lower. At higher clock frequency, the CPU may read incorrect code or status from the Flash banks. The Flash modification problem affects both the dual banks and the OTP sector.

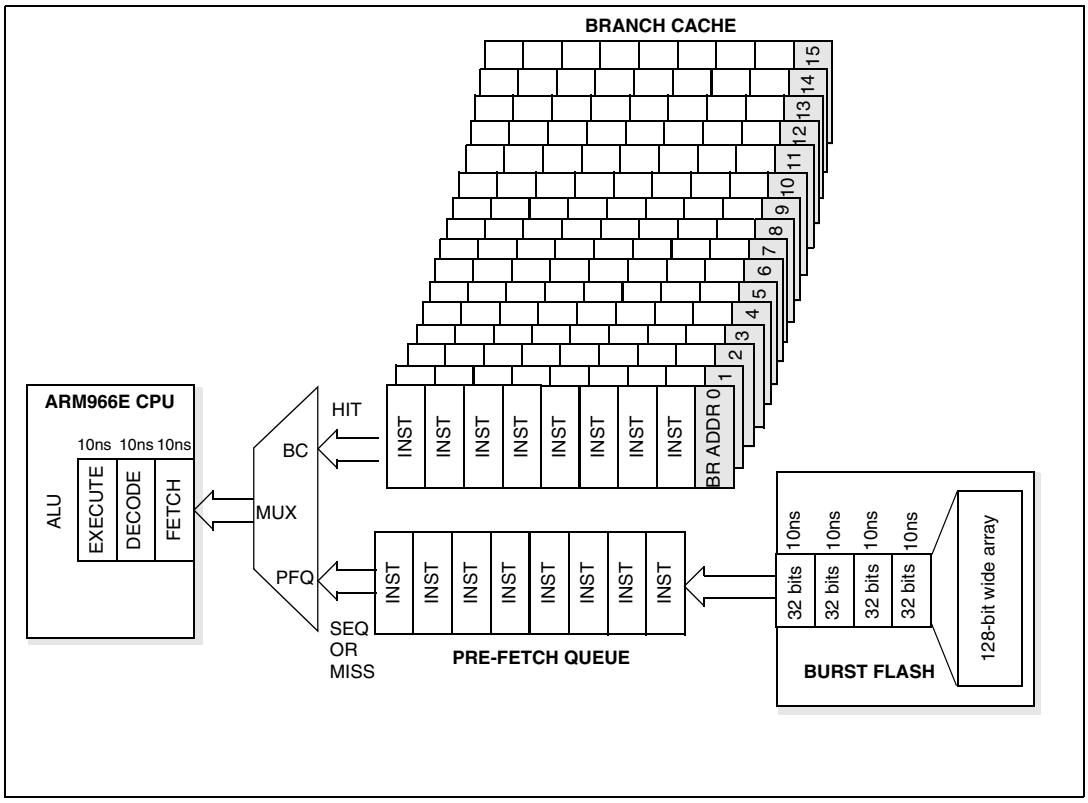
Impact: This problem is fixed in STR91xFA and the Flash memory can be erased or programmed at 96 MHz. The workaround solution for STR91xF remains good in the STR91xFA.

7 Enhancements in the STR91xFA devices

7.1 Prefetch Queue / Branch Cache

Description: The STR91xFA has a custom Memory Accelerator (Pre-fetch Unit and Branch Cache) coupled with the I-TCM to accelerate the performance of the Flash memory system and lower Interrupt Latency. Its general structure is illustrated in *Figure 1* below. A full description may be found in the STR91XFA Reference Manual.

Figure 1. Memory accelerator



In STR91xFA, the number and size of branch cache entries was increased from five entries with four words each to 16 entries with 8 words each. The 16 entries are partitioned into 15 general purpose entries plus one entry dedicated to the VIC. The branch cache serves to accelerate instruction fetching from the burst-mode flash memory in looping code.

Impact: Performance enhancement. Fewer wait states will be incurred in response to program branches taken repeatedly. Aside from the performance improvement, the change is completely transparent to both systems and application software.

In STR91xF, the FMI_CR register bit 0 is used to define the PFQ FIFO size (4 or 8 words). In STR91xFA this bit becomes a "don't' care" bit. The PFQ FIFO size is always powered up as 8 words. The change in FIFO word size will have no impact on your system operation.

7.2 ADC

Description: For STR91xFA, several significant enhancements were implemented in the ADC controller. They include:

1. External Pin Trigger: the ability to initiate a conversion in response to an edge event on an external I/O pin
2. Timer Connection: the ability to initiate a conversion in response to a timer expiration
3. PWM Connection: the ability to initiate a conversion in response to cycling of the PWM counter in the induction motor controller. (See *Section 6.9: Motor Control on page 13*.)
4. DMA: the ability to issue a DMA request to store conversion results in memory

Two new registers have been added to the ADC controller to support the above new capabilities. They are ADC_DDR and ADC_CR2. ADC_DDR is the DMA data register, while ACD_CR2 is a second control register.

The DMA data register buffers a completed 10-bit conversion result pending its storage in memory. It also contains the ADC channel number, an overflow indicator bit (OV), and an overrun indicator bit (OR), as shown below. The second control register holds control bits associated with the conversion triggering mode.

Table 4. ADC registers

Name	Address Offset	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADC_DDR	38h	OV		OR	Channel			Channel's converted data									
ADC_CR2	3Ch												Trigger selection mode and enable bits				

Trigger selection mode and enable bits:

[1,0] trigger select - selects the source of trigger (PWM, TIMER or EXTERNAL)

01: PWM trigger

10: Timer trigger

11: External pin trigger

00: No trigger (default)

[2] EXTRG- enable external trigger (when '1')

[3] DMAEN- DMA enable

[4] MOR - mask over-run interrupt

Impact: The new capabilities are extensions only; the ADC unit for STR91xFA remains upward compatible with that of STR91xF. There is no impact for any applications developed for STR91xF. However, any new applications which take advantage of the extended capabilities will require software modification.

Note: The new ADC DMA request to the DMA Controller shares the same input (input #9) with the External DMA Request1. If External DMA Request1 is used in your current design, you may not be able to use the ADC DMA feature.

7.3 Motor control enhancement

Like the ADC controller, the Induction Motor Controller was substantially enhanced for STR91xFA. Also as with the ADC enhancements, the IMC enhancements were designed for upward compatibility. There should be no software impact for applications developed for STR91xF which do not specifically enable the enhancements. The only impacts are for new applications that choose to make use of the enhancements.

The paragraphs below summarize the new features, and what they enable. The features are controlled by two new control registers: an Enhance Control Register (MC_ECR) at offset 0x48, and a Lock Register (MC_LOK) at 0x4C.

7.3.1 Double update mode

Description: A Double Update Mode (DUM) is implemented, whereby the three phase compare registers CMU, CMV, and CMW, along with the PWM clock compare register CM0, can be updated from their respective preload registers when the PWM counter register hits its maximum value as well as its minimum value (i.e., zero). The maximum value for the PWM counter is the value set in the CM0 register. When the PWM counter increments up to this value, it resets to zero (in classical mode) or reverses direction and begins counting down to zero (in zero-centered mode).

DUM is only applicable in zero-centered mode, because in classical mode, the maximum value for the PWM counter register is followed immediately by a clear to zero. The zero value triggers a normal update cycle, which would make the DUM update on the maximum counter value redundant.

Impact: When enabled through settings in register MC_ECR, the DUM doubles the frequency of control value updates to the PWM counter compare registers. This provides a finer granularity of PWM control. Since the reset values in MC_ECR disable DUM by default, there is no impact to older software.

7.3.2 Lock bits

Description: A lock register, MC_LOK, has been added to prevent certain control register bits from being inadvertently modified. A lock bit, once set, prevents its associated control register bit or bits from being modified. The lock bits are "write once" bits; once a specific lock bit is set, it cannot be cleared except through a system reset. Its format and a list of associated control bits are shown below.

Table 5. Lock register

Name	Address Offset	15	14	13	12	11	10	9	8	7	6	5	lock bits LOKx				
MC_LOK	4Ch	Reserved: all bits '0'											4	3	2	1	0

LOK0 - Locks PCR0(7,0), DTE and ODTS bits

LOK1 - Locks PCR1(6), EST_EN

LOK2 - Locks PSR(5:0), phase polarity bits PUH, PUL, PVH, PVL, PWH, PWL

LOK3 - Locks OPR(5:0), Output Peripheral Register bits

LOK4 - Locks DTG(5:0), Dead Time Generation Register

Impact: Lock bits can be used to simplify software development and add robustness. By locking critical control register bits, the hardware can be protected from malfunctioning software. In addition, locks on selected bits enable software to update other bits in the same control registers without concern for changing the values of the locked bits.

7.3.3 Trigger ADC with PWM

Description: A capability was added to trigger an ADC conversion synchronized with the PWM counter cycle. Four options are supported:

- Don't generate an ADC trigger event (default)
- Generate an ADC trigger when the PWM counter goes to zero ('ZPC')
- Generate an ADC trigger when the PWM counter reaches its maximum ('CM0')
- Generate an ADC trigger when the PWM counter goes to zero AND the pulse repetition down counter is at zero (RDC = 0)

The choice among the above four options is made through the 2-bit ATS field (ADC Trigger Selection) in the Enhance Control Register MC_ECR.

Impact: The ADC trigger capability enables control of "sensorless" PM or SR motors, in which rotor position is inferred by tracking the back EMF or the inductance in one or more stator coils after a drive pulse. It has no impact on software developed for earlier silicon revisions.

7.3.4 16-bit PWM counter and compare registers

Description: The compare registers CP0, CPU, CPV, and CPW, as well as the PWM counter itself, have been widened to 16 bits. Bit 5 of the Enhanced Control Register MC_ECR (the 'EPWM' bit) controls whether or not the additional high order bits are used. In normal mode, when EPWM = 0 (the default), the additional bits are masked to zero, and operation of the PWM unit is identical to what it was in STR91xF. When EPWM is set to '1', the additional high order bits are used. All compares between the PWM counter and the four compare registers are then full 16-bit compares.

Impact: The wider compare registers enable finer granularity of PWM control, if needed. They permit a larger step count for one PWM cycle, when the enhanced mode is selected. For a given PWM cycle frequency, the PCM counter can be clocked at a higher frequency, by using a smaller value in the PWM clock prescaler register, MC_CPRS. There is no impact to older software when the default mode (normal) is used.

7.3.5 10-bit dead time counter

Description: The Dead Time Generator register, MC_DTG, has been widened from 6 bits for the delay count to 10 bits. Whether the old 6-bit width or the new 10-bit width is used is controlled by bit 4 of MC_ECR, the EDTC bit. When EDTC = 0 (default), the 6-bit width is used. MC_DTG bits (9:6) are masked to zeros. When EDTC = 1 (enhance mode), all 10 MC_DTG bits are used to count delays.

Impact: Enables larger delay counts to be specified when a faster PWM counter clock is used. No impact on previously developed software when default mode is used.

7.3.6 Output values in Emergency Stop and Debug mode

Description: Two control bits, EMS and ESP, are present in the MC_ECR register which, under particular circumstances, modify the logic values that are output on the six PWM output pins MC_UH, MC_UL, MC_VH, MC_VL, MC_WH, and MC_WL.

Bit MC_ECR[6] is designated as the Enhanced Motor Stop or EMS control bit. Writing a '1' to that bit enables an enhanced stop feature that is described below. Bit MC_ECR[1] is the Enhanced Stop Polarity or ESP bit. The ESP bit selects between normal and inverted output values under applicable conditions.

The conditions under which these bits affect the PWM output values are complex. However, they can be summarized as any condition under which normal PWM cycling is halted, or needs to be halted. The intent is to place all motor drive switches in the OFF state, allowing the motor to freewheel. The purpose is to protect the motor drive circuits from burnout, not to apply active braking to stop the motor.

There are three situations in which normal PWM cycling is halted. One is in response to an active signal on the motor controller's Emergency Stop pin, ESTOP. This signal, mapped through one of the GPIO interrupt request pins, normally originates with thermal protection circuitry in the motor drive power electronics. It should not be confused with the signal from a motor equipment operator's emergency OFF button. The latter calls for active braking of the motor, which requires continued PWM cycling.

In normal operation, the automatic response to the ESTOP signal is to force the PWM outputs to zeroes. Zero is assumed to be the value corresponding to the OFF state for the drive switches. In Enhanced Stop configuration, the value forced to the PWM outputs is determined by the ESP bit. This allows for the possibility of that a PWM output of '1' corresponds to the OFF state of a drive switch.

The second situation in which PWM cycling is halted is when software has explicitly stopped it, by clearing the PWM Counter Enable bit (PCE, bit 5) in register MC_PCR0. In normal operation, it is essential for the controller software to "safe" the PWM outputs before disabling the PWM counter. This is done by setting bit 6, the Output Data Selection bit (ODS) in the Output Peripheral Register MC_OPR. Setting the ODS bit in MC_OPR forces the six PWM outputs to the XOR of MC_OPR bits [5:0] and MC_PSR bits [5:0]. Failure to set the ODS bit before disabling the PWM counter could result in burnout of one or more power switches in the motor drive. As a protection measure, the Enhanced Motor Stop (EMS) feature has been implemented. If the PWM counter is disabled by software while EMS bit is enabled, control logic will check the ODS bit. If it is not set, then the PWM outputs are forced to a safe state in the same manner they would be in response to the ESTOP signal, where the PWM output values are the XOR of ESP bit and MC_PSR bits[5:0]

The third situation in which PWM cycling is halted is in debug mode, when a hardware break condition effectively halts the master clock. When EMS bit is set, the Debug Output Protection bit (DOP) in register MC_ECR enables the PWM outputs to be determined by the ESP bit.

Impact: Default settings for control registers insure no impact to software developed for older revisions. Use of the new stop mode features will facilitate software development and testing for new projects, and result in more robust production code.

7.3.7 Hardware reset of ESC register

In STR91xF devices, after an emergency stop, the firmware writes "4321h" to the MC_ESC register to restart the PWM and then writes "0000" to clear and re-arm the ESTOP. In

STR91xFA devices, the clearing of the MC_ESC register is performed by hardware automatically right after the "4321h" write cycle. This feature is enabled by bit 8 (HRE) in the new MC_ECR register.

7.4 EMI bus enhancement (BGA 144 package only)

In addition to the LQFP80 and LQFG128 packages available in the STR91xF device family, STR91xFA devices are offered in a new BGA144 package. Some of the additional I/O pins available in the BGA package have been used to provide an enhanced External Memory Interface (EMI). The enhanced interface supports PSRAM type burst mode memories.

7.4.1 Option to configure the new EMI_BCLK signal

Description: A bit was added in the GPIO external memory interface register (SCU_EMI) to enable/disable the new external EMI_BCLK clock.

Bit 1 was added to the SCU_EMI register, defined as follows:

- Bit 1 = 0: EMI_BCLK clock out is ENABLED (default)
- Bit1 = 1: EMI_BCLK clock out is DISABLED

Impact: No impact for STR91xF users.

7.4.2 Option to configure the EMI_WRLn and EMI_WRHn pins

Description: A bit was added in the GPIO external memory interface register (SCU_EMI) to configure the EMI_WRLn and WMI_WRHn pins.

Bit 2 was added to the SCU_EMI register, defined as follows:

- Bit 2 = 0: The EMI pins function as EMI_WRLn and EMI_WRHn signals as in STR91xF devices (default)
- Bit 2 = 1: The EMI pins function as byte select signals (EMI_LBn and EMI_UBn)

Impact: No impact for STR91xF users.

7.4.3 Interface to PSRAM (burst mode)

Description: The BGA package brings out four new bus signals: EMI_BCLK, EMI_BAA, EMI_WE and EMI_WAIT. It also provides options to program the EMI_WRLn and EMI_WRHn signals as EMI_LBn (low byte select) and EMI_UBn (upper byte select). With the additional bus control signals, the EMI is able to interface directly to a PSRAM.

In PSRAM mode, the EMI bus is configured as a 16-bit, multiplexed bus. The EMI_ALEn signal is programmed with negative polarity and a 2-clock-wide pulse width to meet the PSRAM's ADV# (address valid) timing requirement. The EMI address is latched by the PSRAM at the rising edge of the BCLK while the EMI_ALEn is low. In a read bus cycle, the EMI bus is tri-stated half a clock after the trailing edge of the EMI_ALE signal. The PSRAM can then drive the bus when EMI_RDn becomes active.

The EMI bus can access the PSRAM memory array in asynchronous mode or in burst mode.

However, the EMI bus must be in asynchronous mode when writing to the PSRAM bus configuration register. The CRE signal, which is required to be high when writing to the

PSRAM configuration register, can be connected to any GPIO output pin and the signal logic level is controlled by the firmware.

Impact: There is no impact for STR91xF users. The new BGA package is needed to implement the new EMI signals

7.4.4 Asynchronous mode and PSRAM (Synchronous) mode timings

Description: The STR91xF supports asynchronous access only while the STR91xFA supports both asynchronous and synchronous modes. There are timing differences between the modes which are listed below:

1. ALE pulse width - In asynchronous mode, the ALE pulse width is either 1 or 2 BLCK clock periods in length. In synchronous mode, the ALE pulse width is truncated to half or one and half of BCLK.
2. In asynchronous mode, the control signals such as WRn, RDn, ALE are aligned to the rising edge of BCLK, while in synchronous mode the signals are aligned with the falling edge of BCLK.
3. The WR and RD pulse widths are different in the two modes.

Impact: There is no impact for STR91xF users. The new BGA package is needed to implement PSRAM mode.

8 Revision history

Table 6. Document revision history

Date	Revision	Changes
17-Apr-2007	1	Initial release
07-May-2007	2	Added *Section 3.1: Product ID and Silicon Revision Indicator on page 7*

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