

CLEAR LOGIC

# CL8636A

Laser-Configured ASIC Family

## Key Features

- ◆ Laser-Configured ASIC (LASIC<sup>®</sup>) technology offers the ultimate combination of performance, flexibility, and low cost
- ◆ Functionally, architecturally, and electrically compatible with industry-standard FLEX<sup>®</sup> 8000 series FPGAs
- ◆ High Density
  - 6,000 Usable gates
  - 636 Flip-flops
  - 136 Maximum user I/O pins
- ◆ Laser fuse technology provides very fast, dense interconnect routing
- ◆ Optional Instant-On configuration eliminates the need for an external configuration EPROM
- ◆ Fabricated using 0.5 micron CMOS process
- ◆ Very low current consumption (active and standby)
- ◆ Supports 3.3 volt or 5.0 volt I/O operation
- ◆ Alpha particle immune

## CL8000 Product Family Overview

Parameter	CL8282A	CL8452A	CL8636A	CL8820A	CL81188A
Available Gates	5,000	8,000	12,000	16,000	24,000
Useable Gates	2,500	4,000	6,000	8,000	12,000
Flip-flops	282	452	636	820	1,188
Logic Elements	208	336	504	672	1,008
Max user I/O pins	78	120	136	152	184
Packages	84 pin PLCC 100 pin TQFP	84 pin PLCC 100 pin TQFP 160 pin PQFP	84 pin PLCC 160 pin PQFP 208 pin PQFP	144 pin TQFP 160 pin PQFP 208 pin PQFP	208 pin PQFP 240 pin PQFP

8K tbl 01

**Description**

The Clear Logic CL8000 Laser-Configured ASIC (LASIC®) family offers the ultimate combination of performance, flexibility, and cost. This family is a system level second source to Altera FLEX® 8000 products. For designs not requiring in-system reprogrammability, design verification can be performed using the programmable Altera devices, and Clear Logic LASICs can be used for low cost, high volume production.

Clear Logic's innovative laser ASIC technology eliminates NRE costs, test vector development, ordering minimums and long lead times. No re-simulation or re-layout is required, as the device is engineered using a cell-based, PLD-like architecture. Clear Logic's TestCell technology ensures complete test coverage through the use of specialized testing modes which are transparent to the user.

The Clear Logic CL8000 Laser-Configured ASIC family is based upon a large array of logic elements. Each logic element contains a configurable look up table for combinatorial functions and a register for sequential operations. A group of eight logic elements forms a block. Laser-configured metal fuses implement logical functions and control signal routing

Laser configuration provides reduced cost and enhanced performance. These inherent performance benefits include extremely consistent propagation delays, reduced power consumption, and improved immunity to noise and upset events.

**Configuration**

Clear Logic's CL8000 LASIC® family is compatible with all six configuration modes defined for the FLEX® 8000 product family. These configuration modes include the following:

- ◆ Active Serial
- ◆ Active Parallel Up
- ◆ Active Parallel Down
- ◆ Passive Parallel Synchronous
- ◆ Passive Parallel Asynchronous
- ◆ Passive Serial

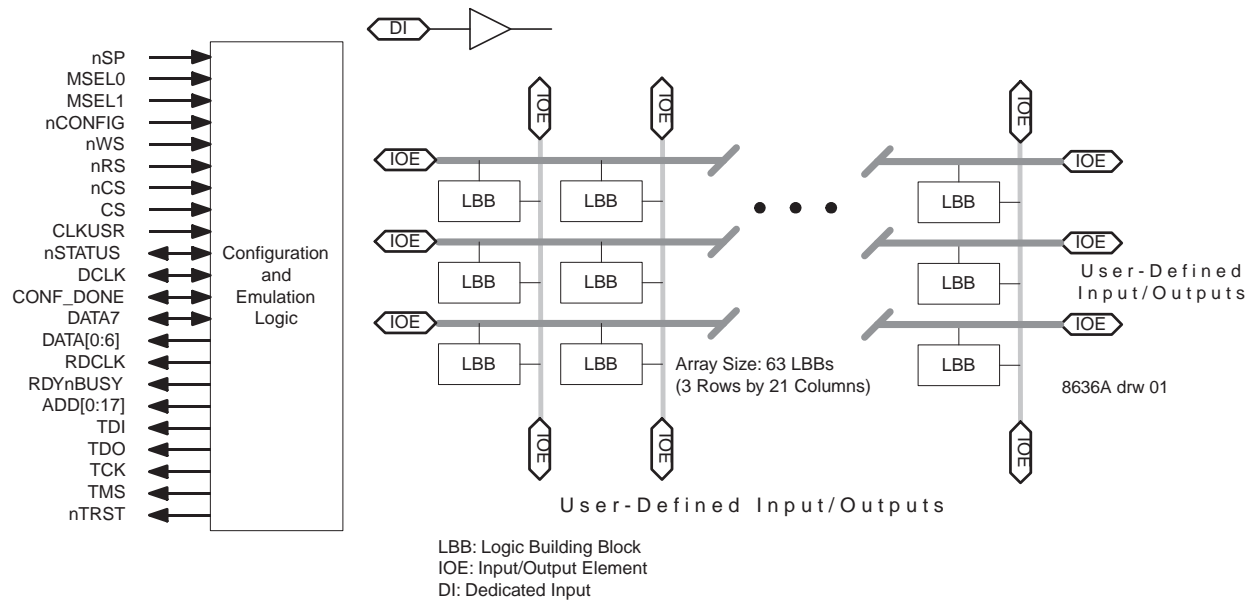
The CL8000 is already configured when it is shipped, and can be configured to bypass the FLEX<sup>®</sup> 8000 configuration modes. This “Instant-On” configuration mode eliminates the need for external EPROMs or microcode. In the Instant-On mode, the CL8000 device begins Initialization immediately upon a low-to-high transition on the nCONFIG pin.

## Additional Information

For further information on designing with the CL8000 LASIC family, please refer to the following documents:

- ◆ AN-01: Requesting a First Article. This document provides instructions on how to submit a bitstream file for generation of first articles.
- ◆ AN-02: Clear Logic Packaging Guide. This document provides specifications and drawings for packages used by the CL10K family and other Clear Logic devices.
- ◆ AN-03: CL8000 and System Configuration. This document contains a detailed discussion of all aspects of configuring CL8000-based systems.
- ◆ AN-04: CL8000 Technology White Paper. This document outlines the technologies employed by the CL8000 LASIC family.
- ◆ AN-05: Calculating CL8000 Power Consumption. This document provides guidelines for calculating power consumption based on CL8000 design characteristics.
- ◆ AN-06: Eliminating the Serial EPROM from FLEX 8000 Designs. This document outlines how additional savings can be achieved by removing the EPROM from the CL8000 LASIC family.
- ◆ AN-07: CL8000 Test Methodology. This document describes how Clear Logic provides 100% stuck-at fault coverage.
- ◆ AN-08: CL8000 LASIC Timing and Function Compatibility. This document shows how a seamless conversion from FPGA to ASIC can be achieved with no additional engineering can be achieved with Clear Logic.

**Block Diagram**



**Pin Configuration**

Pin Name	84 pin PLCC	160 pin PQFP	208 pin PQFP
nSP	75	1	207
MSEL0	74	3	4
MSEL1	53	38	49
nSTATUS	32	83	108
nCONFIG	33	81	103
DCLK	10	120	158
CONF_DONE	11	118	153
nWS	30	89	114
nRS	48	50	66
RDCLK	49	48	64
nCS	29	91	116
CS	28	93	118
RDYnBUSY	77	155	201
CLKUSR	50	44	59
ADD17	51	43	57
ADD16	55	33	43
ADD15	56	31	41
ADD14	57	29	39
ADD13	58	27	37
ADD12	60	24	31
ADD11	61	23	30
ADD10	62	22	29
ADD9	63	21	28
ADD8	64	20	24
ADD7	65	19	23
ADD6	66	18	22
ADD5	67	17	21
ADD4	69	13	14

8636A tbl 01A

**Pin Configuration**

Pin Name	84 pin PLCC	160 pin PQFP	208 pin PQFP
ADD3	70	11	12
ADD2	71	9	10
ADD1	72	7	8
ADD0	76	157	203
DATA7	2	137	178
DATA6	4	132	172
DATA5	6	129	169
DATA4	7	127	165
DATA3	8	124	162
DATA2	9	122	160
DATA1	13	115	149
DATA0	14	113	147
TDI	45	55	72
TDO	27	95	120
TCLK	44	57	74
TMS	43	59	76
nTRST	52	40	54
Dedicated Inputs	12, 31, 54, 73	6, 35, 87, 116	7, 45, 112, 150
VCCINT	17, 38, 59, 80	4, 5, 26, 85, 106	5, 6, 33, 110, 137
VCCIO	-	25, 41, 60, 70, 80, 107, 121, 140, 149, 160	32, 55, 78, 91, 102, 138, 159, 182, 193, 206
GND	5, 26, 47, 68	15, 16, 36, 37, 45, 51, 75, 84, 86, 96, 97, 117, 126, 131, 154	19, 20, 46, 47, 60, 67, 96, 109, 111, 124, 125, 151, 164, 171, 200
NC (No Connect)		2, 39, 82, 119	1, 2, 3, 16, 17, 18, 25, 26, 27, 34, 35, 36, 50, 51, 52, 53, 104, 105, 106, 107, 121, 122, 123, 130, 131, 132, 139, 140, 141, 154, 155, 156, 157, 208
<b>Total user I/O pins</b>	<b>64</b>	<b>114</b>	<b>132</b>

8636A tbl 01B

**DC Electrical Specifications**

**Absolute Maximum Ratings**

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	Supply voltage		-2.0	7.0	V
V <sub>I</sub>	DC input voltage <sup>[1]</sup>		-2.0	7.0	V
I <sub>OUT</sub>	DC output current, per pin		-25	25	mA
T <sub>STG</sub>	Storage temperature	No bias	-65	150	°C
T <sub>AMB</sub>	Ambient temperature	Under bias	-65	135	°C
T <sub>J</sub>	Junction temperature	Under bias		135	°C

8K tbl 02

**Recommended Operating Conditions <sup>[2]</sup>**

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CCINT</sub>	Supply voltage, internal logic and input buffers	Commercial Grade Devices	4.75	5.25	V
		Industrial Grade Devices	4.50	5.50	V
V <sub>CCIO</sub>	DC input voltage	5.0 volt commercial	4.75	5.25	V
		5.0 volt industrial	4.50	5.50	V
		3.3 volt operation	3.00	3.60	V
V <sub>I</sub>	Input voltage		0	V <sub>CCINT</sub>	V
V <sub>O</sub>	Output voltage		0	V <sub>CCIO</sub>	V
T <sub>A</sub>	Operating temperature	Commercial temperature range	0	70	°C
		Industrial temperature range	-40	85	°C
t <sub>R</sub>	Input signal rise time			40	ns
t <sub>F</sub>	Input signal fall time			40	ns
t <sub>RVCC</sub>	V <sub>CC</sub> rise time			100	ms

8K tbl 03

## DC Electrical Specifications cont.

### DC Electrical Characteristics (over the operating range)

Symbol	Parameter	Conditions	Min	Typ <sup>[3]</sup>	Max	Unit
$V_{IH}$	Input HIGH Voltage		2.0		$V_{CCINT} + 0.3$	V
$V_{IL}$	Input LOW Voltage		-0.3		0.8	V
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -4.0$ mA, $V_{CCIO} = V_{CCIO}[\text{Min}]$	2.4			V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 12.0$ mA, $V_{CCIO} = V_{CCIO}[\text{Min}]$			0.45	V
$I_{IN}$	Input Leakage Current	$V_I = V_{CC}$ or GND	-10		10	$\mu\text{A}$
$I_{OZ}$	Output Leakage Current	$V_O = V_{CC}$ or GND	-40		40	$\mu\text{A}$
$I_{CC0}$	Standby Current	$V_I = \text{GND}$ , no load		0.5	10	mA

8K tbl 04

### Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
$C_{IN}$	Input Capacitance	$V_{IN} = 0$ V, $f = 1.0$ MHz		10	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = 0$ V, $f = 1.0$ MHz		10	pF

8K tbl 05



**AC Electrical Specifications**

**I/O Element Timing Parameters <sup>[5]</sup>**

Symbol	Parameter	Conditions	Speed: -2		Speed: -3		Speed: -4		Unit
			Min	Max	Min	Max	Min	Max	
t <sub>IOD</sub>	IOE register data delay			0.7		0.8		0.9	ns
t <sub>IOC</sub>	IOE register control signal delay			1.7		1.8		1.9	ns
t <sub>IOE</sub>	Output enable delay			1.7		1.8		1.9	ns
t <sub>IOCO</sub>	IOE register clock to output delay			1.0		1.0		1.0	ns
t <sub>IOCOMB</sub>	IOE combinatorial delay			0.3		0.2		0.1	ns
t <sub>IOSU</sub>	IOE register setup time before clock		1.4		1.6		1.8		ns
t <sub>IOH</sub>	IOE register hold time after clock		0.0		0.0		0.0		ns
t <sub>IOCLR</sub>	IOE register clear delay			1.2		1.2		1.2	ns
t <sub>IN</sub>	Input pad and buffer delay			1.5		1.6		1.7	ns
t <sub>OD1</sub>	Output buffer and pad delay <sup>[6]</sup>	Slow Slew Rate = off, V <sub>CCIO</sub> = 5.0v, C <sub>L</sub> = 35 pF		1.1		1.4		1.7	ns
t <sub>OD2</sub>	Output buffer and pad delay <sup>[6]</sup>	Slow Slew Rate = off, V <sub>CCIO</sub> = 5.0v, C <sub>L</sub> = 35 pF		1.6		1.9		2.2	ns
t <sub>OD3</sub>	Output buffer and pad delay <sup>[6]</sup>	Slow Slew Rate = off, V <sub>CCIO</sub> = 5.0v, C <sub>L</sub> = 35 pF		4.6		4.9		5.2	ns
t <sub>ZX</sub>	Output buffer disable delay <sup>[6]</sup>	C <sub>L</sub> = 5 pF		1.4		1.6		1.8	ns
t <sub>ZX1</sub>	Output buffer and pad delay <sup>[6]</sup>	Slow Slew Rate = off, V <sub>CCIO</sub> = 5.0v, C <sub>L</sub> = 35 pF		1.4		1.6		1.8	ns
t <sub>ZX2</sub>	Output buffer and pad delay <sup>[6]</sup>	Slow Slew Rate = off, V <sub>CCIO</sub> = 5.0v, C <sub>L</sub> = 35 pF		1.6		2.1		2.3	ns
t <sub>ZX3</sub>	Output buffer and pad delay <sup>[6]</sup>	Slow Slew Rate = off, V <sub>CCIO</sub> = 5.0v, C <sub>L</sub> = 35 pF		4.9		5.1		5.3	ns

8K tbl 06C

**External Timing Parameters<sup>[4]</sup>**

Symbol	Parameter	Conditions	Speed: -2		Speed: -3		Speed: -4		Unit
			Min	Max	Min	Max	Min	Max	
t <sub>DRR</sub>	Register to register delay via four LEs, three row interconnects, and four local interconnects			16		20		25	ns
t <sub>ODH</sub>	Output data hold time after clock		1.0		1.0		1.0		ns

8K tbl 07B

**AC Electrical Specifications cont.****Logic Element Timing Parameters<sup>[5]</sup>**

Speed: -2      Speed: -3      Speed: -4

Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	Unit
$t_{LUT}$	Look up table delay for data-in			2.0		2.3		3.0	ns
$t_{CLUT}$	Look up table delay for carry-in			0.0		0.2		0.1	ns
$t_{RLUT}$	Look up table delay for LE register feedback			0.9		1.6		1.6	ns
$t_{GATE}$	Cascade gate delay			0.0		0.0		0.0	ns
$t_{CASC}$	Cascade chain routing delay			0.6		0.7		0.9	ns
$t_{CICO}$	Carry-in to carry-out delay			0.4		0.5		0.6	ns
$t_{CGEN}$	Data-in to carry-out delay			0.4		0.9		0.8	ns
$t_{CGENR}$	LE register feedback to carry-out delay			0.9		1.4		1.5	ns
$t_C$	LE register control signal delay			1.6		1.8		2.4	ns
$t_{CH}$	Clock high time		1.7		1.7		2.7		ns
$t_{CL}$	Clock low time		1.7		1.7		2.7		ns
$t_{CO}$	LE register clock-to-output delay			0.4		0.5		0.6	ns
$t_{COMB}$	Combinatorial delay			0.4		0.5		0.6	ns
$t_{SU}$	LE register setup time before clock		0.8		1.0		1.1		ns
$t_H$	LE register hold time after clock		0.9		1.1		1.4		ns
$t_{PRE}$	LE register preset delay			0.6		0.7		0.8	ns
$t_{CLR}$	LE register clear delay			0.6		0.7		0.8	ns

8K tbl 08B

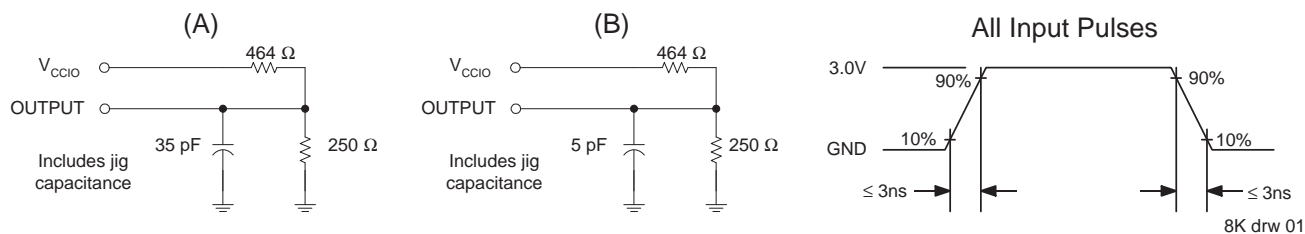
**Interconnect Timing Parameters<sup>[5]</sup>**

Speed: -2      Speed: -3      Speed: -4

Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	Unit
$t_{LABCASC}$	Cascade delay between LEs in different LABs			0.3		0.4		0.4	ns
$t_{LABCARRY}$	Carry delay between LEs in different LABs			0.3		0.4		0.4	ns
$t_{LOCAL}$	LAB local interconnect delay			0.5		0.5		0.7	ns
$t_{ROW}$	Row interconnect routing delay			5.0		5.0		5.0	ns
$t_{COL}$	Column interconnect routing delay			3.0		3.0		3.0	ns
$t_{DIN_C}$	Dedicated input to LE control delay			5.0		5.0		5.5	ns
$t_{DIN_D}$	Dedicated input to LE data delay			7.0		7.0		7.5	ns
$t_{DIN_IO}$	Dedicated input to IOE control delay			5.0		5.0		5.5	ns

8K tbl 09B

AC Test Conditions



A: Test fixture set-up A is for general testing.  
 B: Test fixture set-up B is for high Z testing ( $t_{ZX\#}$ ).

Notes to Tables

1. During transitions, inputs may undershoot to -2.0V for periods shorter than 20ns. Otherwise, minimum DC input voltage is -0.3V.
2. The following devices do not have  $V_{CCIO}$  pins: CL8282A, CL8452A. For these devices, all references to  $V_{CCIO}$  should be changed to  $V_{CCINT}$
3. Typical values are at  $V_{CC}$  of 5.0 volts and ambient temperature of 25 °C.
4. Guaranteed but not tested. Characterized initially, and after any design changes which may affect these parameters.
5. Internal timing delays are based on characterization, and cannot be explicitly tested. Internal timing parameters should be used for performance estimation only.
6. Use AC Test Conditions set-up B for these parameters.

Revision History

- 16 Jan. 1998: Created new document
- 31 Jul. 1999: Recompiled databook, 8820 package update.
- 29 Nov. 1999: Remove reference to the 8282AV device which is not supported.
- 01 Dec. 2000: Review and reprint.

Ordering Information

Part Number	Temperature Range	Package Type	Speed	Altera Equivalent
CL8636ALC84-4	Commercial	84-pin PLCC	-4 (slowest)	EPF8636ALC84-4
CL8636ALC84-3			-3 (fastest)	EPF8636ALC84-3
CL8636AQC160-4		160-pin Plastic QFP	-4 (slowest)	EPF8636AQC160-4
CL8636AQC160-3			-3 (fastest)	EPF8636AQC160-3
CL8636AQC208-4			-4 (slowest)	EPF8636AQC208-4
CL8636AQC208-3		208-pin Plastic QFP	-3	EPF8636AQC208-3
CL8636AQC208-2	-2 (fastest)		EPF8636AQC208-2	
CL8636ALI84-4	Industrial	84-pin PLCC	-4	EPF8636ALI84-4

8636A tbl 05

