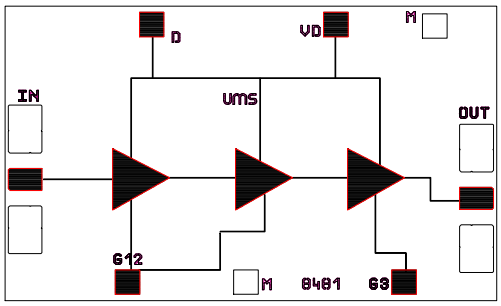
36-44GHz Low Noise Amplifier
Self biased
GaAs Monolithic Microwave IC

Description

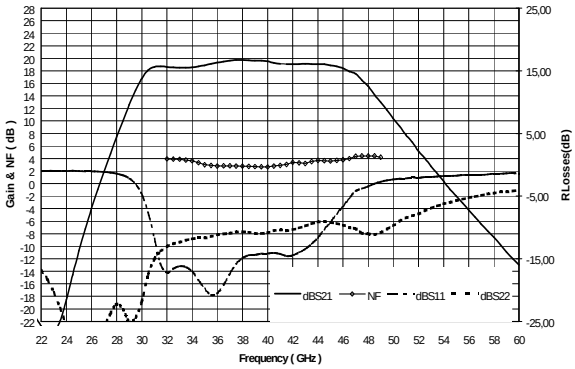
The circuit is a three-stage self biased wide band monolithic low noise amplifier, designed for 36GHz to 44GHz point to point and point to multipoint communication **.**

The circuit is manufactured with a standard pHEMT process: 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is supplied in chip form.



Main Features

- Broad band performance 36-44GHz
- 3dB noise figure
- 19dB gain, ± 0.5dB gain flatness
- Low DC power consumption, 45mA
- 20dBm 3rd order intercept point
- Chip size : 1.670 x 0.970x 0.1mm



Main Characteristics

On wafer typical measurement

Tamb = +25°C

Symbol	Parameter	Min	Typ	Max	Unit
NF	Noise figure at freq : 40GHz		3	4	dB
G	Gain	17	19		dB
ΔG	Gain flatness		± 0.5	± 1	dB

ESD Protections : Electrostatic discharge sensitive device observe handling precautions !

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Electrical Characteristics

Tamb = +25℃, Vd = +3,5V (On wafer)

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	36		44	Ghz
G	Gain (1)	17	19		dB
ΔG	Gain flatness (1)		± 0.5	± 1	dB
NF	Noise figure (1) (freq: 36-40 GHz)		3	4	dB
VSWRin	Input VSWR (1)		2.5:1	3.0:1	
VSWRout	Ouput VSWR (1)		2:5:1	3.0:1	
IP3	3rd order intercept point		20		dBm
P1dB	Output power at 1dB gain compression	8	10		dBm
Id	Drain bias current (2)		45	75	mA

(1)These values are representative of wafer measurements without bonding wire at the RF ports.
(2) This current is the typical value for low noise and low current consumption biasing:
Vd=3.5V, Vg12 and Vg3 not connected.

Absolute Maximum Ratings (3)

Tamb = +25℃

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage (5)	4	V
Vg	Vg12 and Vg3 max	+1	V
Id	Drain current	75	mA
Pin	Maximum peak input power overdrive (4)	15	dBm
Top	Operating temperature range	-40 to +85	℃
Tstg	Storage temperature range	-55 to +125	℃

(3) Operation of this device above anyone of these paramaters may cause permanent damage.
(4) Duration < 1s.
(5) See chip biasing options page 9

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Typical Result

Chip Typical Response (On wafer Scattering parameters) :

Tamb = +25°C Vd=3.5V Id=+42mA

F(GHz)	S11		S12		S21		S22	
	mod	Pha	mod	Pha	mod	Pha	mod	Pha
	dB	deg	dB	deg	dB	deg	dB	deg
2,00	-4,39	-56,73	-75,42	44,36	-37,71	179,84	-0,11	-26,01
4,00	-3,92	-86,19	-68,73	-0,07	-38,99	144,86	-0,41	-51,53
6,00	-3,01	-111,00	-68,42	-40,89	-38,00	82,75	-0,87	-75,92
8,00	-2,33	-132,18	-62,78	-61,43	-31,40	-24,55	-1,53	-98,47
10,00	-1,87	-149,64	-58,07	-92,78	-22,10	-68,40	-2,33	-120,41
12,00	-1,57	-164,59	-54,16	-118,46	-15,19	-121,90	-3,50	-140,34
14,00	-1,35	-177,94	-51,89	-167,25	-11,48	-177,68	-4,77	-158,48
16,00	-1,25	169,65	-52,93	158,44	-10,44	129,48	-6,27	-176,02
18,00	-1,16	157,50	-51,04	165,85	-11,48	84,35	-8,13	163,01
20,00	-1,09	144,51	-49,77	164,40	-15,47	49,64	-12,66	138,91
22,00	-1,01	130,06	-48,14	114,15	-22,72	64,72	-16,87	134,36
24,00	-0,99	113,68	-47,48	73,88	-18,51	144,50	-25,93	129,23
25,00	-1,00	104,41	-48,97	61,97	-10,74	152,58	-35,08	177,75
26,00	-1,05	93,20	-48,69	52,80	-4,00	142,49	-27,71	-121,39
27,00	-1,15	80,32	-48,51	18,34	1,96	125,50	-25,75	-116,09
28,00	-1,42	63,49	-49,95	6,77	7,45	100,83	-22,24	-115,84
29,00	-2,17	40,77	-47,16	-37,23	12,59	70,07	-25,05	-110,45
30,00	-4,74	10,16	-44,24	-94,27	16,78	28,35	-21,79	-68,00
31,00	-11,78	-12,14	-41,60	-147,89	18,62	-19,04	-15,03	-77,79
32,00	-17,20	17,23	-41,18	175,51	18,62	-57,49	-13,03	-96,11
33,00	-16,20	20,67	-41,81	148,47	18,49	-87,41	-12,36	-107,46
34,00	-17,00	-2,28	-39,78	125,02	18,57	-113,67	-11,84	-116,00
35,00	-19,78	-48,40	-39,87	112,63	18,87	-138,52	-11,68	-122,31
36,00	-20,49	-119,64	-39,25	98,45	19,30	-164,01	-11,17	-127,64
37,00	-17,37	-175,00	-37,96	86,45	19,60	170,44	-10,94	-133,38
38,00	-14,90	148,19	-36,53	76,61	19,70	143,82	-10,68	-140,12
39,00	-14,38	119,40	-35,30	57,46	19,60	118,71	-10,97	-145,87
40,00	-14,17	99,78	-33,63	38,26	19,51	94,31	-10,84	-148,12
41,00	-14,23	81,41	-33,70	20,37	19,12	70,56	-10,39	-154,43
42,00	-14,45	68,04	-32,62	5,49	19,06	46,84	-10,36	-159,30
43,00	-13,44	54,31	-32,01	-15,03	19,10	22,80	-9,76	-166,74
44,00	-11,65	37,44	-31,08	-35,85	19,06	-3,12	-9,13	178,41
45,00	-9,14	15,96	-30,72	-59,51	18,88	-30,61	-9,22	158,00
46,00	-6,61	-8,98	-31,56	-86,95	18,39	-60,43	-9,63	130,78
47,00	-4,21	-34,87	-33,12	-117,26	17,52	-91,46	-10,19	94,17
48,00	-3,45	-62,16	-35,95	-136,86	15,52	-122,46	-11,03	49,86
49,00	-2,71	-84,52	-37,02	-153,94	13,00	-148,98	-10,81	7,88
50,00	-2,35	-102,45	-38,27	165,40	10,38	-171,73	-9,71	-23,44

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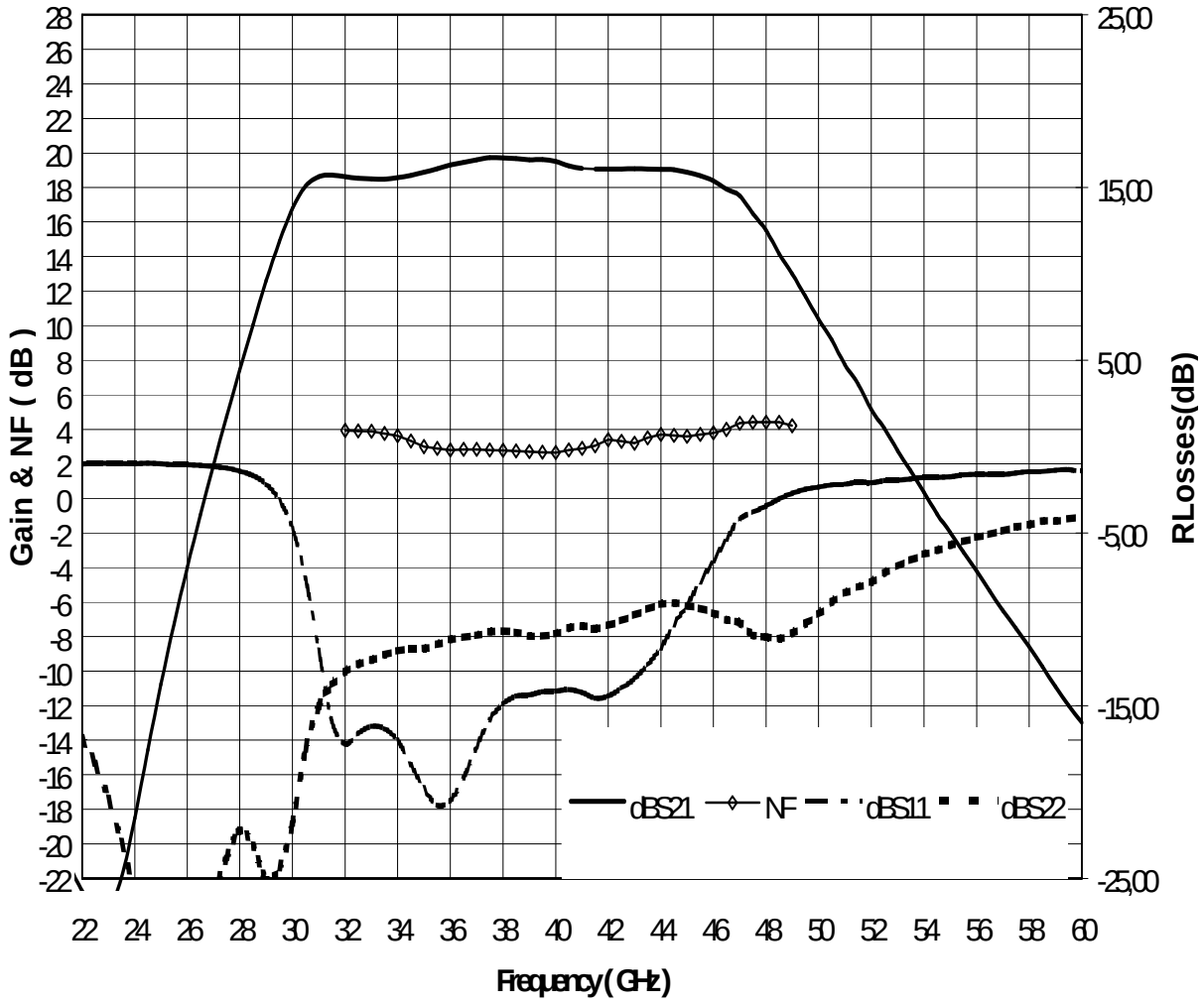
Typical Results

Chip Typical Response (On wafer Scattering parameters)

Tamb = +25°C
Vd = 3.5V Vg12& Vg3 not connected; Id = 42mA



Typical Gain , Matching and Noise Figure (Measurements on wafer.)

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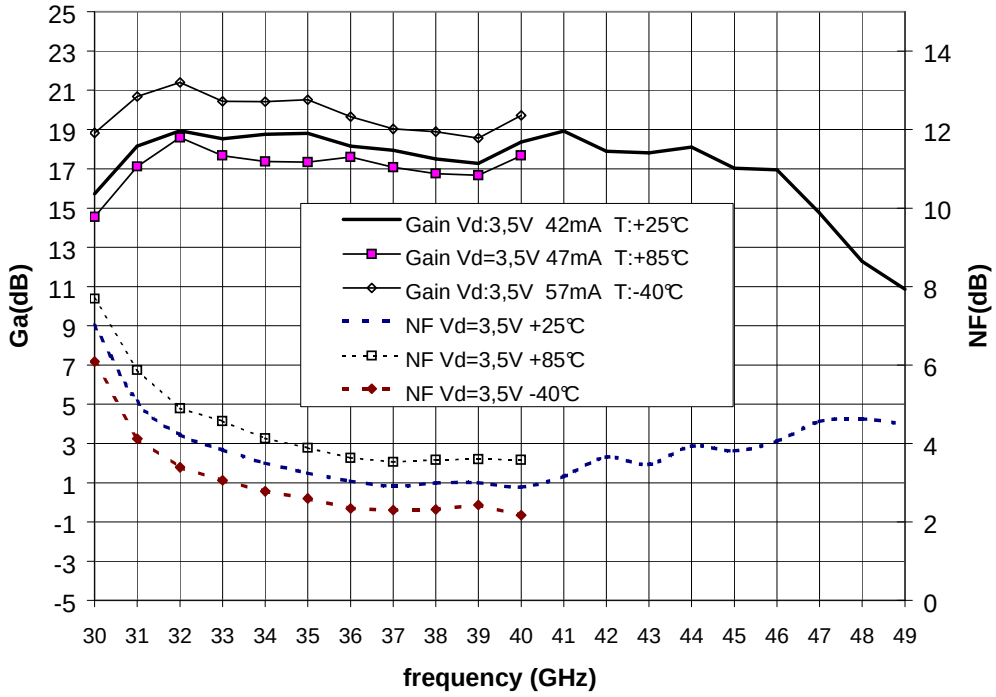
Typical Results

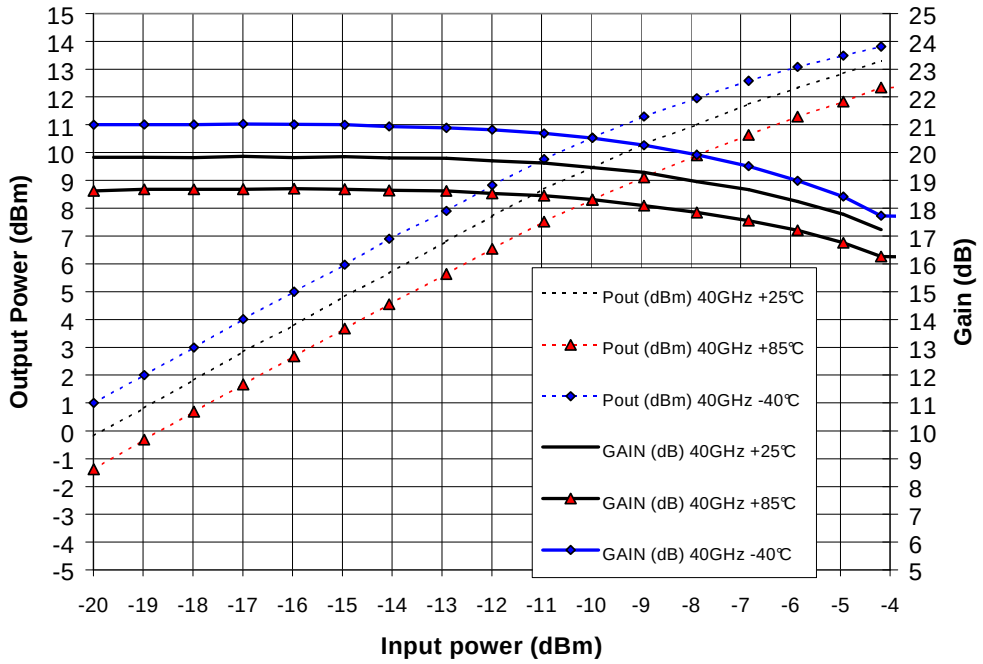
Chip Typical Response (In test Jig)

Vd = 3.5V Vg12& Vg3 not connected; Id = 42mA

Typical gain slope versus temperature : -0.025dB/°C
Typical noise figure slope versus temperature : 0.011dB/°C



Typical Gain and NF versus temperature (measurements in test jig)



Typical Gain & Pout versus temperature (measurements in test-jig)

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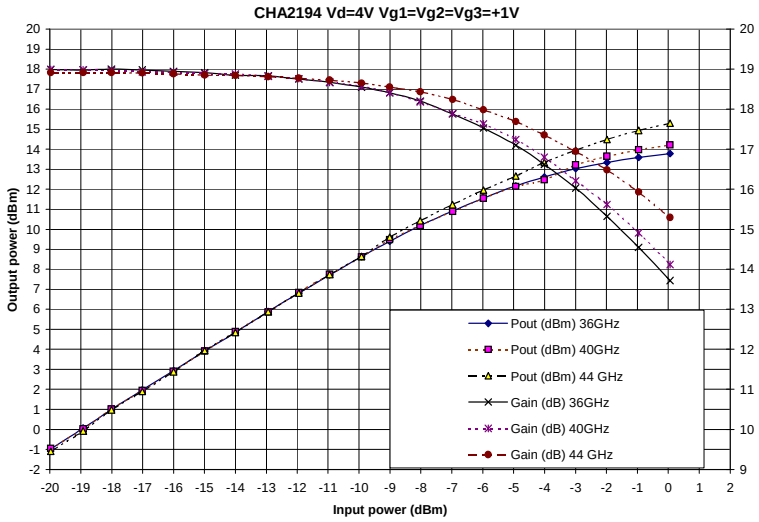
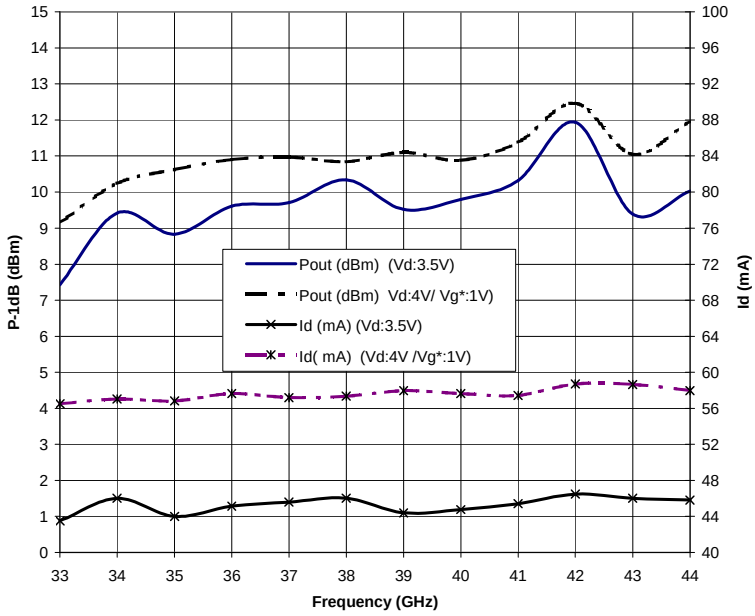
Circuit Typical Response (In test-Jig)



Typical Output Power (Measurement in test Jig)

Tamb = +25°C Vd=4V and Vg12=Vg3=1V
These values are representative of the package assembly with input and output bonding.



Typical Output power –1dB. (Measurement in test Jig)

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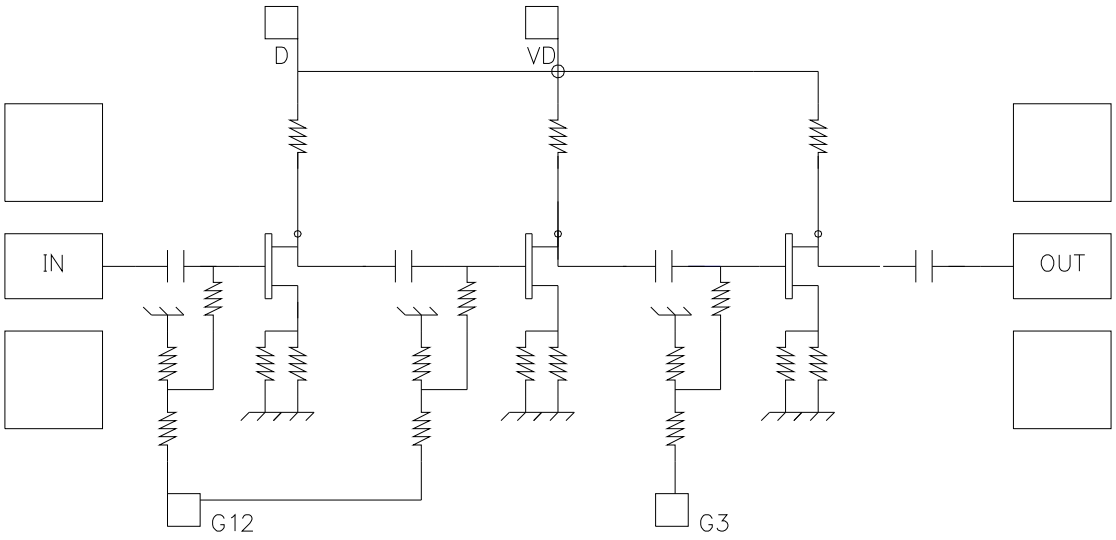
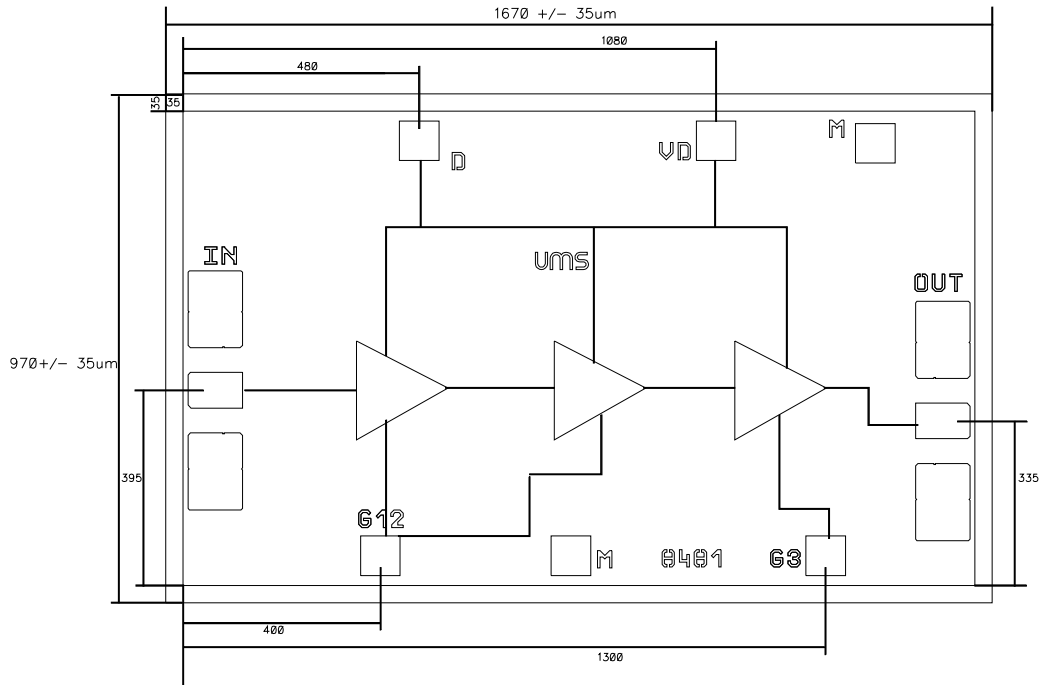
Chip schematic and Pad Identification (see also page 9)



Pad Size :80/80µm, chip thickness 100um
Dimensions : 1670µm x 970µm ± 35µm



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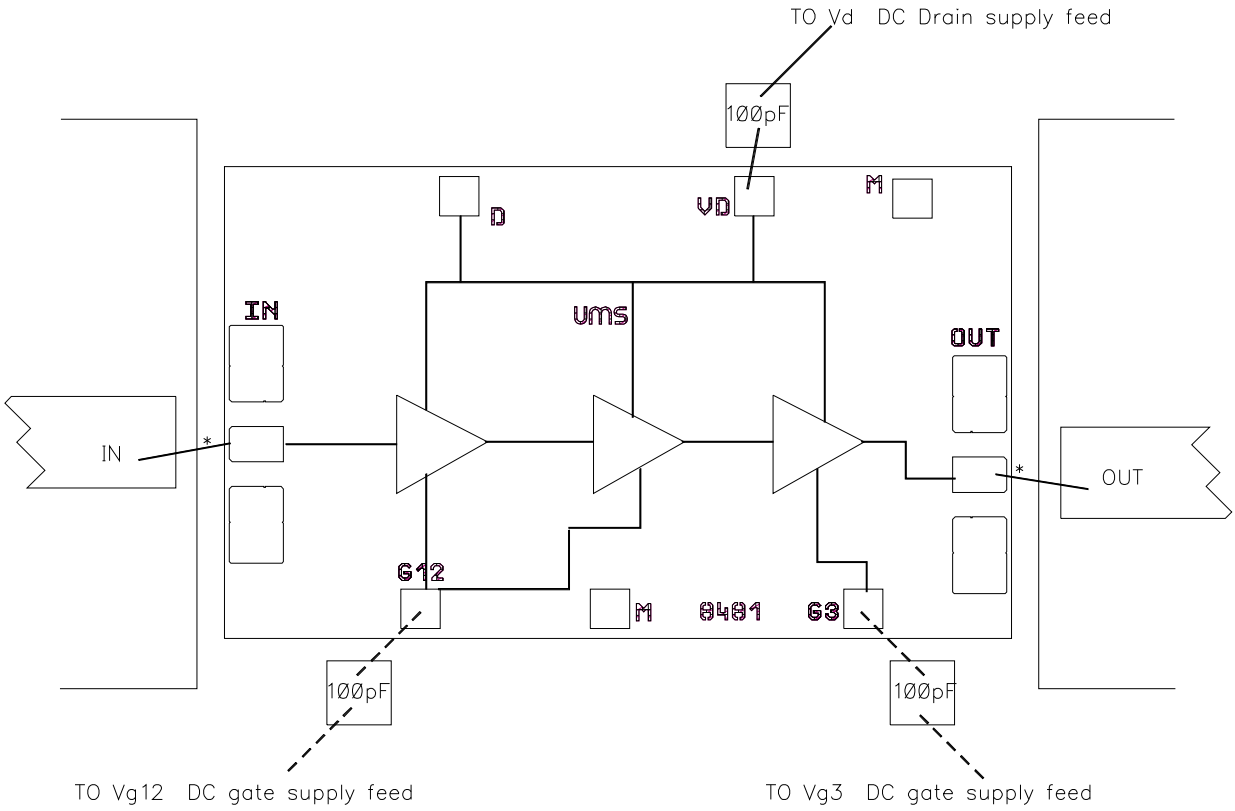
Typical Chip Assembly



- * Nominal Input and Output bonding length: 0.3 to 0.38nH for one 25µm bond wire.
- Chip backside is DC and RF bonding grounded

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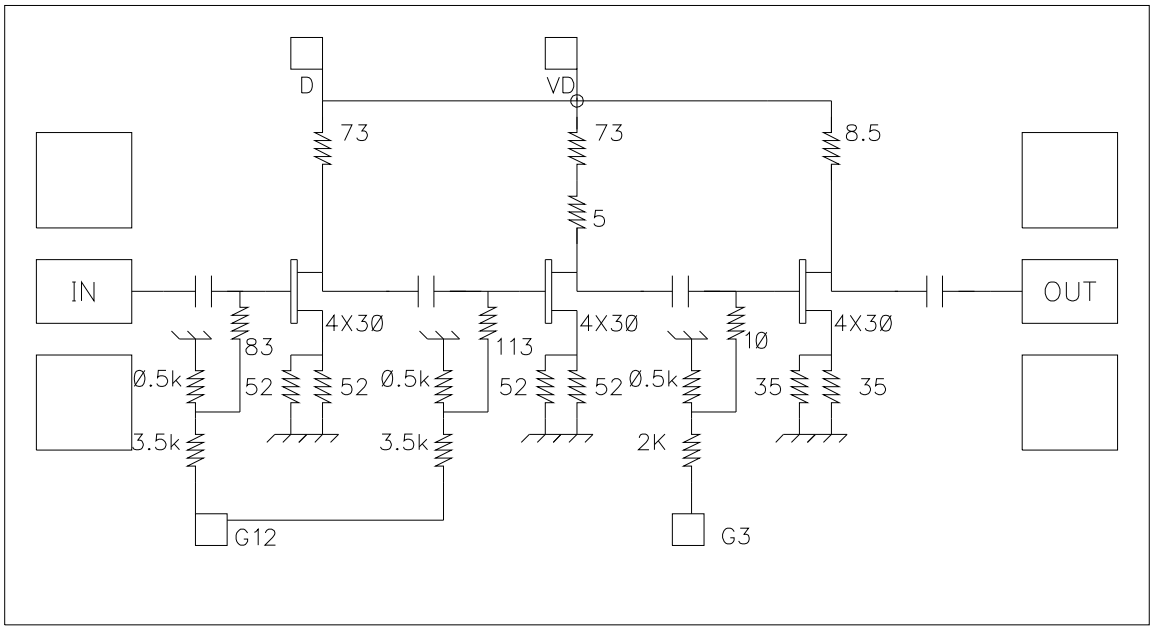
Chip Biasing options

Internal DC schematic



This chip is self-biased, and flexibility is provided by the access to positive Vg.
The internal DC electrical schematic is given in order to use these pads in a safe way.

Absolute recommandations

N°1: Do not exceed Vds* = 3,5 Volt (internal Drain to Source voltage).
N°2: Do not bias in such a way that Vgs* becomes po sitive. (internal Gate to Source voltage)

Typical biasing table and Typical results in test Jig at 40 GHz

40GHz IN TEST Jig	Vds (V)	Vg12 (V)	Vg3 (V)	Id (mA)	Typical NF(dB)	Typical Gain (dB)	Typical P-1dB (dB)	Typical Psat (dB)
Standard	3.5	NC	NC	42	2.9	19	10	12
Low Noise High linearity	4	1	1	60	2,95	20	11	14
Low noise /low current consumption	3,5	-1	-1	30	3	17,5	8	11
Switch off	3.5	-8	-5	0	X	X	X	X

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Ordering Information

Chip form : CHA2194-99F/00

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