

NT256D72S4PA0GR

256MB : 32M x 72

Registered DDR SDRAM DIMM



184pin One Bank Registered DDR SDRAM MODULE Based on 32Mx4 DDR SDRAM

Features

- 184-Pin Registered 8-Byte Dual In-Line Memory Module
- 32Mx72 Double Data Rate (DDR) SDRAM DIMM
- Performance :

Speed Sort	PC1600			PC2100			Unit
	- 8B	- 75B	- 7K				
DIMM CAS Latency	3	3.5	3				
f CK Clock Frequency	100	133	133				MHz
t CK Clock Cycle	10	7.5	7.5				ns
f DQ DQ Burst Frequency	200	266	266				MHz

- Intended for 100 MHz and 133 MHz applications
- Inputs and outputs are SSTL-2 compatible
- V_{DD} = 2.5Volt ± 0.2, V_{DDQ} = 2.5Volt ± 0.2
- Single Pulsed RAS interface
- SDRAMs have 4 internal banks for concurrent operation
- Module has one physical bank
- Differential clock inputs
- Data is read or written on both clock edges

- Bi-directional data strobe with one clock cycle preamble and one-half clock post-amble
- Address and control signals are fully synchronous to positive clock edge
- Programmable Operation:
 - DIMM CAS Latency: 3, 3.5
 - Burst Type: Sequential or Interleave
 - Burst Length: 2, 4, 8
 - Operation: Burst Read and Write
- Auto Refresh (CBR) and Self Refresh Modes
- Automatic and controlled precharge commands
- 12/11/2 Addressing (row/column/bank)
- 15.625 μs Max. Average Periodic Refresh Interval
- Serial Presence Detect
- Gold contacts
- SDRAMs in 66-pin TSOP Type II Package

Description

NT256D72S4PA0GR is a registered 184-Pin Double Data Rate (DDR) Synchronous DRAM Dual In-Line Memory Module (DIMM), organized as a one-bank high-speed memory array. The 32Mx72 module is a single-bank DIMM that uses eighteen 32Mx4 DDR SDRAMs in 400 mil TSOP packages. The DIMM achieves high-speed data transfer rates of up to 266MHz. The DIMM is intended for use in applications operating from 100 MHz to 133 MHz clock speeds with data rates of 200 to 266 MHz. Clock enable CKE0 controls all devices on the DIMM.

Prior to any access operation, the device CAS latency and burst type/ length/operation type must be programmed into the DIMM by address inputs A0-A11 and I/O inputs BA0 and BA1 using the mode register set cycle.

These DIMMs are manufactured using raw cards developed for broad industry use as reference designs. The use of these common design files minimizes electrical variation between suppliers.

The DIMM uses serial presence detects implemented via a serial EEPROM using the two-pin IIC protocol. The first 128 bytes of serial PD data are programmed and locked during module assembly. The last 128 bytes are available to the customer.

All NANYA 184 DDR SDRAM DIMMs provide a high-performance, flexible 8-byte interface in a 5.25" long space-saving footprint.

Ordering Information

Part Number	Speed		Organization	Leads	Power
	Component	Module			
NT256D72S4PA0GR -7K	143MHz (7ns @ CL = 2.5)	DDR266A PC2100	32Mx72	Gold	2.5V
	133MHz (7.5ns @ CL= 2)				
NT256D72S4PA0GR -75B	133MHz (7.5ns @ CL= 2.5)	DDR266B PC2100			
	100MHz (10ns @ CL = 2)				
NT256D72S4PA0GR - 8B	125MHz (8ns @ CL = 2.5)	DDR200 PC1600			
	100MHz (10ns @ CL = 2)				



Pin Description

CK0, $\overline{\text{CK0}}$	Differential Clock Inputs	DQ0-DQ63	Data input/output
CKE0	Clock Enable	CB0-CB7	Check Bit Data Input/Output
$\overline{\text{RAS}}$	Row Address Strobe	DQS0-DQS17	Bidirectional data strobes
$\overline{\text{CAS}}$	Column Address Strobe	VDD	Power (2.5V)
$\overline{\text{WE}}$	Write Enable	VDDQ	Supply voltage for DQs(2.5V)
$\overline{\text{S0}}$	Chip Selects	VSS	Ground
A0-A9, A11	Address Inputs	NC	No Connect
A10/AP	Address Input/Autoprecharge	SCL	Serial Presence Detect Clock Input
BA0, BA1	SDRAM Bank Address Inputs	SDA	Serial Presence Detect Data input/output
$\overline{\text{RESET}}$	Reset pin	SA0-2	Serial Presence Detect Address Inputs
VREF	Ref. Voltage for SSTL_2 inputs	VDDSPD	Serial EEPROM positive power supply(2.5V)
VDDID	VDD Identification flag.		

Pinout

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VREF	32	A5	62	VDDQ	93	VSS	124	VSS	154	$\overline{\text{RAS}}$
2	DQ0	33	DQ24	63	$\overline{\text{WE}}$	94	DQ4	125	A6	155	DQ45
3	VSS	34	VSS	64	DQ41	95	DQ5	126	DQ28	156	VDDQ
4	DQ1	35	DQ25	65	$\overline{\text{CAS}}$	96	VDDQ	127	DQ29	157	$\overline{\text{S0}}$
5	DQS0	36	DQS3	66	VSS	97	DQS9	128	VDDQ	158	NC
6	DQ2	37	A4	67	DQS5	98	DQ6	129	DQS12	159	DQS14
7	VDD	38	VDD	68	DQ42	99	DQ7	130	A3	160	VSS
8	DQ3	39	DQ26	69	DQ43	100	VSS	131	DQ30	161	DQ46
9	NC	40	DQ27	70	VDD	101	NC	132	VSS	162	DQ47
10	$\overline{\text{RESET}}$	41	A2	71	NC	102	NC	133	DQ31	163	NC
11	VSS	42	VSS	72	DQ48	103	NC	134	CB4	164	VDDQ
12	DQ8	43	A1	73	DQ49	104	VDDQ	135	CB5	165	DQ52
13	DQ9	44	CB0	74	VSS	105	DQ12	136	VDDQ	166	DQ53
14	DQS1	45	CB1	75	NC	106	DQ13	137	CK0	167	NC
15	VDDQ	46	VDD	76	NC	107	DQS10	138	$\overline{\text{CK0}}$	168	VDD
16	NC	47	DQS8	77	VDDQ	108	VDD	139	VSS	169	DQS15
17	NC	48	A0	78	DQS6	109	DQ14	140	DQS17	170	DQ54
18	VSS	49	CB2	79	DQ50	110	DQ15	141	A10	171	DQ55
19	DQ10	50	VSS	80	DQ51	111	NC	142	CB6	172	VDDQ
20	DQ11	51	CB3	81	VSS	112	VDDQ	143	VDDQ	173	NC
21	CKE0	52	BA1	82	VDDID	113	NC	144	CB7	174	DQ60
22	VDDQ	KEY		83	DQ56	114	DQ20	KEY		175	DQ61
23	DQ16	53	DQ32	84	DQ57	115	NC	145	VSS	176	VSS
24	DQ17	54	VDDQ	85	VDD	116	VSS	146	DQ36	177	DQS16
25	DQS2	55	DQ33	86	DQS7	117	DQ21	147	DQ37	178	DQ62
26	VSS	56	DQS4	87	DQ58	118	A11	148	VDD	179	DQ63
27	A9	57	DQ34	88	DQ59	119	DQS11	149	DQS13	180	VDDQ
28	DQ18	58	VSS	89	VSS	120	VDD	150	DQ38	181	SA0
29	A7	59	BA0	90	NC	121	DQ22	151	DQ39	182	SA1
30	VDDQ	60	DQ35	91	SDA	122	A8	152	VSS	183	SA2
31	DQ19	61	DQ40	92	SCL	123	DQ23	153	DQ44	184	VDDSPD

Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0	(SSTL)	Positive Edge	The positive line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL. All the DDR SDRAM address and control inputs are sampled on the rising edge of their associated clocks.
$\overline{\text{CK0}}$	(SSTL)	Negative Edge	The negative line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL.
CKE0	(SSTL)	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
$\overline{\text{S0}}$	(SSTL)	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	(SSTL)	Active Low	When sampled at the positive rising edge of the clock, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$ define the operation to be executed by the SDRAM.
VREF	Supply		Reference voltage for SSTL-2 inputs
VDDQ	Supply		Isolated power supply for the DDR SDRAM output buffers to provide improved noise immunity
BA0, BA1	(SSTL)	-	Selects which SDRAM bank is to be active.
A0 - A9, A11 A10/AP	(SSTL)	-	During a Bank Activate command cycle, A0-A11 defines the row address (RA0-RA11) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A10 defines the column address (CA0-CA10) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke Autoprecharge operation at the end of the Burst Read or Write cycle. If AP is high, autoprecharge is selected and BA0/BA1 define the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0/BA1 to control which bank(s) to precharge. If AP is high all 4 banks will be precharged regardless of the state of BA0/BA1. If AP is low, then BA0/BA1 are used to define which bank to pre-charge.
DQ0 - DQ63,	(SSTL)	-	Data and Check Bit input/output pins operate in the same manner as on conventional DRAMs.
DQ0 – DQ63 CB0 – CB7	(SSTL)	Active High	Data and Check Bit Input/Output pins. Check bits are only applicable on the x72 DIMM configurations.
VDD , VSS	Supply		Power and ground for the DDR SDRAM input buffers and core logic
DQS0 – DQS17	(SSTL)	Negative and Positive Edge	Data strobe for input and output data
$\overline{\text{RESET}}$	(LVC-MOS)	Active Low	
SA0 – SA2		-	Address inputs. Connected to either VDD or VSS on the system board to configure the Serial Presence Detect EEPROM address.
SDA		-	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V DD to act as a pullup.
SCL		-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V DD to act as a pullup.
V DDSPD	Supply		Serial EEPROM positive power supply.

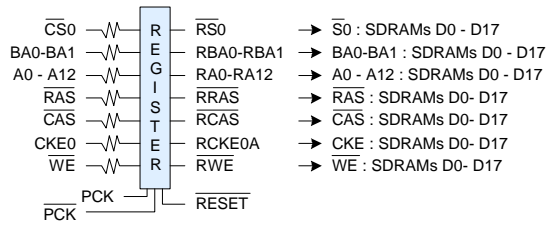
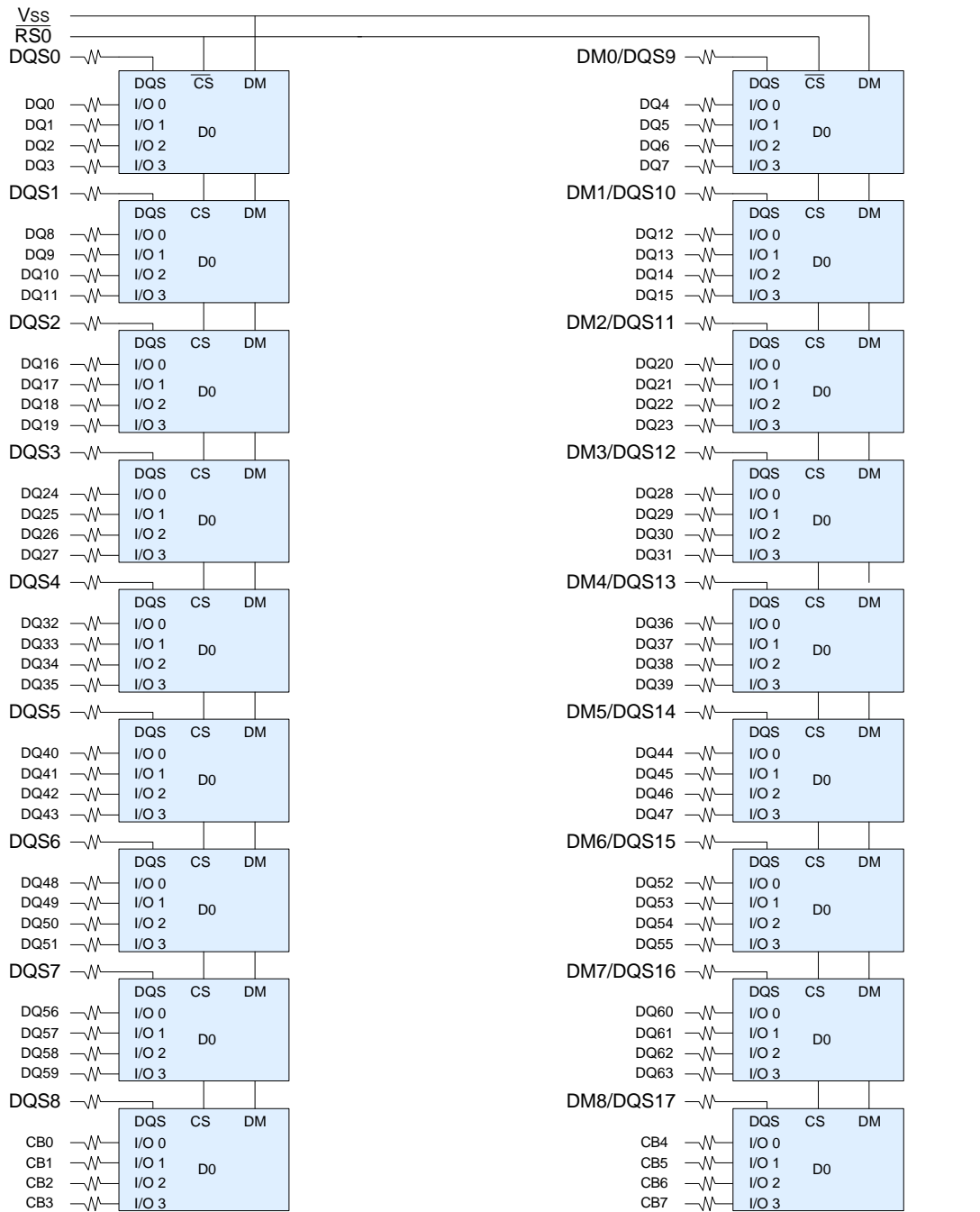
NT256D72S4PA0GR

256MB : 32M x 72

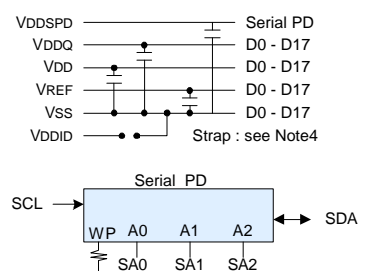
Registered DDR SDRAM DIMM



Functional Block Diagram (1 Bank, 32Mx4 DDR SDRAMs)



- Notes :
1. DQ-to-I/O wiring may be changed within a byte
 2. DQ/DQS/DM/CKE/CS relationships are maintained as shown.
 3. DQ/DQS resistors are 22 Ohms.
 4. VDDID strap connections (for memory device VDD, VDDQ):
STRAP OUT (OPEN): VDD = VDDQ
STRAP IN (VSS): VDD 1 VDDQ.
 5. Address and control resistors are 22Ohms.



* CK0, CK0 ----- PLL*
* Wire per Clock Loading Table/Wiring Diagrams



Serial Presence Detect -- Part 1 of 2

32Mx72 1 BANK REGISTERED DDR SDRAM DIMM based on 32Mx4, 4Banks, 4K Refresh, 2.5V DDR SDRAMs with SPD

Byte	Description	SPD Entry Value			Serial PD Data Entry (Hexadecimal)			Note
		DDR266A -7K	DDR266B -75B	DDR200 -8B	DDR266A -7K	DDR266B -75	DDR200 -8B	
0	Number of Serial PD Bytes Written during Production	128			80			
1	Total Number of Bytes in Serial PD device	256			08			
2	Fundamental Memory Type	SDRAM DDR			07			
3	Number of Row Addresses on Assembly	12			0C			
4	Number of Column Addresses on Assembly	11			0B			
5	Number of DIMM Bank	1			01			
6.	Data Width of Assembly	X72			48			
7	Data Width of Assembly (cont')	X72			00			
8	Voltage Interface Level of this Assembly	SSTL 2.5V			04			
9	DDR SDRAM Device Cycle Time at CL=2.5	7ns	7.5ns	8ns	70	75	80	
10	DDR SDRAM Device Access Time from Clock at CL=2.5	0.75ns	0.75ns	0.8ns	75	75	80	
11	DIMM Configuration Type	ECC			02			
12	Refresh Rate/Type	15.625us / SR			80			
13	Primary DDR SDRAM Width	X4			04			
14	Error Checking DDR SDRAM Device Width	X4			04			
15	DDR SDRAM Device Attr: Min CLK Delay, Random Col Access	1 Clock			01			
16	DDR SDRAM Device Attributes: Burst Length Supported	2,4,8			0E			
17	DDR SDRAM Device Attributes: Number of Device Banks	4			04			
18	DDR SDRAM Device Attributes: CAS Latencies Supported	2/2.5	2/2.5	2/2.5	0C	0C	0C	
19	DDR SDRAM Device Attributes: CS Latency	0			01			
20	DDR SDRAM Device Attributes: WE Latency	1			02			
21	DDR SDRAM Device Attributes:	Differential Clock, PLL, REGISTER			26			
22	DDR SDRAM Device Attributes: General	+/-0.2V Voltage Tolerance			00			
23	Minimum Clock Cycle at CL=2	7.5ns	10ns	10ns	75	A0	A0	
24	Maximum Data Access Time from Clock at CL=2	0.75ns	0.75ns	0.8ns	75	75	80	
25	Minimum Clock Cycle Time at CL=1	N/A			00			
26	Maximum Data Access Time from Clock at CL=1	N/A			00			
27	Minimum Row Precharge Time(trP)	20ns	20ns	20ns	50	50	50	
28	Minimum Row Active to Row Active delay (tRRD)	15ns	15ns	15ns	3C	3C	3C	
29	Minimum RAS to CAS delay (trCD)	20ns	20ns	20ns	50	50	50	
30	Minimum RAS Pulse Width (tRAS)	45ns	45ns	50ns	2D	2D	32	
31	Module Bank Density	256MB			40			
32	Address and Command Setup Time Before Clock	0.9ns	0.9ns	1.1ns	90	90	B0	
33	Address and Command Hold Time After Clock	0.9ns	0.9ns	1.1ns	90	90	B0	
34	Data Input Setup Time Before Clock	0.5ns	0.5ns	0.6ns	50	50	60	
35	Data Input Hold Time After Clock	0.5ns	0.5ns	0.6ns	50	50	60	
36-61	Reserved	Undefined			00			
62	SPD Revision	Initial	Initial	Initial	00	00	00	
63	Checksum Data				DF	0F	95	

NT256D72S4PA0GR

256MB : 32M x 72

Registered DDR SDRAM DIMM



Serial Presence Detect -- Part 2 of 2

64Mx72 1 BANK REGISTERED DDR SDRAM DIMM based on 64Mx4, 4Banks, 8K Refresh, 2.5V DDR SDRAMs with SPD

Byte	Description	SPD Entry Value			Serial PD Data Entry (Hexadecimal)			Note
		DDR266A -7K	DDR266B -75B	DDR200 -8B	DDR266A -7K	DDR266B -75	DDR200 -8B	
64-71	Manufacturer's JEDED ID Code	NANYA			7F7F7F0B00000000			
72	Module Manufacturing Location	N/A			00			
73-90	Module Part number	N/A	N/A	N/A	00	00	00	
91-92	Module Revision Code	N/A			00			
93-94	Module Manufacturing Data	Year/Week Code			yy/ww			1,2
95-98	Module Serial Number	Serial Number			00			
99-255	Reserved	Undefined			00			

1. yy= Binary coded decimal year code, 0-99(Decimal), 00-63(Hex)
2. ww= Binary coded decimal year code, 01-52(Decimal), 01-34(Hex)

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{IN}, V_{OUT}	Voltage on I/O pins relative to Vss	-0.5 to VDDQ+0.5	V
V_{IN}	Voltage on Input relative to Vss	-0.5 to +2.7	V
V_{DD}	Voltage on VDD supply relative to Vss	-0.5 to +2.7	V
V_{DDQ}	Voltage on VDDQ supply relative to Vss	-0.5 to +2.7	V
T_A	Operating Temperature (Ambient)	0 to +70	°C
T_{STG}	Storage Temperature (Plastic)	-55 to +150	°C
P_D	Power Dissipation	18	W
I_{OUT}	Short Circuit Output Current	50	mA

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Capacitance

Parameter	Symbol	Max.	Units	Notes
Input Capacitance: CK0, $\overline{CK0}$	C11	7	pF	1
Input Capacitance: A0-A12, BA0, BA1, \overline{WE} , \overline{RAS} , \overline{CAS} , $\overline{CKE0}$, $\overline{S0}$	C12	7	pF	1
Input Capacitance: \overline{RESET}	C13	7	pF	1
Input Capacitance: SA0-SA2, SCL	C14	9	pF	1
Input/Output Capacitance DQ0-63; DQS0-17, CB0-7	C101	10	pF	1,2
Input/Output Capacitance: SDA	C103	11	pF	

1. VDDQ = VDD = 2.5V ± 0.2V, f = 100 MHz, TA = 25 °C, VOUT (DC) = VDDQ/2, VOUT (Peak to Peak) = 0.2V.

2. DM inputs are grouped with I/O pins reflecting the fact that they are matched in loading to DQ and DQS to facilitate trace matching at the board level.

DC Electrical Characteristics and Operating Conditions

(TA = 0 °C ~ 70 °C ; VDDQ = 2.5V ± 0.2V; VDD = 2.5V ± 0.2V, See AC Characteristics)

Symbol	Parameter	Min	Max	Units	Notes
V _{DD}	Supply Voltage	2.3	2.7	V	1
V _{DDQ}	I/O Supply Voltage	2.3	2.7	V	1
V _{SS} , V _{SSQ}	Supply Voltage, I/O Supply Voltage	0	0	V	
V _{REF}	I/O Reference Voltage	0.49 x V _{DDQ}	0.51 x V _{DDQ}	V	1,2
V _{TT}	I/O Termination Voltage (System)	V _{REF} - 0.04	V _{REF} + 0.04	V	1,3
V _{IH} (DC)	Input High (Logic1) Voltage	V _{REF} + 0.15	V _{DDQ} + 0.3	V	1
V _{IL} (DC)	Input Low (Logic0) Voltage	-0.3	V _{REF} - 0.15	V	1
V _{IN} (DC)	Input Voltage Level, CK and \overline{CK} Inputs	-0.3	V _{DDQ} + 0.3	V	1
V _{ID} (DC)	Input Differential Voltage, CK and \overline{CK} Inputs	0.30	V _{DDQ} + 0.6	V	1,4
I _I	Input Leakage Current Any input 0V ≤ V _{IN} ≤ V _{DD} ; (All other pins not under test = 0V)	-5	5	uA	1
I _{OZ}	Output Leakage Current (DQs are disabled; 0V ≤ V _{out} ≤ V _{DDQ})	-5	5	uA	1
I _{OH}	Output High Current (V _{OUT} = V _{DDQ} - 0.373V, min V _{REF} , min V _{TT})	-16.8	-	mA	1
I _{OL}	Output Low Current (V _{OUT} = 0.373, max V _{REF} , max V _{TT})	16.8	-	mA	1

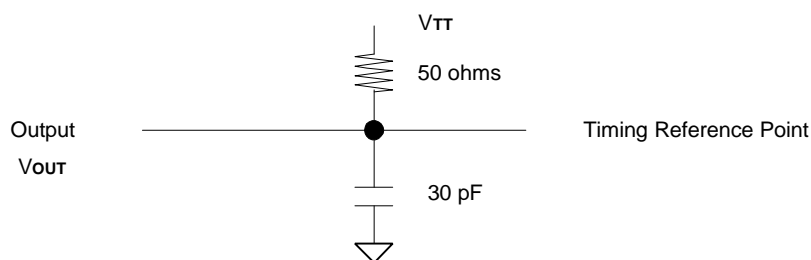
1. Inputs are not recognized as valid until V_{REF} stabilizes.
2. V_{REF} is expected to be equal to 0.5 V_{DDQ} of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed 2% of the DC value.
3. V_{TT} is not applied directly to the DIMM. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} , and must track variations in the DC level of V_{REF} .
4. V_{ID} is the magnitude of the difference between the input level on CK and the input level on \overline{CK} .

AC Characteristics

(Notes 1-5 apply to the following Tables; Electrical Characteristics and DC Operating Conditions, AC Operating Conditions, Operating, Standby, and Refresh Currents, and Electrical Characteristics and AC Timing.)

1. All voltages referenced to VSS .
2. Tests for AC timing, I_{DD} , and electrical, AC and DC characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load. Refer to the AC Output Load Circuit below.
4. AC timing and I_{DD} tests may use a V_{IL} to V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK, CK), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals is 1V/ns in the range between V_{IL(AC)} and V_{IH(AC)} unless otherwise specified.
5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e. the receiver effectively switches as a result of the signal crossing the AC input level, and remains in that state as long as the signal does not ring back above (below) the DC input LOW (HIGH) level.

AC Output Load Circuits



AC Operating Conditions

(TA = 0 °C ~ 70 °C ; VDDQ = 2.5V ± 0.2V; VDD = 2.5V ± 0.2V, See AC Characteristics)

Symbol	Parameter/Condition	Min	Max	Unit	Notes
V _{IH(AC)}	Input High (Logic 1) Voltage.	V _{REF} + 0.31	-	V	1, 2
V _{IL(AC)}	Input Low (Logic 0) Voltage.	-	V _{REF} - 0.31	V	1, 2
V _{ID(AC)}	Input Differential Voltage, CK and \overline{CK} Inputs	0.7	V _{DDQ} + 0.6	V	1, 2, 3
V _{IX(AC)}	Input Differential Pair Cross Point Voltage, CK and \overline{CK} Inputs	(0.5*V _{DDQ}) - 0.2	(0.5*V _{DDQ}) + 0.2	V	1, 2, 4

1. Input slew rate = 1V/ ns .
2. Inputs are not recognized as valid until V_{REF} stabilizes.
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on \overline{CK} .
4. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.



Operating, Standby, and Refresh Currents

(TA = 0 °C ~ 70 °C ; VDDQ = 2.5V ± 0.2V; VDD = 2.5V ± 0.2V, See AC Characteristics)

Symbol	Parameter/Condition	PC1600	PC2100	Unit	Notes	
I DD0	Operating Current : one bank; active / precharge; tRC = tRC (MIN) ; tCK = tCK (MIN) ; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	2180	2470	mA	1	
I DD1	Operating Current : one bank; active / read / precharge; Burst = 2; tRC = tRC (MIN) ; CL=2.5; tCK = tCK (MIN) ; IOUT = 0mA; address and control inputs changing once per clock cycle	2450	2990	mA	1	
I DD2P	Precharge Power-Down Standby Current : all banks idle; power-down mode; CKE ≤ VIL (MAX) ; tCK = tCK (MIN)	1100	1100	mA	1	
I DD2N	Idle Standby Current : CS ≥ VIH (MIN) ; all banks idle; CKE ≥ VIH(MIN) ; tCK = tCK (MIN) ; address and control inputs changing once per clock cycle	1370	1600	mA	1	
I DD3P	Active Power-Down Standby Current : one bank active; power-down mode; CKE ≤ VIL (MAX) ; tCK = tCK (MIN)	1110	1100	mA	1	
I DD3N	Active Standby Current : one bank; active / precharge; CS ≥ VIH (MIN) ; CKE ≥ VIH (MIN) ; tRC = tRAS (MAX) ; tCK = tCK (MIN) ; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	1730	2078	mA	1	
I DD4R	Operating Current : one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 2.5; tCK = tCK (MIN) ; IOUT = 0mA	3170	4026	mA	1	
I DD4W	Operating Current : one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL=2.5; tCK = tCK (MIN)	2900	2840	mA	1	
I DD5	Auto-Refresh Current :	t RC = t RFC (MIN)	3710	3940	mA	1,3
		t RC = 15.625 μs	1113	1113	mA	
I DD6	Self-Refresh Current : CKE ≤ 0.2V	61	61	mA	1	

1. I DD specifications are tested after the device is properly initialized.
 2. Enables on-chip refresh and address counters.
 3. Current at 7.8 μs is time averaged value of IDD5 at tRFC (MIN) and IDD2P over 15.625 μs.

AC Timing Specifications for DDR SDRAM Devices Used on Module

(TA = 0 °C ~ 70 °C ; VDDQ = 2.5V ± 0.2V; VDD = 2.5V ± 0.2V, See AC Characteristics) (Part 1 of 2)

Symbol	Parameter	-7K		-75B		-8B		Unit	Notes	
		Min.	Max.	Min.	Max.	Min.	Max.			
tAC	DQ output access time from CK/ $\overline{\text{CK}}$	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	1,2,3,4	
tDQSCK	DQS output access time from CK/ $\overline{\text{CK}}$	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	1,2,3,4	
tCH	CK high-level width	0.45	0.55	0.45	0.55	0.45	0.55	tCK	1,2,3,4	
tCL	CK low-level width	0.45	0.55	0.45	0.55	0.45	0.55	tCK	1,2,3,4	
tCK	Clock cycle time	CL=2.5	7	12	7.5	12	8	12	ns	1,2,3,4
tCK		CL=2	7.5	12	10	12	10	12	ns	1,2,3,4
tDH	DQ and DM input hold time	0.5		0.5		0.6		ns	1,2,3,4 ,15,16	
tDS	DQ and DM input setup time	0.5		0.5		0.6		ns	1,2,3,4 ,15,16	
tDIPW	DQ and DM input pulse width (each input)	1.75		1.75		2		ns	1,2,3,4	
tHZ	Data-out high-impedance time from CK/ $\overline{\text{CK}}$	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	1, 2, 3, 4, 5	
tLZ	Data-out low-impedance time from CK/ $\overline{\text{CK}}$	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	1, 2, 3, 4, 5	
tDQSQ	DQS-DQ skew (DQS & associated DQ signals)		0.5		0.5		0.6	ns	1,2,3,4	
tDQSQA	DQS-DQ skew (DQS & all DQ signals)		0.5		0.5		0.6	ns	1,2,3,4	
tHP	Minimum half clk period for any given cycle; defined by clk high(tCH) or clk low (tCL) time	tCH or tCL		tCH or tCL		tCH or tCL		tCK	1,2,3,4	
tQH	Data output hold time from DQS	tHP - 0.75ns		tHP - 0.75ns		tHP - 1.0ns		tCK	1,2,3,4	
tDQSS	Write command to 1st DQS latching transition	0.75	1.25	0.75	1.25	0.75	1.25	tCK	1,2,3,4	
tDQSL,H	DQS input low (high) pulse width (write cycle)	0.35		0.35		0.35		tCK	1,2,3,4	
tDSS	DQS falling edge to CK setup time (write cycle)	0.2		0.2		0.2		tCK	1,2,3,4	
tDSH	DQS falling edge hold time from CK (write cycle)	0.2		0.2		0.2		tCK	1,2,3,4	
tMRD	Mode register set command cycle time	14		15		16		ns	1,2,3,4	
tWPRES	Write preamble setup time	0		0		0		ns	1, 2, 3, 4, 7	
tWPST	Write postamble	0.40	0.60	0.40	0.60	0.40	0.60	tCK	1, 2, 3, 4, 6	
tWPRE	Write preamble	0.25		0.25		0.25		tCK	1,2,3,4	
tIH	Address and control input hold time (fast slew rate)	0.9		1.1		1.1		ns	2, 3, 4, 9, 11, 12	
tIS	Address and control input setup time (fast slew rate)	0.9		1.1		1.1		ns	2, 3, 4, 9, 11, 12	
tIH	Address and control input hold time (slow slew rate)	1.0		1.1		1.1		ns	2, 3, 4, 10, 11, 12, 14	

AC Timing Specifications for DDR SDRAM Devices Used on Module

(TA = 0 °C ~ 70 °C ; VDDQ = 2.5V ± 0.2V; VDD = 2.5V ± 0.2V, See AC Characteristics) (Part 2 of 2)

Symbol	Parameter	-7K		-75B		-8B		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
tIS	Address and control input setup time (slow slewrate)	1.0		1.0		1.1		ns	2, 3, 4, 10, 11, 12, 14
tIPW	Input pulse width	2.2		2.2			-	ns	2, 3, 4, 12
tRPRE	Read preamble	0.9	1.1	0.9	1.1	0.9	1.1	tCK	1,2,3,4
tRPST	Read postamble	0.40	0.60	0.40	0.60	0.40	0.60	tCK	1,2,3,4
tRAS	Active to Precharge command	45	120,000	45	120,000	50	120,000	ns	1,2,3,4
tRC	Active to Active/Auto-refresh command period	65		65		70		ns	1,2,3,4
tRFC	Auto-refresh to Active/Auto-refresh command period	75		75		80		ns	1,2,3,4
tRCD	Active to Read or Write delay	20		20		20		ns	1,2,3,4
tRAP	Active to Read Command with Autoprecharge	20		20		20		ns	1,2,3,4
tRP	Precharge command period	20		20		20		ns	1,2,3,4
tRRD	Active bank A to Active bank B command	15		15		15		ns	1,2,3,4
tWR	Write recovery time	15		15		15		ns	1,2,3,4
tDAL	Auto precharge write recovery + precharge time	(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		tCK	1, 2, 3, 4, 13
tWTR	Internal write to read command delay	1		1		1		tCK	1,2,3,4
tXSNR	Exit self-refresh to non-read command	75		75		80		ns	1,2,3,4
tXSRD	Exit self-refresh to read command	200		200		200		tCK	1,2,3,4
tREFI	Average Periodic Refresh Interval		15.625		15.625		15.625	µs	1, 2, 3, 4, 8

AC Timing Specification Notes

- Input slew rate = 1V/ns.
- The CK/ $\overline{\text{CK}}$ input reference level (for timing reference to CK/ $\overline{\text{CK}}$) is the point at which CK and $\overline{\text{CK}}$ cross: the input reference level for signals other than CK/ $\overline{\text{CK}}$, is VREF.
- Inputs are not recognized as valid until VREF stabilizes.
- The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (Note 3) is VTT.
- tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
- The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
- The specific requirement is that DQS be valid (high, low, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from high to low at this time, depending on tDQSS.
- A maximum of eight Auto refresh commands can be posted to any given DDR SDRAM device.
- For command/address input slew rate ≥ 1.0 V/ns. Slew rate is measured between VOH (AC) and VOL (AC).
- For command/address input slew rate ≥ 0.5 V/ns and < 1.0 V/ns. Slew rate is measured between VOH (AC) and VOL (AC).
- CK/ $\overline{\text{CK}}$ slew rates are ≥ 1.0 V/ns.
- These parameters guarantee device timing, but they are not necessarily tested on each device, and they may be guaranteed by design or tester characterization.
- For each of the terms in parentheses, if not already an integer, round to the next highest integer. tCK is equal to the actual system clock cycle time. For example, for PC2100 at CL= 2.5, tDAL = (15ns/7.5ns) +(20ns/7.0ns) = 2 + 3 = 5.
- An input setup and hold time derating table is used to increase tIS and tIH in the case where the input slew rate is below 0.5 V/ns.

Input Slew Rate	Delta (tIS)	Delta (tIH)	Unit	Note
0.5 V/ns	0	0	ps	1,2
0.4 V/ns	+50	0	ps	1,2
0.3 V/ns	+100	0	ps	1,2

1. Input slew rate is based on the lesser of the slew rates determined by either V IH (AC) to V IL (AC) or V IH (DC) to V IL (DC) , similarly for rising transitions.
2. These derating parameters may be guaranteed by design or tester characterization and are not necessarily tested on each device.

- An input setup and hold time derating table is used to increase tDS and tDH in the case where the I/O slew rate is below 0.5 V/ns.

Input Slew Rate	Delta (tDS)	Delta (tDH)	Unit	Note
0.5 V/ns	0	0	ps	1,2
0.4 V/ns	+75	+75	ps	1,2
0.3 V/ns	+150	+150	ps	1,2

1. I/O slew rate is based on the lesser of the slew rates determined by either V IH (AC) to V IL (AC) or V IH (DC) to V IL (DC) , similarly for rising transitions.
2. These derating parameters may be guaranteed by design or tester characterization and are not necessarily tested on each device.

- An I/O Delta Rise, Fall Derating table is used to increase tDS and tDH in the case where DQ, DM, and DQS slew rates differ.

Delta Rise and Fall Rate	Delta (tDS)	Delta (tDH)	Unit	Note
0.0 ns/V	0	0	ps	1,2,3,4
0.25 ns/V	+50	+50	ps	1,2,3,4
0.5 ns/V	+100	+100	ps	1,2,3,4

1. Input slew rate is based on the lesser of the slew rates determined by either V IH (AC) to V IL (AC) or V IH (DC) to V IL (DC) , similarly for rising transitions.
2. Input slew rate is based on the larger of AC to AC delta rise, fall rate and DC to DC delta rise, fall rate.
3. The delta rise, fall rate is calculated as: [1/(slew rate 1)] - [1/(slew rate 2)]
For example: slew rate 1 = 0.5 V/ns; slew rate 2 = 0.4 V/ns. Delta rise, fall = (1/0.5) - (1/0.4) [ns/V] = -0.5 ns/V
Using the table above, this would result in an increase in tDS and tDH of 100 ps.
4. These derating parameters may be guaranteed by design or tester characterization and are not necessarily tested on each device.

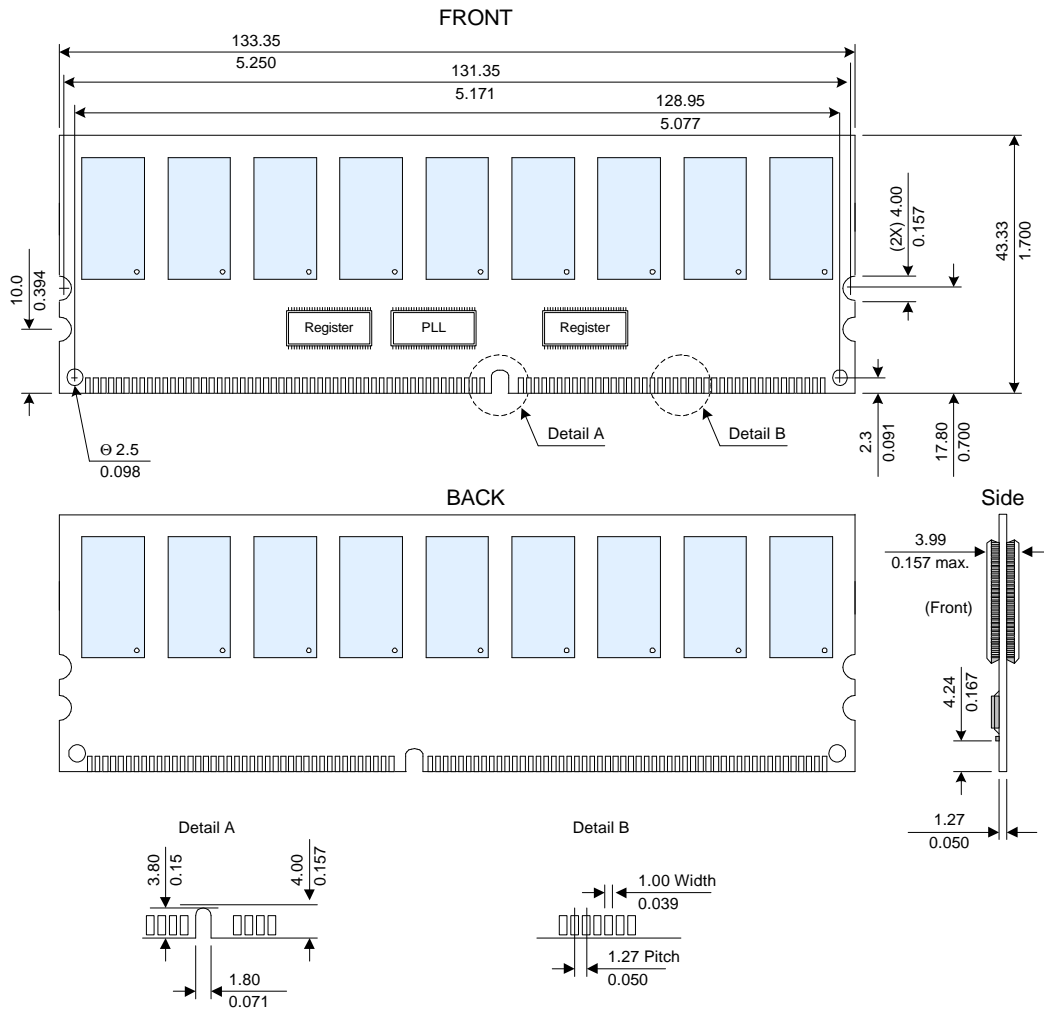
NT256D72S4PA0GR

256MB : 32M x 72

Registered DDR SDRAM DIMM



Package Dimensions



Note : All dimensions are typical unless otherwise stated.

Unit : Millimeters(Inches)