AN6574, AN6574S

Low Noise, High Slew Rate Operational Amplifiers

Outline

The AN6574 and the AN6574S are low noise, high slew rate quadruple operational amplifiers with phase compensation circuits built-in. They are wideband with high stability and suited for application to various electronic circuits such as active filters and audio preamplifiers.

■ Features

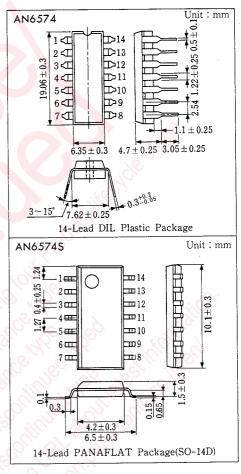
• Phase compensation circuit

 \bullet High gain : $G_v = 110dB$ typ.

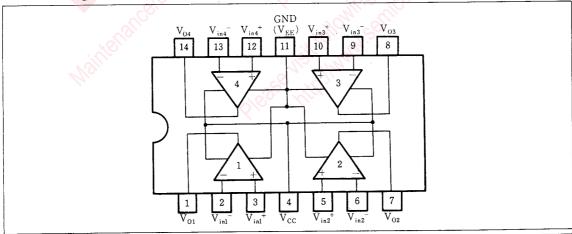
 \bullet Low noise : $V_{nl} = 0.9 \mu V_{rms} typ$.

• High slew rate : SR=6V/μs typ.

• High stability.



■ Block Diagram



■ Pin

Pin No.	Pin Name	Pin No.	Pin Name	
1	Ch. 1 Output	8	Ch. 3 Output	
2	Ch. 1 Invert Input	9	Ch. 3 Invert Input	
3	Ch. 1 Non Invert Input	10	Ch. 3 Non Invert Input	
4	V _{cc}	11	$\overline{\text{GND}}(V_{\text{EE}})$	
5	Ch. 2 Non Invert Input	12	Ch. 4 Non Invert Input	
6	Ch. 2 Invert Input	13	Ch. 4 Invert Input	
7	Ch. 2 Output	14	Ch. 4 Output	

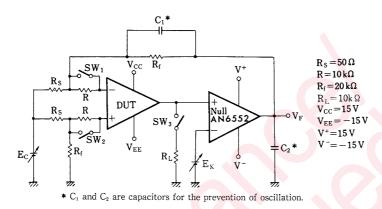
■ Absolute Maximum Ratings (Ta=25°C)

	Item	Symbol	Rating	Unit
	Supply Voltage	V _{cc}	±18	V
Voltage	Differential Input Voltage	V _{ID}	±30	V
	Common-Mode Input Voltage	V _{ICM}	±15	V
Power Dissipation	AN6574	D	570	
Tower Bissipation	AN6574S	P_{D}	380	mW
Operating Ambie	nt Temperature	Topr	$-20 \sim +75$	°C
Storage Temperature	AN6574	T	$-55 \sim +150$	80
z z z z z z z z z z z z z z z z z z z	AN6574S	$T_{ m stg}$	-55~+125	$^{\circ}$

■ Electrical Characteristics ($V_{cc} = 15V$, $V_{EE} = -15V$, Ta = 25°C)

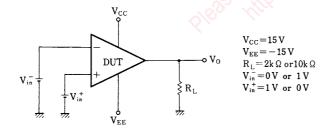
Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Input Offset Voltage	V _{I(offset)}	1	$R_s \leq 10 k\Omega$		0.3	5	mV
Input Offset Current	Iio	1	1,10° ill' 00° 100	0.	5	200	nA
Input Bias Current	$I_{\mathtt{Bias}}$	1	with the shift	Q . 3	300	1000	nA
Voltage Gain	Gv	1	$R_L \ge 2k\Omega$, $V_0 \pm 10V$	90	110	2000	dB
Maximum Output Voltage	V _{O(max.)}	2	$R_L \ge 10 k\Omega$	±12	±13.5		V
Maximum Output Voltage	V _{O(max.)}	2	$R_{L} \ge 2k\Omega$	±10	±13.4		V
Common-Mode Input Voltage Width	V _{CM}	3	60 69, 157	±12	±14		V
Common-Mode Rejection Ratio	CMR	1	19/1/2/2010	80	100		dB
Supply Voltage Rejection Ratio	SVR	1	9); 6); 6	- 00	10	100	$\mu V/V$
Power Consumption	P _c	4	$R_{I} = \infty$		210	360	mW
Slew Rate	SR	5	$R_L \ge 2k\Omega$	-	6	500	V/μs
Zero-Cross Frequency	f _(T)	6	$A_v = 1$		7		MHz
Input Referred Noise Voltage V _{ni} 7		$R_s=1k\Omega$, DIN/AUDIO		0.9		$\mu V_{\rm rms}$	

Test Circuit 1 (V_{I(o'ffset)}, I_{IO}, I_{Bias}, G_V, CMR, SVR)



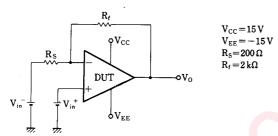
Item	Measurement Conditions				
Input Offset Voltage	V_{F1} is measured with the SW ₁ , SW ₂ and SW ₃ set to OFF and $E_c = E_k = 0V$. Can be given by $V_{\text{1(offset)}} = \frac{V_{\text{F1}}}{400}(V)$				
Input Offset Current	V_{F2} is measured with the SW ₁ and SW ₂ set to ON, and the SW ₃ set to OFF and $E_c = E_K = 0V$. Can be given by $I_{10} = \frac{ V_{F2} - V_{F1} }{4 \times 10^6}$ (A)				
Input Bias Current	V_{F3} is measured with the SW_1 set to ON , the SW_2 set to OFF , SW_3 set to OFF and $E_C = E_K = 0V$. V_{F4} is measured with the SW_1 and SW_2 reversed. Can be given by $I_{B1aS} = \frac{ V_{F3} - V_{F4} }{8 \times 10^5}$ (A)				
Voltage Gain	V_{FS} is measured with the SW ₁ ' SW ₂ and SW ₃ set to ON, $E_c = 0V$ and $E_K = 10V$. V_{FS} ' is measured with $E_K = -10V$. Can be given by $G_V = 20\log\left(\frac{8000}{\mid V_{FS} - V_{FS} \mid \mid}\right)$				
Common-Mode Rejection Ratio	V_{Fe} is measured with the SW ₁ and SW ₂ set to ON, the SW ₃ set to OFF, E_{K} =0V and E_{C} =5V. V_{Fe} is measured with E_{C} =-5V. Can be given by CMR=20log $\left(\frac{4000}{\mid V_{\text{Fe}} - V_{\text{F}'e} \mid}\right)$				
Supply Voltage Rejection Ratio I	V_{F7} is measured with the SW_1 and SW_2 set to ON, the SW_3 set to OFF, $E_{\kappa}\!=\!E_c\!=\!0V$ and $V_{cc}\!=\!10V$. Can be given by $SVR(+)=\frac{\mid V_{F7}\!-\!V_{F2}\mid}{2\!\times\!10^3}$				
Supply Voltage Rejection Ratio II	V_{F8} is measured with the SW ₁ and SW ₂ set to ON, the SW ₃ set to OFF, $E_K = E_C = 0V$ and $V_{EE} = -10V$. Can be given by $SVR(-) = \frac{V_{F8} - V_{F2}}{2 \times 10^3}$				

Test Circuit 2 (V_{O(max.)})



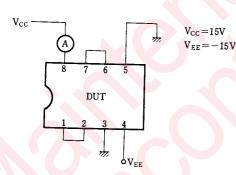


Test Circuit 3 (V_{CM})

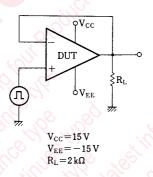


Note) Apply a voltage of $\mid V_{in}^+ \mid > 12V$ and check $V_o = V_{in}^+ + \frac{R_f}{R_s} (V_{in}^+ - V_{in}^-)$

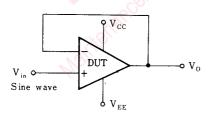
Test Circuit 4 (Pc)



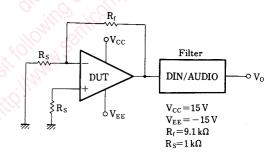
Test Circuit 5 (SR)



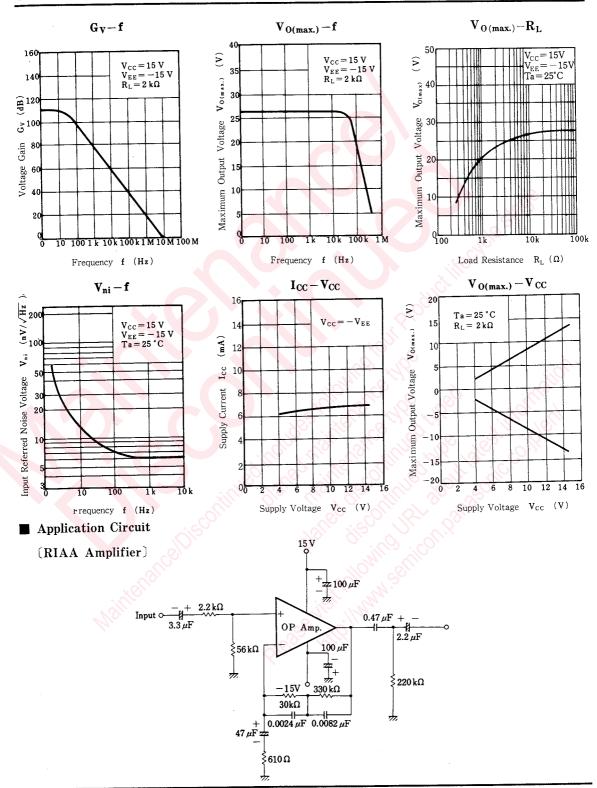
Test Circuit 6 (f_(T))



Test Circuit 7 (Vni)



Note) An input referred noise voltage $V_{ni}\!=\!\!\frac{V_0}{(1\!+\!R_f/R_s)}$ is given.



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