AN440
Application note

QII and QIII TRIAC triggering with positive power supply

Introduction

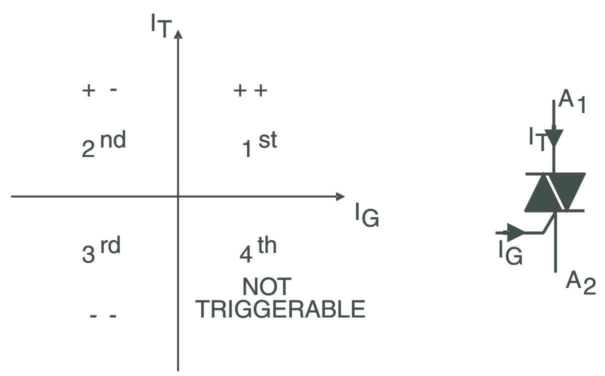
New TRIACs with high commutation and dv/dt performances are now available on the market.

Generally these TRIACs can be triggered only in the first three quadrants (case of Snubberless™, logic level and Snubberless high temperature TRIACs) as shown in *Figure 1*.

This paper describes a trigger circuit supplying a negative gate current for quadrants II and III implemented in a system using a positive power supply.

Without a new design, just by adding a capacitor and a diode, new series TRIACs can replace conventional TRIACs.

Figure 1. The quadrants of Snubberless, logic-level, and Snubberless high temperature TRIACs

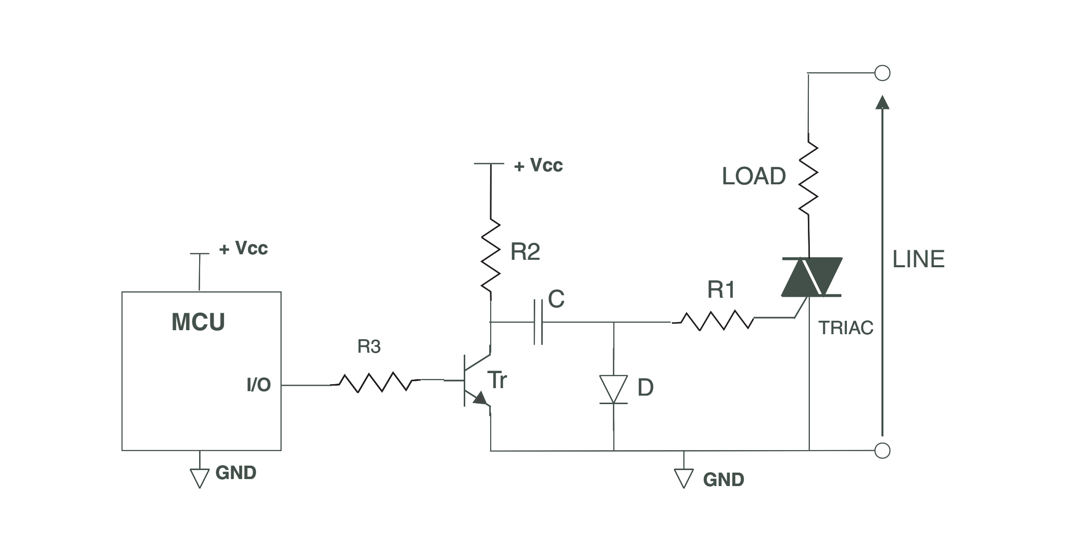


TM: Snubberless is a trademark of STMicroelectronics

1 Principle of proposed gate circuit

To drive the TRIAC in the 2nd and 3rd quadrants, a discharge capacitor is used as shown in *Figure 2*.

Figure 2. Basic diagram of the triggering circuit



When the transistor Tr is switched off, capacitor C is charged through resistance R2 and diode D. The diode is used to avoid a capacitor charging current through the TRIAC gate. A Schottky diode could be used to keep the voltage drop level below the gate non trigger voltage (V_{GD}). When the TRIAC is triggered, Tr transistor is switched on, C is discharged through R1 and Tr and a negative current flows through the TRIAC gate.

We have to consider different parameters to define all the components:

- The TRIAC gate triggering current (I_{GT}).
- The time duration of the gate current pulse.
- The TRIAC latching current (I_L) especially for low rms current loads.

2 Gate current pulse width setting

The TRIAC latching current (I_L) is the minimum value of the main current which allows the component to remain in the conducting state after the gate current I_G has been removed.

That is to say the gate current has to be higher than I_{GT} until the main current reaches the latching current.

Example: for most of CW Snubberless TRIACs (refer to datasheet for further information):

Q1 – Q3: I_L max = 50 mA

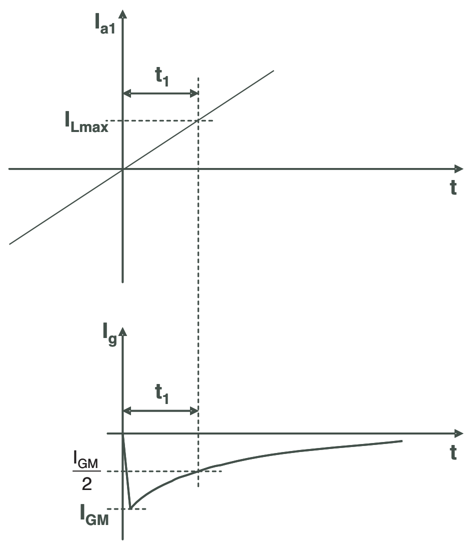
Q2: I_L max = 60 mA

Example: for most BW Snubberless TRIACs:

Q1 – Q3: I_L max = 70 mA

Q2: I_L max = 80 mA

Figure 3. Gate control principle



t_1 calculation

The TRIAC gate has to be supplied to reach an anode current higher than the latching current. Furthermore, a minimum gate current pulse width of 20 µs has to be ensured. The minimum t_1 level is then given by the following equation:

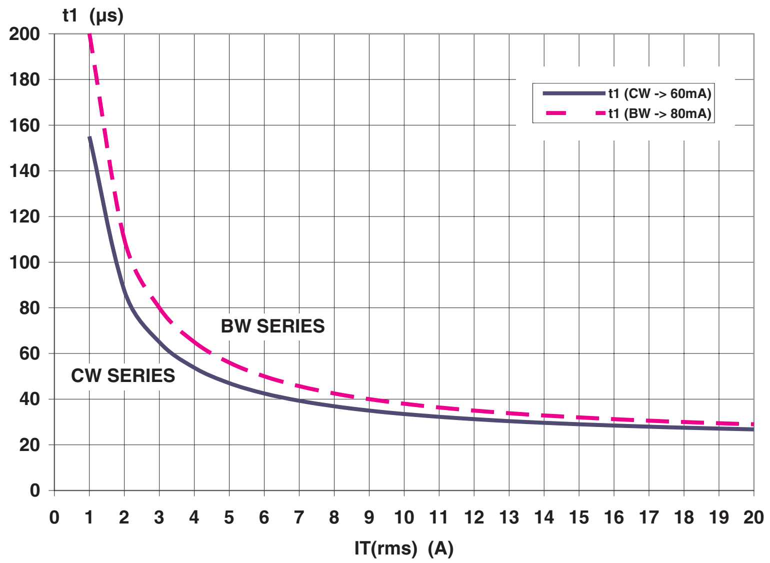
$$t_1 \geq \frac{1}{\omega} \operatorname{asin}\left(\frac{I_L MAX}{I_{RMS} \cdot \sqrt{2}}\right) + 20\ \mu s$$

Where $\omega = 2.\pi.f$ and f is mains frequency.

I_{RMS}: minimum rms current of the load (depending on line and load variations).

Figure 4 shows the minimum time versus I_{RMS} load current for a 50Hz application.

Figure 4. t_1 time versus I_{RMS} for different load currents (worst case: ILQ2)



Note: Curve given for $V_{CE} = 1\ V$ and $V_{GK} = 1.3\ V$

I_{GT} is the maximum gate trigger current specified in the data sheet. To ensure a good safety margin and a good triggering we chose $I_{GM} = 2.I_{GT}$.

The gate resistor can be defined by the following equation:

$$R_1 = \frac{V_{CC} - V_{GK} - V_{CE}}{I_{GM}}$$

with typically $V_{CE} = 1$ V and $V_{GK} = 1.3$ V at $I_{GM} = 2.I_{GT}$

Capacitor C is then given by the following equation (where t_1 is given by *Figure 4*):

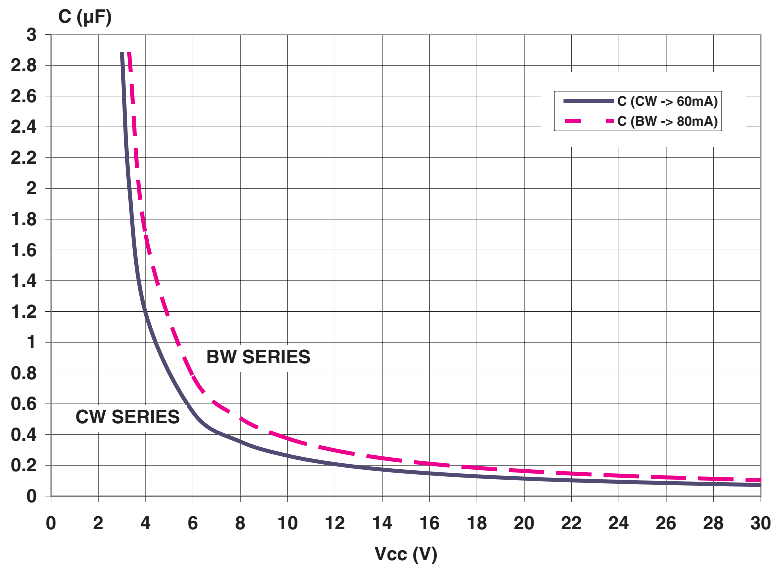
$$C \geq \frac{t_1}{R_1 \cdot \ln(2)}$$

Figure 5 gives the minimum capacitance versus supply voltage for different TRIACs series.

To ensure that capacitor C will be charged for the nest half cycle, R_2 could be chosen with this equation (charging time constant < 1 ms):

$$R_2 < \frac{0.001}{C}$$

Figure 5. Capacitance value versus supply voltage for different sensitivities

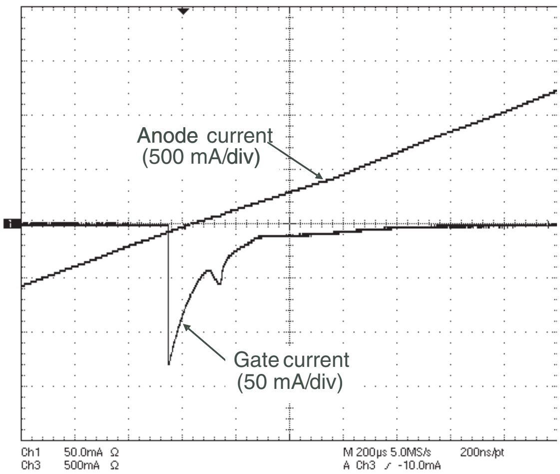


3 Experimental results

Figure 6 gives a typical oscillogram within the following conditions:

- TRIAC = BTA08-600CW
- I_{RMS} = 2.12 A (load power: 500 W)
- Line voltage: 230 V rms, 50 Hz
- V_{CC} = 5 V
- R_1 = 36 Ω
- R_2 = 300 Ω
- C = 3.3 μF

Figure 6. Triggering at zero current



The component values are given in the following table for different application cases.

Table 1. Component values for 3 different cases. TRIAC: BTA08-600CW (I_{GT} = 35 mA)

	I_{RMS} = 2 A V_{cc} = 5 V	I_{RMS} = 5 A V_{cc} = 5 V	I_{RMS} = 5 A V_{cc} = 10 V
t_{1MIN} (μs)	87.5	47	47
R_{1MAX} (Ω)	39	39	110
C_{MIN} (μF)	3.3	1.76	0.62
R_{2MAX} (Ω)	306	569	1622

4 Conclusion

In the case of controllers supplied by positive voltage this solution allows the replacement of conventional TRIACs used in the 1st and 4th quadrants by Snubberless or LOGIC LEVEL TRIACs which operate only in the first three quadrants. This solution only requires the addition of a capacitor and a diode to control each TRIAC.

With inductive loads (motor, transformer, etc...) a pulse train can be used because of the phase lag between current and voltage.

In the case of logic or transistor failure, the capacitor C operates as an open circuit for dc current and avoids all triggering. This factor acts as a safety feature.

But this trigger circuit can not be effectively used to drive small loads (like valves, fan etc...) because the latching current value is quite high compared to the load current. In this case a dc gate current is required.

Then the V_{CC} point of the power supply should be connected to A_1 to sink the current directly from the gate with the control circuit. There is then no need of a supplementary capacitor and diode. This solution is then easier and cheaper.

5 Revision history

Table 2. Document revision history

Date	Revision	Changes
May-1992	1	Initial release.
23-Apr-2004	2	Style sheet update. No Content change.
10-Mar-2008	3	Reformatted to current standards. Full technical review