

# P3P76Z11D, P3P76Z11DH

## Low Voltage, Timing-Safe™ Peak EMI reduction IC

### Functional Description

P3P76Z11D/DH is a versatile low voltage peak EMI reduction IC based on Timing-Safe technology. P3P76Z11D/DH accepts one input from an external reference, and locks on to it delivering a 1x Timing-Safe output clock. P3P76Z11D/DH has a Frequency Selection (FS) control that facilitates selecting one of the two frequency ranges within the operating frequency range. Refer *frequency Selection table*. The device has an SSEXTR pin to select different deviations depending upon the value of an external resistor connected at this pin to GND. P3P76Z11D/DH has a DLY\_CTRL for adjusting the Input-Output clock delay, depending upon the value of the capacitor connected at this pin to GND. PD# / OE provide the Power Down option. Outputs will be tri-stated when power down is active.

P3P76Z11D is a Low drive part and P3P76Z11DH is a High drive part. Refer to *DC/AC Electrical characteristic table*.

P3P76Z11D/DH operates over a supply voltage range of  $1.8\text{ V} \pm 0.2\text{ V}$ , and is available in an 8 Pin WDFN (2 mm x 2 mm) Package.

### General Features

- 1x , LVC MOS Timing-Safe Peak EMI Reduction
- Input Clock Frequency:  
15 MHz – 75 MHz
- Output Clock Frequency( Timing-Safe):  
15 MHz – 75 MHz
- Analog Frequency Deviation Selection
- Analog Input-Output Delay Control
- Power Down option for Power Save
- Low and High drive parts
- Supply Voltage:  $1.8\text{ V} \pm 0.2\text{ V}$
- 8 pin WDFN(2 mm x 2 mm) package
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

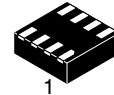
### Application

- P3P76Z11D/DH is targeted for use in consumer electronic applications like mobile phones, Camera modules, MFP and DPF.



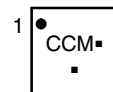
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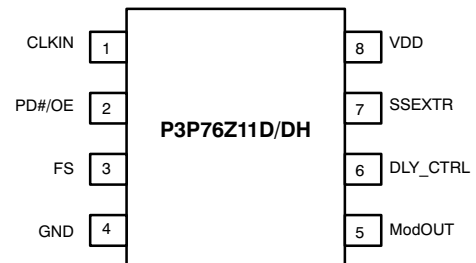
WDFN8  
CASE 511AQ

### MARKING DIAGRAMS



CC = Specific Device Code  
M = Date Code  
■ = Pb-Free Device

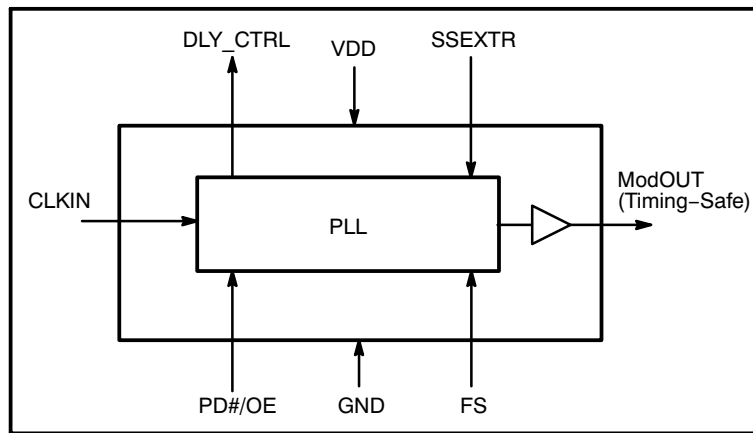
### PIN CONFIGURATION



### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

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**Figure 1. Block Diagram**

**Table 1. PIN DESCRIPTION**

Pin#	Pin Name	Type	Description
1	I	CLKIN	External reference Clock input.
2	I	PD# / OE	Power Down. Pull LOW to enable Power Down. Outputs will be tri-stated when power down is enabled. Pull HIGH to disable power down and enable output. Has NO default state.
3	I	FS	Frequency Select (see <i>Frequency Selection table</i> for details). Has NO default state.
4	P	GND	Ground
5	O	ModOUT	Buffered modulated Timing-Safe clock output
6	O	DLY_CTRL	External Input-Output Delay control
7	I	SSEXTR	Analog Spread Selection through external resistor to GND.
8	P	VDD	Supply Voltage

**Table 2. FREQUENCY SELECTION TABLE**

FS	Frequency (MHz)
0	15 – 30
1	30 – 75

**Table 3. OPERATING CONDITIONS**

Symbol	Description	Min	Max	Unit
V <sub>DD</sub>	Supply Voltage	1.6	2	V
T <sub>A</sub>	Operating Temperature	0	+70	°C
C <sub>L</sub>	Load Capacitance		15	pF
C <sub>IN</sub>	Input Capacitance		7	pF

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**Table 4. ABSOLUTE MAXIMUM RATING**

Parameter	Min	Max	Unit
Supply Voltage to Ground Potential	-0.3	+2.7	V
DC Input Voltage(CLKIN)	-0.3	+2.7	V
DC Input Voltage (Except CLKIN)	-0.3	VDD + 0.3	V
Storage Temperature	-65	+150	°C
Max. Soldering Temperature (10 sec)		260	°C
Junction Temperature		150	°C
Static Discharge Voltage (As per JEDEC STD22- A114-B)		2000	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**Table 5. DC ELECTRICAL CHARACTERISTICS FOR  $V_{DD} = 1.8\text{ V} \pm 0.2\text{ V}$**

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{DD}$	Supply Voltage		1.6	1.8	2	V
$V_{IH}$	Input HIGH Voltage		0.65 * $V_{DD}$			V
$V_{IL}$	Input LOW Voltage				0.35 * $V_{DD}$	V
$I_{IH}$	Input HIGH Current	$V_{IN} = V_{DD}$			5	$\mu\text{A}$
$I_{IL}$	Input LOW Current	$V_{IN} = 0\text{ V}$			5	$\mu\text{A}$
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -8\text{ mA}$ (P3P76Z11D)	0.75 * $V_{DD}$			V
		$I_{OH} = -16\text{ mA}$ (P3P76Z11DH)				
$V_{OL}$	Output LOW Voltage	$I_{OL} = 8\text{ mA}$ (P3P76Z11D)			0.25 * $V_{DD}$	V
		$I_{OL} = 16\text{ mA}$ (P3P76Z11DH)				
$I_{CC}$	Static Supply Current	PD# pin pulled to GND			10	$\mu\text{A}$
$I_{DD}$	Dynamic Supply Current	Unloaded Output	FS = 0, @ 15 MHz		3	mA
			FS = 0, @ 30 MHz		5	
			FS = 1, @ 30 MHz		4	
			FS = 1, @ 75 MHz		10	
$Z_o$	Output Impedance	P3P76Z11D		23		$\Omega$
		P3P76Z11DH		17		

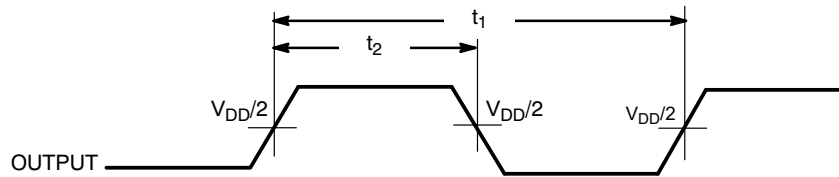
# P3P76Z11D, P3P76Z11DH

**Table 6. AC ELECTRICAL CHARACTERISTICS FOR  $V_{DD} = 1.8\text{ V} \pm 0.2\text{ V}$**

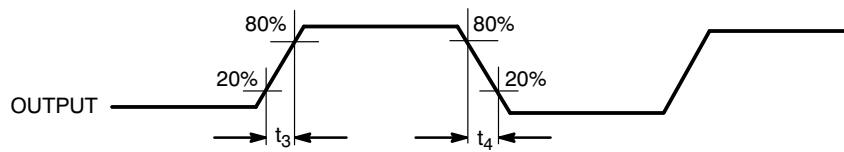
Parameter	Test Conditions	Min	Typ	Max	Unit	
Input Frequency	FS = 0	15		30	MHz	
	FS = 1	30		75		
ModOUT	FS = 0	15		30		
	FS = 1	30		75		
Duty Cycle (Notes 1 and 2)	Measured at $V_{DD} / 2$	45	(49–51)	55	%	
Rise Time (Notes 1 and 2)	Measured between 20% to 80%	P3P76Z11D		1.3	2.1	ns
		P3P76Z11DH		1	1.7	
Fall Time (Notes 1 and 2)	Measured between 80% to 20%	P3P76Z11D		1.3	2.1	ns
		P3P76Z11DH		1	1.7	
Cycle-to-Cycle Jitter (Note 2)	Unloaded output with SSEXTR = OPEN	FS = 0	15 MHz		$\pm 150$	ps
			30 MHz		$\pm 100$	
		FS = 1	30 MHz		$\pm 150$	
			75 MHz		$\pm 100$	
Input-Output propagation Delay (Note 2)	SSEXTR = OPEN, No load on DLY_CTRL and ModOUT		1.1		ns	
Load line	Change in Input-Output delay (with capacitive load $\leq 15\text{ pF}$ ), SSEXTR = OPEN	on DLY_CTRL		-35	ps/pF	
		on ModOUT		35		
PLL Lock Time (Note 2)	Stable power supply, valid clock presented on CLKIN pin, PD# toggled from Low to High			1	ms	

1. All parameters are specified with 15 pF loaded output.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production.

## SWITCHING WAVEFORMS

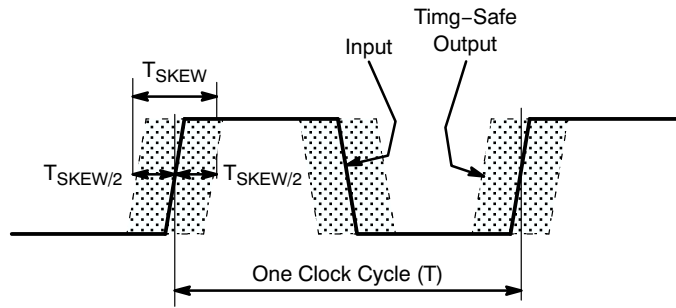


**Figure 2. Duty Cycle Timing**



**Figure 3. Output Rise/Fall Time**

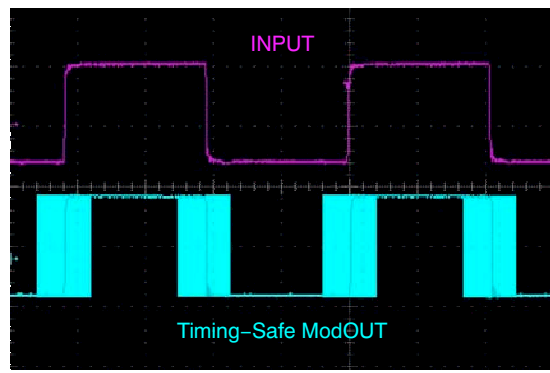
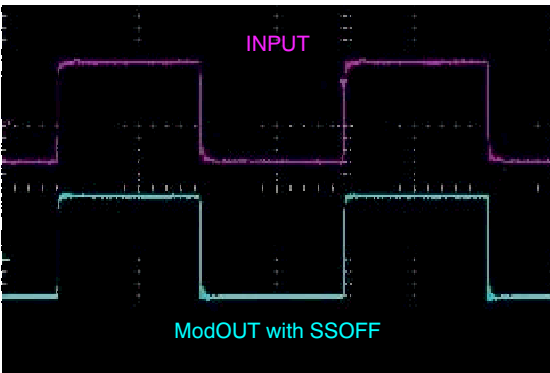
# P3P76Z11D, P3P76Z11DH



$T_{SKEW}$  represents input-output skew when spread spectrum is ON

For example,  $T_{SKEW} / 2 = 0.20 * T$  for an Input clock of 24 MHz, translates in to  $(1/24 \text{ MHz}) * 0.20 = 8.33 \text{ ns}$

**Figure 4. Input-Output Skew**



**Figure 5. Typical Example of Timing-Safe Waveform**

DEVIATION CHARTS

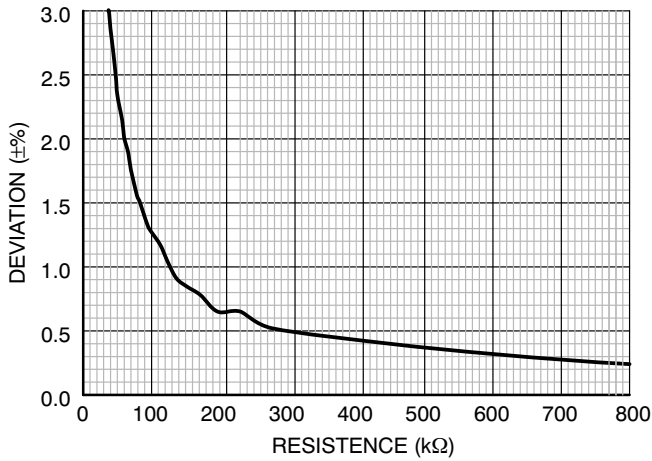


Figure 6. Deviation vs. SSEXT<sub>R</sub> @ FS = 0, 15 MHz

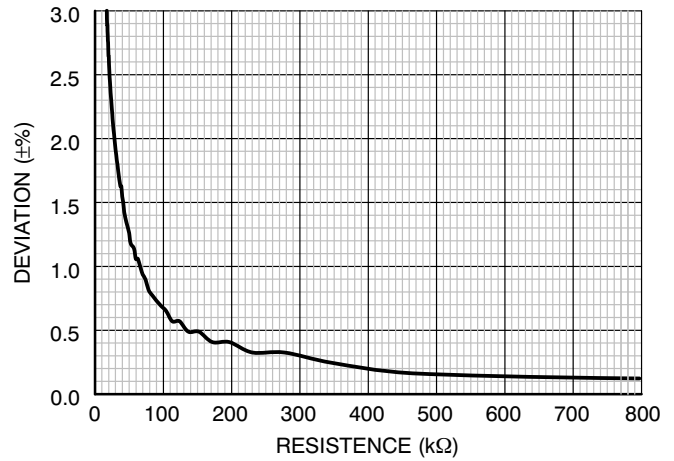


Figure 7. Deviation vs. SSEXT<sub>R</sub> @ FS = 0, 24 MHz

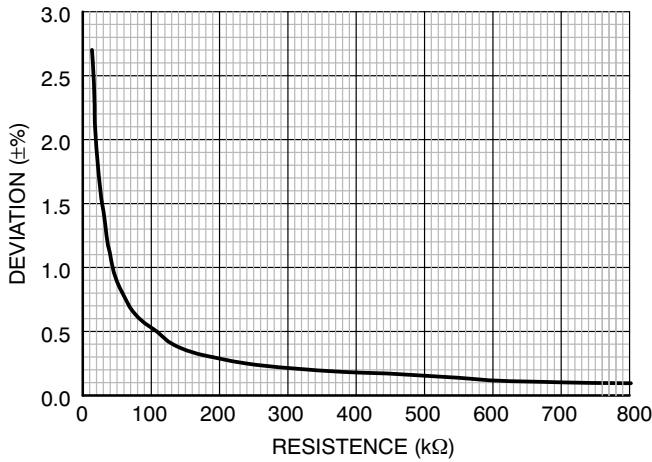


Figure 8. Deviation vs. SSEXT<sub>R</sub> @ FS = 0, 30 MHz

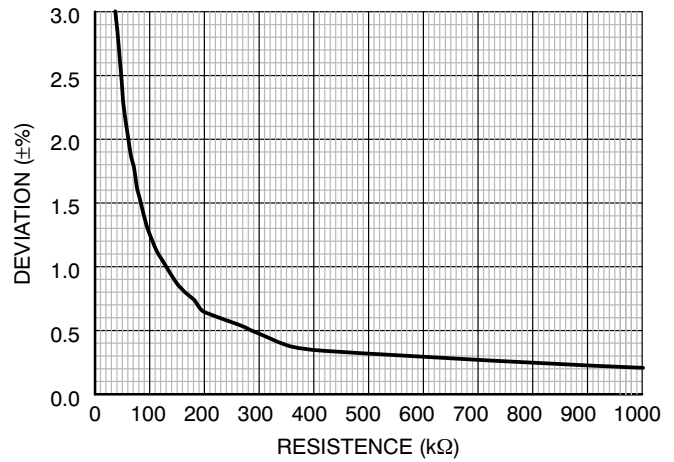


Figure 9. Deviation vs. SSEXT<sub>R</sub> @ FS = 1, 30 MHz

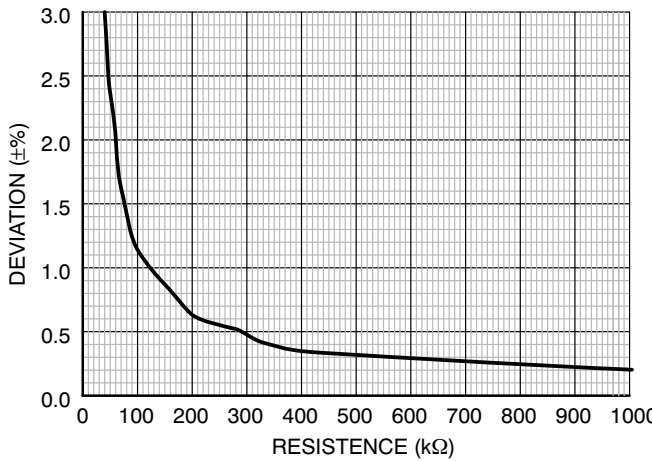


Figure 10. Deviation vs. SSEXT<sub>R</sub> @ FS = 1, 40 MHz

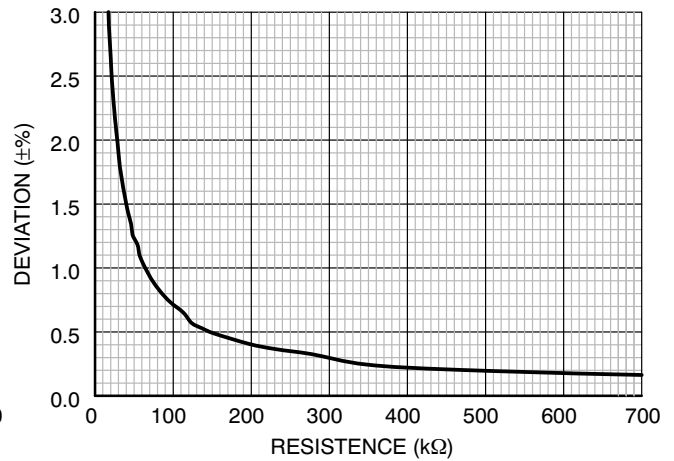


Figure 11. Deviation vs. SSEXT<sub>R</sub> @ FS = 1, 48 MHz

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## DEVIATION CHARTS

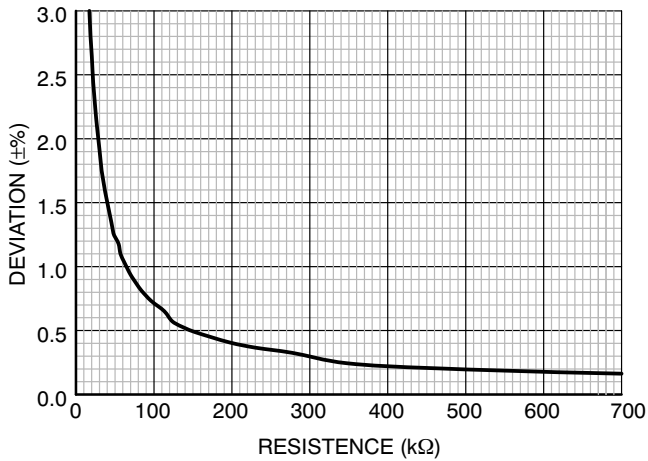


Figure 12. Deviation vs. SSEXTR @ FS = 1, 54 MHz

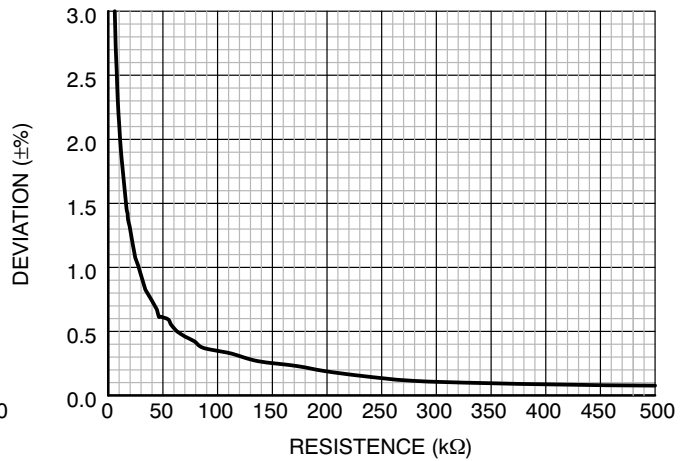


Figure 13. Deviation vs. SSEXTR @ FS = 1, 72 MHz

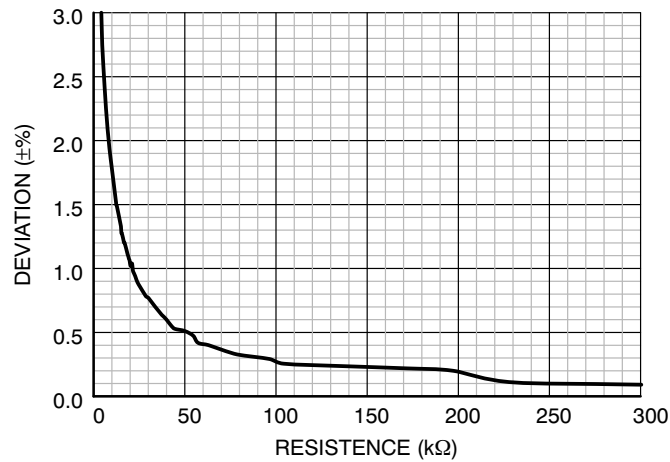
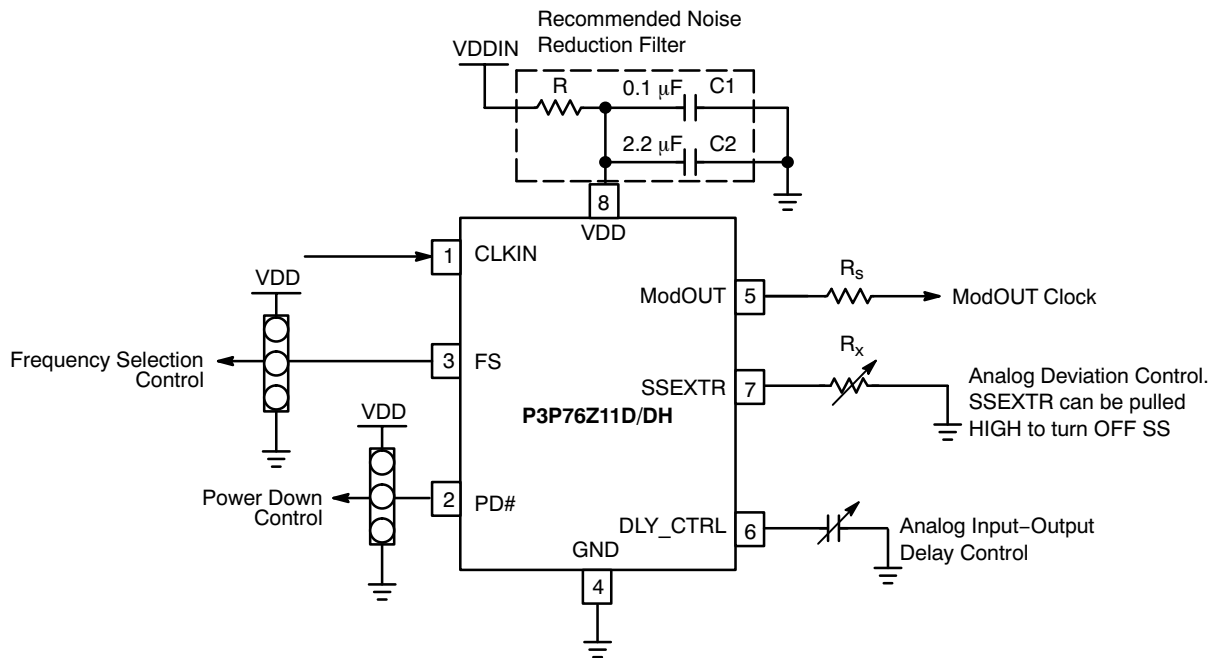


Figure 14. Deviation vs. SSEXTR @ FS = 1, 74.25 MHz

NOTE: Device-to-Device variation of Deviation and I/O delay is ±15%.

## P3P76Z11D, P3P76Z11DH



NOTE: Refer Pin Description table for Functionality details.

Figure 15.

### PCB Layout Recommendation

For optimum device performance, following guidelines are recommended.

- Dedicated VDD and GND planes.
- The device must be isolated from system power supply noise. A 0.1 μF and a 2.2 μF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitor and VDD pin. The PCB trace to VDD pin and the ground via should be kept as short as possible. All the VDD pins should have decoupling capacitors.
- In an optimum layout all components are on the same side of the board, minimizing vias through other signal layers.

A typical layout is shown in the figure

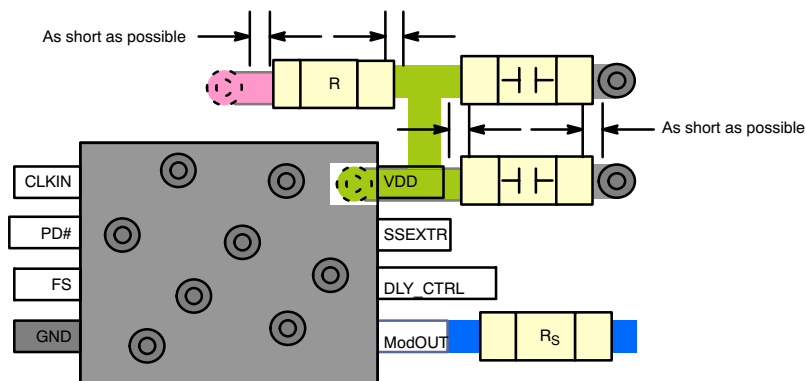


Figure 16.



## P3P76Z11D, P3P76Z11DH

### ORDERING INFORMATION

Part Number	Top Marking	Temperature	Package Type	Shipping†
P3P76Z11DHG-08CR	FE	0°C to +70°C	8-pin (2 mm x 2 mm) WDFN (Pb-Free)	Tape & Reel

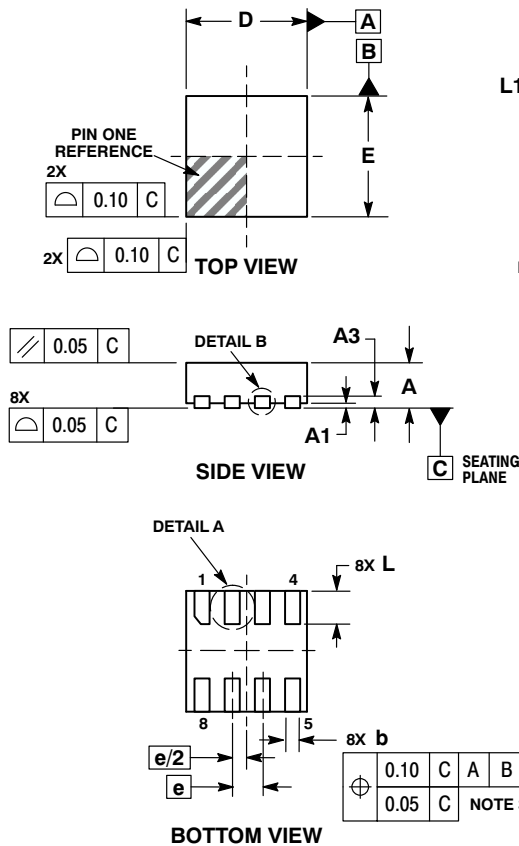
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*A "microdot" placed at the end of last row of marking or just below the last row toward the center of package indicates Pb-Free.

# P3P76Z11D, P3P76Z11DH

## PACKAGE DIMENSIONS

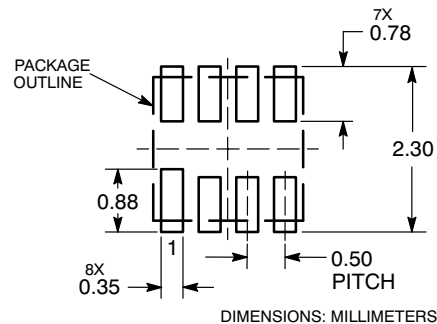
WDFN8 2x2, 0.5P  
CASE 511AQ-01  
ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL.

DIM	MILLIMETERS	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20	REF
b	0.20	0.30
D	2.00	BSC
E	2.00	BSC
e	0.50	BSC
L	0.50	0.60
L1	---	0.15

### RECOMMENDED SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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