LS4117
N-CHANNEL JFET

Linear Systems replaces discontinued Siliconix 2N4117

The LS4117 is an Ultra-High Input Impedance N-Channel JFET

The LS4117 provides ultra-high input impedance. The device is specified with a 10-pA limit and is ideal for use as a high-impedance sensitive front-end amplifier.

LS4117 Benefits:

- Insignificant Signal Loss/Error Voltage with High-Impedance Source
- Low Power Consumption (Battery)
- Maximum Signal Output, Low Noise
- High Sensitivity to Low-Level Signals

LS4117 Applications:

- High-Impedance Transducer
- Smoke Detector Input
- Infrared Detector Amplifier
- Precision Test Equipment

FEATURES	
DIRECT REPLACEMENT FOR SILICONIX 2N4117	
LOW POWER	I_{DSS}<90 µA
MINIMUM CIRCUIT LOADING	I_{GSS}<10 pA
ABSOLUTE MAXIMUM RATINGS @ 25°C (unless otherwise noted)	
Maximum Temperatures	
Storage Temperature	-65°C to +175°C
Operating Junction Temperature	-55°C to +150°C
Maximum Power Dissipation	
Continuous Power Dissipation	300mW
MAXIMUM CURRENT	
Gate Current (Note 1)	50mA
MAXIMUM VOLTAGES	
Gate to Drain or Gate to Source (Note 2)	-40V

LS4117 ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTIC	MIN	TYP.	MAX	UNITS	CONDITIONS
BV_{GSS}	Gate to Source Breakdown Voltage	-40	--	--	V	I_G = -1µA, V_{DS} = 0V
$V_{GS(off)}$	Gate to Source Cutoff Voltage	-0.6	--	-1.8	V	V_{DS} = 10V, I_D = 1nA
I_{DSS}	Gate to Source Saturation Current	0.03	--	0.09	mA	V_{DS} = 10V, V_{GS} = 0V
I_{GSS}	Gate Leakage Current	--	--	-10	pA	V_{GS} = -20V, V_{DS} = 0V
		--	--	-25		V_{GS} = -20V, V_{DS} = 0V, 150°C
g_{fs}	Forward Transconductance(Note 3)	70	--	210	µmho	V_{DS} = 10V, V_{GS} = 0V, f = 1kHz
g_{os}	Output Conductance	--	--	3		
C_{iss}	Input Capacitance	--	--	3	pF	V_{DS} = 10V, V_{GS} = 0V, f = 1MHz
C_{rss}	Reverse Transfer Capacitance	--	--	1.5		

NOTES	1 . Absolute maximum ratings are limiting values above which LS4117 serviceability may be impaired. 2. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged 3. This parameter is measured during a 2ms interval 100ms after power is applied. (Not a JEDEC condition.)

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Available Packages:

LS4117 in TO-92
LS4117 in bare die.

Please contact Micross for full package and die dimensions

TO-92 (Bottom View)