Integrated Circuit Systems, Inc.

ICS9148-17

Frequency Generator & Integrated Buffers for PENTIUM/Pro™

General Description

The **ICS9148-17** generates all clocks required for high speed RISC or CISC microprocessor systems such as Intel PentiumPro or Cyrix. Eight different reference frequency multiplying factors are externally selectable with smooth frequency transitions.

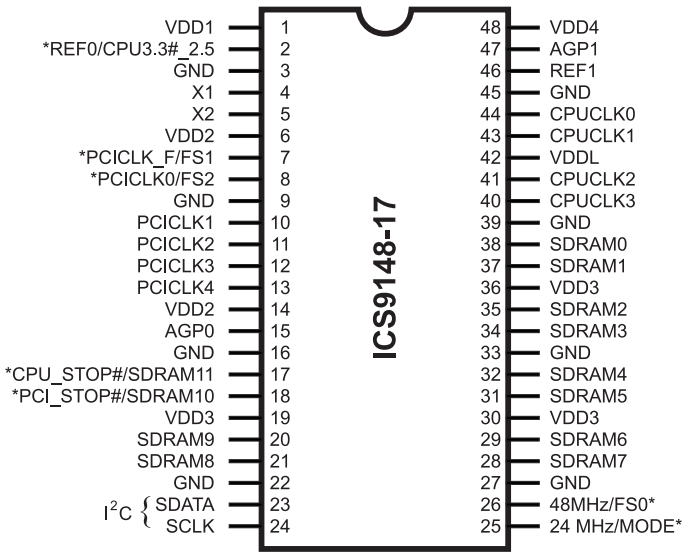
Features include four CPU, six PCI, two AGP (=2xPCI) and Twelve SDRAM clocks. Two reference outputs are available equal to the crystal frequency. One 48 MHz for USB, and one 24 MHz clock for Super IO. Built in ±1.5%, 0.6% center or down spread spectrum modulation to reduce EMI. Serial programming I^2C interface allows changing functions, stop clock programing and frequency selection. Additionally, the device meets the Pentium power-up stabilization, which requires that CPU and PCI clocks be stable within 2ms after power-up.

High drive PCICLK and SDRAM outputs typically provide greater than 1 V/ns slew rate into 30pF loads. CPUCLK outputs typically provide better than 1V/ns slew rate into 20pF loads while maintaining 50±5% duty cycle. The REF and 24 and 48 MHz clock outputs typically provide better than 0.5V/ns slew rates.

Features

- 3.3V outputs: SDRAM, AGP, PCI, REF, 48/24 MHz
- 2.5V or 3.3V outputs: CPU
- 20 ohm CPU clock output impedance
- 20 ohm PCI clock output impedance
- CPU to PCI skew = 2 to 6ns
- No external load cap for C_L=18pF crystals
- 250 ps max CPU, PCI clock skew
- Smooth CPU frequency transition among all CPU frequencies.
- I^2C interface for programming
- 2ms power up clock stable time
- Clock duty cycle 45-55%.
- 48 pin 300 mil SSOP package
- 3.3V operation, 5V tolerant inputs.

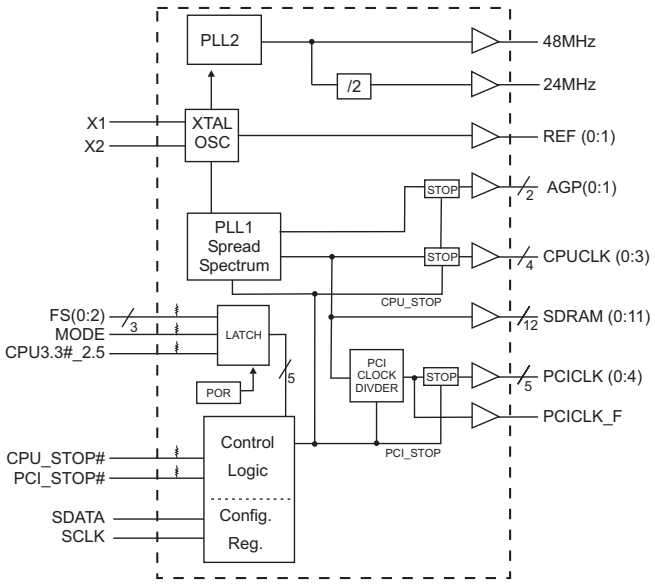
Pin Configuration



48-Pin SSOP

* Internal Pull-up Resistor of 240K to 3.3V on indicated inputs

Block Diagram



Power Groups

VDD1 = REF (0:1), X1, X2
VDD2 = PCICLK_F, PCICLK(0:5)
VDD3 = SDRAM (0:11), supply for PLL core, 24 MHz, 48MHz
VDD4 = AGP (0:1)
VDDL = CPUCLK (0:3)

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I^2C is a trademark of Philips Corporation

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	VDD1	PWR	Ref (0:2), XTAL power supply, nominal 3.3V
2	REF0	OUT	14.318 MHz reference clock.
	CPU3.3#_2.5[1,2]	IN	Indicates whether VDDL is 3.3V or 2.5V. High=2.5V CPU, LOW=3.3V CPU[1]. Latched input.
3,9,16,22,27, 33,39,45	GND	PWR	Ground.
4	X1	IN	Crystal input, has internal load cap (33pF) and feedback resistor from X2.
5	X2	OUT	Crystal output, nominally 14.318MHz. Has internal load cap (33pF).
6,14	VDD2	PWR	Supply for PCICLK_F and PCICLK (0:4), nominal 3.3V
7	PCICLK_F	OUT	Free running PCI clock
	FS1[1, 2]	IN	Frequency select pin. Latched input
8	PCICLK0	OUT	PCI clock output.
	FS2[1, 2]	IN	Frequency select pin. Latched input
10, 11, 12, 13	PCICLK (1:4)	OUT	PCI clock outputs.
15, 47	AGP (0:1)	OUT	Advanced Graphic Port outputs, powered by VDD4.
17	CPU_STOP#[1]	IN	Halts CPUCLK (0:3) clocks and AGP (0:1) clocks at logic 0 level, when input low (in Mobile Mode, MODE=0)
	SDRAM 11	OUT	SDRAM clock output
18	PCI_STOP#[1]	IN	Halts PCICLK (0:5) clocks at logic 0 level, when input low (in mobile mode, MODE=0)
	SDRAM 10	OUT	SDRAM clock output
20, 21,28, 29, 31, 32, 34, 35,37,38	SDRAM (0:9)	OUT	SDRAM clock outputs.
19,30,36	VDD3	PWR	Supply for SDRAM (0:11), Core, 24MHz and 48MHz clocks, nominal 3.3V.
23	SDATA	IN	Data input for I^2C serial input.
24	SCLK	IN	Clock input of I^2C input
25	24MHz	OUT	24MHz output clock.
	MODE[1, 2]	IN	Pin 17, 18 function select pin, 1=Desktop Mode, 0=Mobile Mode. Latched input.
26	48MHz	OUT	48MHz output clock
	FS0[1, 2]	IN	Frequency select pin. Latched input
40, 41, 43, 44	CPUCLK (0:3)	OUT	CPU clock outputs, powered by VDDL.
42	VDDL	PWR	Supply for CPU (0:3), either 2.5V or 3.3V nominal
46	REF1	OUT	14.318MHz reference clock.
48	VDD4	PWR	Supply for AGP (0:1)

Notes:

1: Internal Pull-up Resistor of 240K to 3.3V on indicated inputs

2: Bidirectional input/output pins, input logic levels are latched at internal power-on-reset. Use 10Kohm resistor to program logic Hi to VDD or GND for logic low.

Mode Pin - Power Management Input Control

MODE, Pin 25 (Latched Input)	Pin 17	Pin 18
0	CPU_STOP# (INPUT)	PCI_STOP# (INPUT)
1	SDRAM 11 (OUTPUT)	SDRAM 10 (OUTPUT)

Power Management Functionality

CPU_STOP#	PCI_STOP#	AGP, CPUCLK Outputs	PCICLK (0:5)	PCICLK_F, REF, 24/48MHz and SDRAM	Crystal OSC	VCO
0	1	Stopped Low	Running	Running	Running	Running
1	1	Running	Running	Running	Running	Running
1	0	Running	Stopped Low	Running	Running	Running

CPU 3.3#_2.5V Buffer selector for CPUCLK drivers.

CPU3.3#_2.5 Input level (Latched Data)	Buffer Selected for operation at:
1	2.5V VDD
0	3.3V VDD

Functionality

$V_{DD}1, 2, 3, 4 = 3.3V \pm 5\%$, $V_{DDL} = 2.5V \pm 5\%$ or $3.3 \pm 5\%$, TA= 0 to 70°C
Crystal (X1, X2) = 14.31818MHz

FS2	FS1	FS0	CPU, SDRAM (MHz)	PCI (MHz)	AGP (MHz)	REF, IOAPIC (MHz)
1	1	1	100.2	33.4	66.8	14.318
1	1	0	90	30	60	14.318
1	0	1	83.3	32	64	14.318
1	0	0	75	32	64	14.318
0	1	1	75	37.5	75	14.318
0	1	0	68.5	34.25	68.5	14.318
0	0	1	66.8	33.4	66.8	14.318
0	0	0	60	30	60	14.318

General I^2C serial interface information

The information in this section assumes familiarity with I^2C programming.
For more information, contact ICS for an I^2C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D2_{(H)}$	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Stop Bit	

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address $D3_{(H)}$
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 5***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D3_{(H)}$	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I^2C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I^2C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

Serial Configuration Command Bitmap

Byte0: Functionality and Frequency Select Register (default = 0)

Bit	Description				PWD
Bit 7	0 - ±1.5% Spread Spectrum Modulation 1 - ±0.6% Spread Spectrum Modulation				0
Bit 6:4	Bit 6,5,4	CPU Clock	PCI	AGP	Note 1 0,0,0
	111	100.2	33.4	66.8	
	110	90	30	60	
	101	83.3	32	64	
	100	75	32	64	
	011	75	37.5	75	
	010	68.5	34.25	68.5	
	001	66.8	33.4	66.8	
	000	60	30	60	
Bit 3	0 - Frequency is selected by hardware select, Latched Inputs 1 - Frequency is selected by Bit 6:4 (above)				0
Bit 2	0 - Spread Spectrum center spread type. 1 - Spread Spectrum down spread type.				0
Bit 1	0 - Normal 1 - Spread Spectrum Enabled				0
Bit 0	0 - Running 1- Tristate all outputs				0

Note 1. Default at Power-up will be for latched logic inputs to define frequency. Bits 4, 5, 6 are default to 000, and if bit 3 is written to a 1 to use bits 6:4, then these should be defined to desired frequency at same write cycle.

Note: PWD = Power-Up Default

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Byte 1: CPU, Active/Inactive Register
(1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	-	0	Version bit
Bit 6	-	1	(Reserved)
Bit 5	-	1	(Reserved)
Bit 4	-	1	(Reserved)
Bit 3	40	1	CPUCLK3 (Act/Inact)
Bit 2	41	1	CPUCLK2 (Act/Inact)
Bit 1	43	1	CPUCLK1 (Act/Inact)
Bit 0	44	1	CPUCLK0 (Act/Inact)

Byte 2: PCI Active/Inactive Register
(1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	-	-	Latched FS1#
Bit 6	7	1	PCICLK_F (Act/Inact)
Bit 5	15	1	AGP0 (Act/Inact)
Bit 4	14	1	PCICLK4 (Act/Inact)
Bit 3	12	1	PCICLK3 (Act/Inact)
Bit 2	11	1	PCICLK2 (Act/Inact)
Bit 1	10	1	PCICLK1 (Act/Inact)
Bit 0	8	1	PCICLK0(Act/Inact)

Byte 3: SDRAM Active/Inactive Register
(1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	28	1	SDRAM7 (Act/Inact)
Bit 6	29	1	SDRAM6 (Act/Inact)
Bit 5	31	1	SDRAM5 (Act/Inact)
Bit 4	32	1	SDRAM4 (Act/Inact)
Bit 3	34	1	SDRAM3 (Act/Inact)
Bit 2	35	1	SDRAM2 (Act/Inact)
Bit 1	37	1	SDRAM1 (Act/Inact)
Bit 0	38	1	SDRAM0 (Act/Inact)

Byte 4: SDRAM Active/Inactive Register
(1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	-	-	Latched FS0#
Bit 6	-	1	(Reserved)
Bit 5	-	1	(Reserved)
Bit 4	-	1	(Reserved)
Bit 3	17	1	SDRAM11 (Act/Inact) (Desktop Mode Only)
Bit 2	18	1	SDRAM10 (Act/Inact) (Desktop Mode Only)
Bit 1	20	1	SDRAM9 (Act/Inact)
Bit 0	21	1	SDRAM8 (Act/Inact)

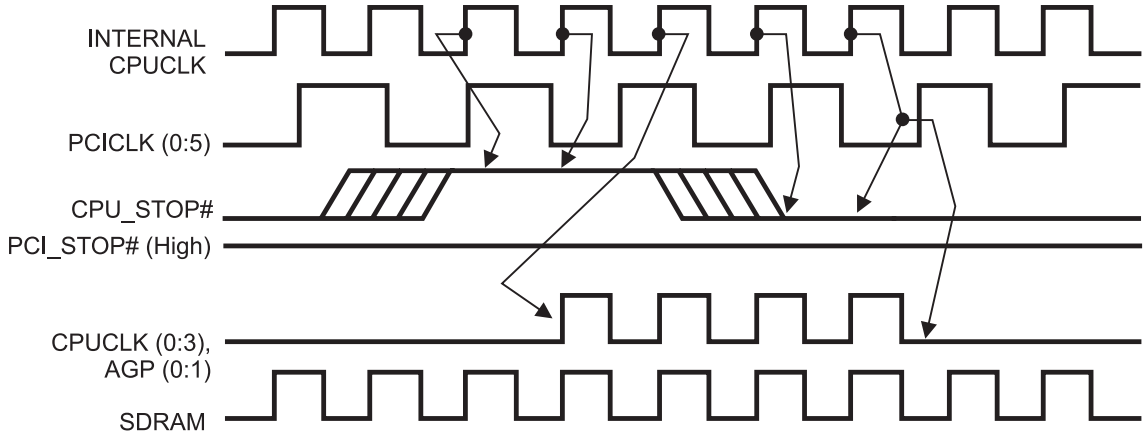
Byte 5: Peripheral Active/Inactive Register
(1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	-	-	Latched FS2#
Bit 6	-	1	(Reserved)
Bit 5	-	1	(Reserved)
Bit 4	47	1	AGP1(Act/Inact)
Bit 3	-	1	(Reserved)
Bit 2	-	1	(Reserved)
Bit 1	46	1	REF1 (Act/Inact)
Bit 0	2	1	REF0 (Act/Inact)

Notes:
1. Inactive means outputs are held LOW and are disabled from switching.
2. Latched Frequency selects will be Inverted logic level of the input frequency select pin conditions.

CPU_STOP# Timing Diagram

CPU_STOP# is an asychronous input to the clock synthesizer. It is used to turn off the CPU clocks for low power operation. CPU_STOP# is synchronized by the **ICS9148-17**. The minimum that the CPU clock is enabled (CPU_STOP# high pulse) is 100 CPU clocks. All other clocks will continue to run while the CPU clocks are disabled. The CPU clocks will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPU clock on latency is less than 4 CPU clocks and CPU clock off latency is less than 4 CPU clocks.

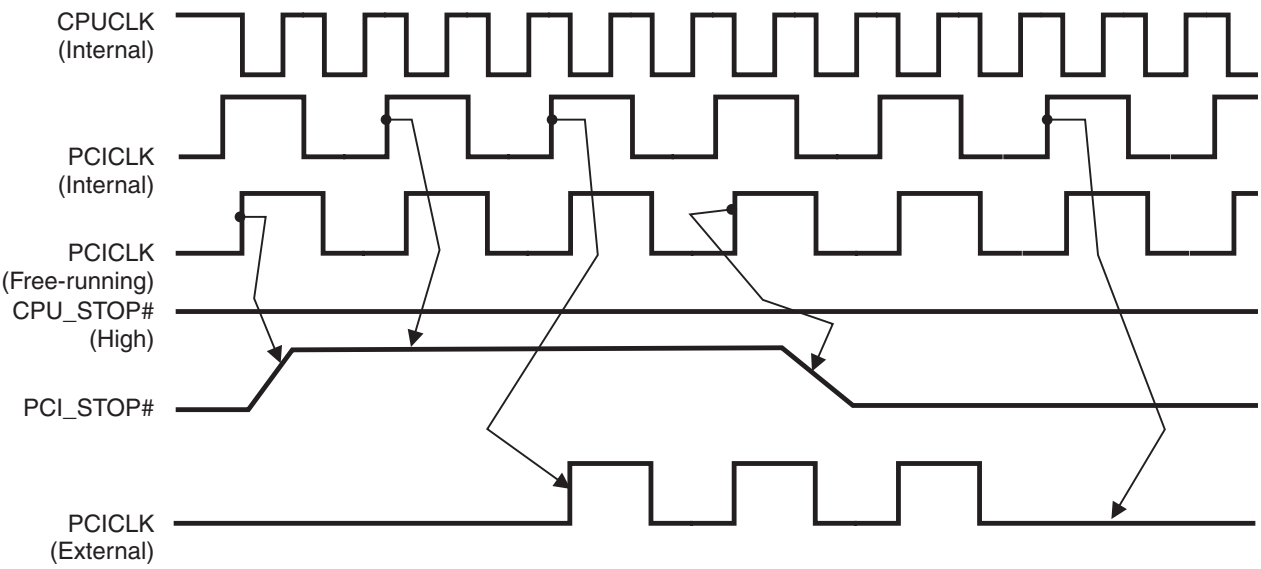


Notes:

1. All timing is referenced to the internal CPU clock.
2. CPU_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPU clocks inside the ICS9148-17.
3. All other clocks except CPU and AGP clocks continue to run undisturbed.

PCI_STOP# Timing Diagram

PCI_STOP# is an asynchronous input to the **ICS9148-17**. It is used to turn off the PCICLK (0:5) clocks for low power operation. PCI_STOP# is synchronized by the **ICS9148-17** internally. The minimum that the PCICLK (0:5) clocks are enabled (PCI_STOP# high pulse) is at least 10 PCICLK (0:5) clocks. PCICLK (0:5) clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK (0:5) clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.



Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9148 device.)
2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS9148.
3. All other clocks continue to run undisturbed.

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the ICS9148-17 serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

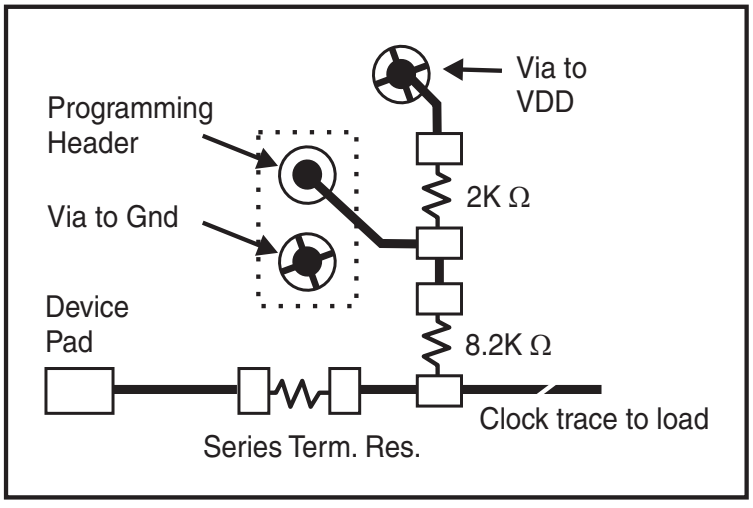


Fig. 1

Absolute Maximum Ratings

Supply Voltage . . . . . 7.0 V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = V_{DDL} = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}		0.1	5	µA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5	2.0		µA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200	-100		µA
Operating	$I_{DD3.3OP}$	C_L = 0 pF; 66.8 MHz		100	160	mA
Supply Current						
Input frequency	F_i	V_{DD} = 3.3 V;		14.318		MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27	36	45	pF
Transition Time[1]	T_{trans}	To 1st crossing of target Freq.			2	ms
Settling Time[1]	T_s	From 1st crossing to 1% target Freq.				ms
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			2	ms
Skew[1]	$T_{CPU-SDRAM1}$	V_T = 1.5 V; SDRAM Leads	-500	200	500	ps
	$T_{CPU-PCI1}$	V_T = 1.5 V; CPU Leads	2	5	6	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current	$I_{DD2.5OP}$	C_L = 0 pF; 66.8 MHz		10	20	mA
Skew[1]	$T_{CPU-SDRAM2}$	V_T = 1.5 V; V_{TL} = 1.25 V; SDRAM Leads	-500	200	500	ps
	$T_{CPU-PCI2}$	V_T = 1.5 V; V_{TL} = 1.25 V; CPU Leads	2	5	6	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPU

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH2A}	I_{OH} = -28 mA	2.5	2.6		V
Output Low Voltage	V_{OL2A}	I_{OL} = 27 mA		0.35	0.4	V
Output High Current	I_{OH2A}	V_{OH} = 2.0 V		-29	-23	mA
Output Low Current	I_{OL2A}	V_{OL} = 0.8 V	33	37		mA
Rise Time	t_{r2A}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.75	2	ns
Fall Time	t_{f2A}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.1	2	ns
Duty Cycle	d_{t2A}[1]	V_T = 1.5 V	45	50	55	%
Skew	t_{sk2A}[1]	V_T = 1.5 V		50	250	ps
Jitter, One Sigma	t_{j1s2A}[1]	V_T = 1.5 V		65	150	ps
Jitter, Absolute	t_{jabs2A}[1]	V_T = 1.5 V	-250	165	250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPU

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5V +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	VOH2B	I_{OH} = -8 mA	2	2.2		V
Output Low Voltage	VOL2B	I_{OL} = 12 mA		0.3	0.4	V
Output High Current	IOH2B	V_{OH} = 1.7 V		-20	-16	mA
Output Low Current	IOL2B	V_{OL} = 0.7 V	19	26		mA
Rise Time	tr2B[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V		1.5	1.8	ns
Fall Time	tf2B[1]	V_{OH} = 2.0 V, V_{OL} = 0.4 V		1.6	1.8	ns
Duty Cycle	dt2B[1]	V_T = 1.25 V	40	47	55	%
Skew	tsk2B[1]	V_T = 1.25 V		60	250	ps
Jitter, Single Edge Displacement[2]	tjsed2B[1]	V_T = 1.25 V		200	250	ps
Jitter, One Sigma	tj1s2B[1]	V_T = 1.25 V		65	150	ps
Jitter, Absolute	tjabs2B[1]	V_T = 1.25 V	-300	160	300	ps

[1] Guaranteed by design, not 100% tested in production.

[2] Edge displacement of a period relative to a 10-clock-cycle rolling average period.

Electrical Characteristics - PCI

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-10%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -28 mA	2.4	3		V
Output Low Voltage	V_{OL1}	I_{OL} = 23 mA		0.2	0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V		-60	-40	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	41	50		mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.8	2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.6	2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	51	55	%
Skew	t_{sk1}[1]	V_T = 1.5 V		130	250	ps
Jitter, One Sigma[1]	t_{j1s1a}	V_T = 1.5 V, synchronous		40	150	ps
	t_{j1s1b}	V_T = 1.5 V, asynchronous		200	250	ps
Jitter, Absolute[1]	tab_{s1a}	V_T = 1.5 V, synchronous	-250	135	250	ps
	t_{jabs1b}	V_T = 1.5 V, asynchronous	-650	500	650	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 30 pF

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -28 mA	2.4	3		V
Output Low Voltage	V_{OL1}	I_{OL} = 23 mA		0.2	0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V		-60	-40	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	41	50		mA
Rise Time[1]	T_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.75	2	ns
Fall Time[1]	T_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.5	2	ns
Duty Cycle[1]	D_{t1}	V_T = 1.5 V	45	50	55	%
Skew[1]	T_{sk1}	V_T = 1.5 V		200	500	ps
Jitter, One Sigma[1]	T_{j1s1}	V_T = 1.5 V		50	150	ps
Jitter, Absolute[1]	T_{jabs1}	V_T = 1.5 V (with synchronous PCI)	-250		+250	ps
Jitter, Absolute[1]	T_{jabs1}	V_T = 1.5 V (with asynchronous PCI)	-400		400	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - AGP

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-10%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -28 mA	2.4	3		V
Output Low Voltage	V_{OL1}	I_{OL} = 23 mA		0.2	0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V		-60	-40	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	41	50		mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.1	2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1	2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.4 V	45	49	55	%
Skew	t_{sk1}[1]	V_T = 1.5 V		130	250	ps
Jitter, One Sigma[1]	t_{j1s1}	V_T = 1.5 V		2	3	%
Jitter, Absolute[1]	t_{abs1a}	V_T = 1.5 V, synchronous	-5	2.5	5	%
	t_{jabs1b}	V_T = 1.5 V, asynchronous	-6	4.5	6	%

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 24MHz, 48MHz, REF0

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-10%; C_L = 10 -20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -16 mA	2.4	2.6		V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA		0.3	0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V		-32	-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16	25		mA
Rise Time	t_{r5}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V		2	4	ns
Fall Time	t_{f5}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.9	4	ns
Duty Cycle	d_{t5}[1]	V_T = 1.5 V	45	54	57	%
Jitter, One Sigma	t_{j1s5}[1]	V_T = 1.5 V		1	3	%
Jitter, Absolute	t_{jabs5}[1]	V_T = 1.5 V	-5	-	5	%

[1]Guaranteed by design, not 100% tested in production.

General Layout Precautions:

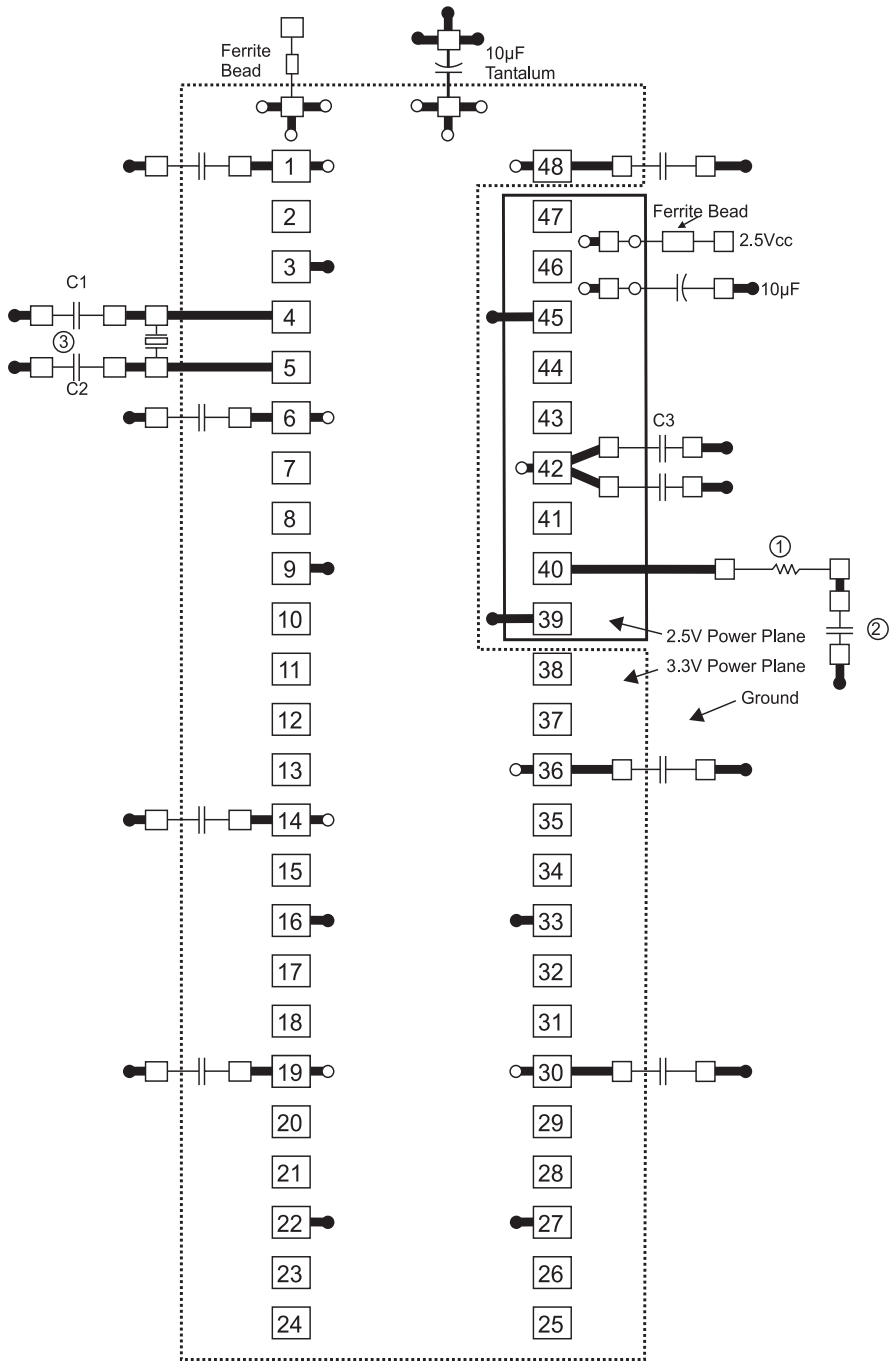
1) Use a ground plane on the top layer of the PCB in all areas not used by traces.
2) Make all power traces and vias as wide as possible to lower inductance.

Notes:

1 All clock outputs should have series terminating resistor. Not shown in all places to improve readibility of diagram

2 Optional EMI capacitor should be used on all CPU, SDRAM, and PCI outputs.

3 Optional crystal load capacitors are recommended.



Capacitor Values:

C1, C2 : Crystal load values determined by user

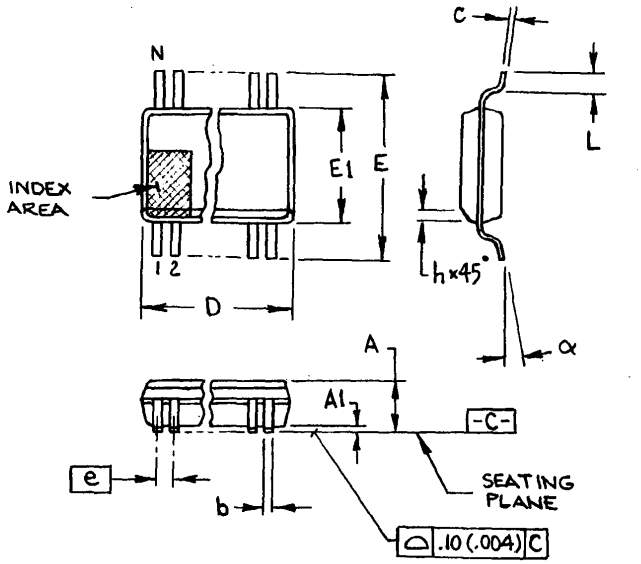
C3 : 100pF ceramic

All unmarked capacitors are 0.01µF ceramic

● = Ground Plane Connection

○ = Power Plane Conncetion

□ = Solder Pads



300 mil SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.40	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.00	10.70	.395	.420
E1	7.40	7.60	.291	.299
e	0.065 BASIC		0.025 BASIC	
h	0.40	0.65	.015	.025
L	0.50	1.00	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
28	9.40	9.65	.370	.380
34	11.30	11.55	.445	.455
48	15.75	16.00	.620	.630
56	18.30	18.55	.720	.730
64	20.80	21.05	.820	.830

Ordering Information

ICS9148yF-17-T

Example:

ICS XXXX y F - PPP - T

- **Designation for tape and reel packaging**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F=SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device