



High Performance Sensorless Motor Control IC

Description

IRMCK172M is a high performance One Time Programmable ROM based motion control IC designed and optimized for appliance control which contains two computation engines integrated into one monolithic chip. One is the Flexible Motion Control Engine (MCE™) for sensorless control of permanent magnet motors or induction motors; the other is an 8-bit high-speed microcontroller (8051). The user can program a motion control algorithm by connecting these control elements using a graphic compiler. Key components of the complex sensorless control algorithms, such as the Angle Estimator, are provided as complete pre-defined control blocks. A unique analog/digital circuit and algorithm fully supports single shunt or leg shunt current reconstruction. IRMCK172M comes in a 48 pin QFN package.

Features

- MCE™ (Flexible Motion Control Engine) - Dedicated computation engine for high efficiency sinusoidal sensorless motor control
- Built-in hardware peripheral for single or two shunt current feedback reconstruction and analog circuits
- Supports induction machine and both interior and surface permanent magnet motor sensorless control
- Loss minimization Space Vector PWM
- Two-channel analog output (PWM)
- Embedded 8-bit high speed microcontroller (8051) for flexible I/O and man-machine control
- JTAG programming port for emulation/debugger
- Serial communication interface (UART)
- I2C/SPI serial interface
- Internal 32Kbyte OTP ROM
- 3.3V single supply

Product Summary

Maximum clock input (fcystal)	60 MHz
Maximum Internal clock (SYSCLK)	128MHz
Maximum 8051 clock (8051CLK)	32MHz
MCETM computation data range	16 bit signed
8051/MCE Data RAM	2KB
MCE Program RAM	12KB
PWM carrier frequency	20 bits/ SYSCLK
A/D input channels	7
A/D converter resolution	12 bits
A/D converter conversion speed	2 µsec
Analog output (PWM) resolution	8 bits
UART baud rate (typ)	57.6 Kbps
Number of digital I/O (max)	10
Package (lead free)	QFN48
Maximum 3.3V operating current	60mA

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRMCK172M	QFN	Tray	1485	IRMCK172MTY
		Tape and Reel	3000	IRMCK172MTR

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1 Overview

IRMCK172M is a new generation International Rectifier integrated circuit device primarily designed as a one-chip solution for complete inverter controlled appliance motor control applications. Unlike a traditional microcontroller or DSP, the IRMCK172M provides a built-in closed loop sensorless control algorithm using the unique flexible Motion Control Engine (MCE™) for permanent magnet motors as well as induction motors. The MCE™ consists of a collection of control elements, motion peripherals, a dedicated motion control sequencer and dual port RAM to map internal signal nodes. IRMCK172M also employs a unique single shunt current reconstruction circuit in addition to two leg shunt current sensing circuit to eliminate additional analog/digital circuitry and enables a direct shunt resistor interface to the IC. Motion control programming is achieved using a dedicated graphical compiler integrated into the MATLAB/Simulink™ development environment. Sequencing, user interface, host communication, and upper layer control tasks can be implemented in the 8051 high-speed 8-bit microcontroller. The 8051 microcontroller is equipped with a JTAG port to facilitate emulation and debugging tools. Figure 1 shows a typical application schematic using the IRMCK172M.

IRMCK172M contains 32K bytes of OTP program ROM, The IRMCF172 contains 64K bytes of Flash RAM and intended for development purposes only while the IRMCK172M is intended for volume production. Both the development and ROM versions come in a 48-pin QFN package with identical pin configuration to facilitate PC board layout and transition to mass production.

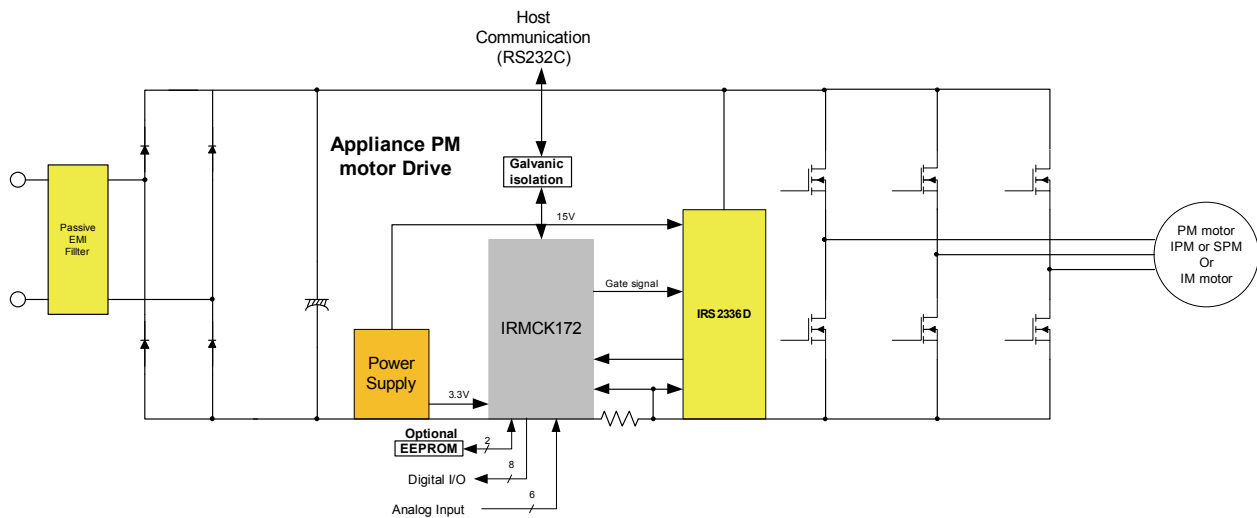


Figure 1 Typical Application Block Diagram Using IRMCK172M

2 Pinout

Pin out shown is based on QFN 7x7 48 pin package.

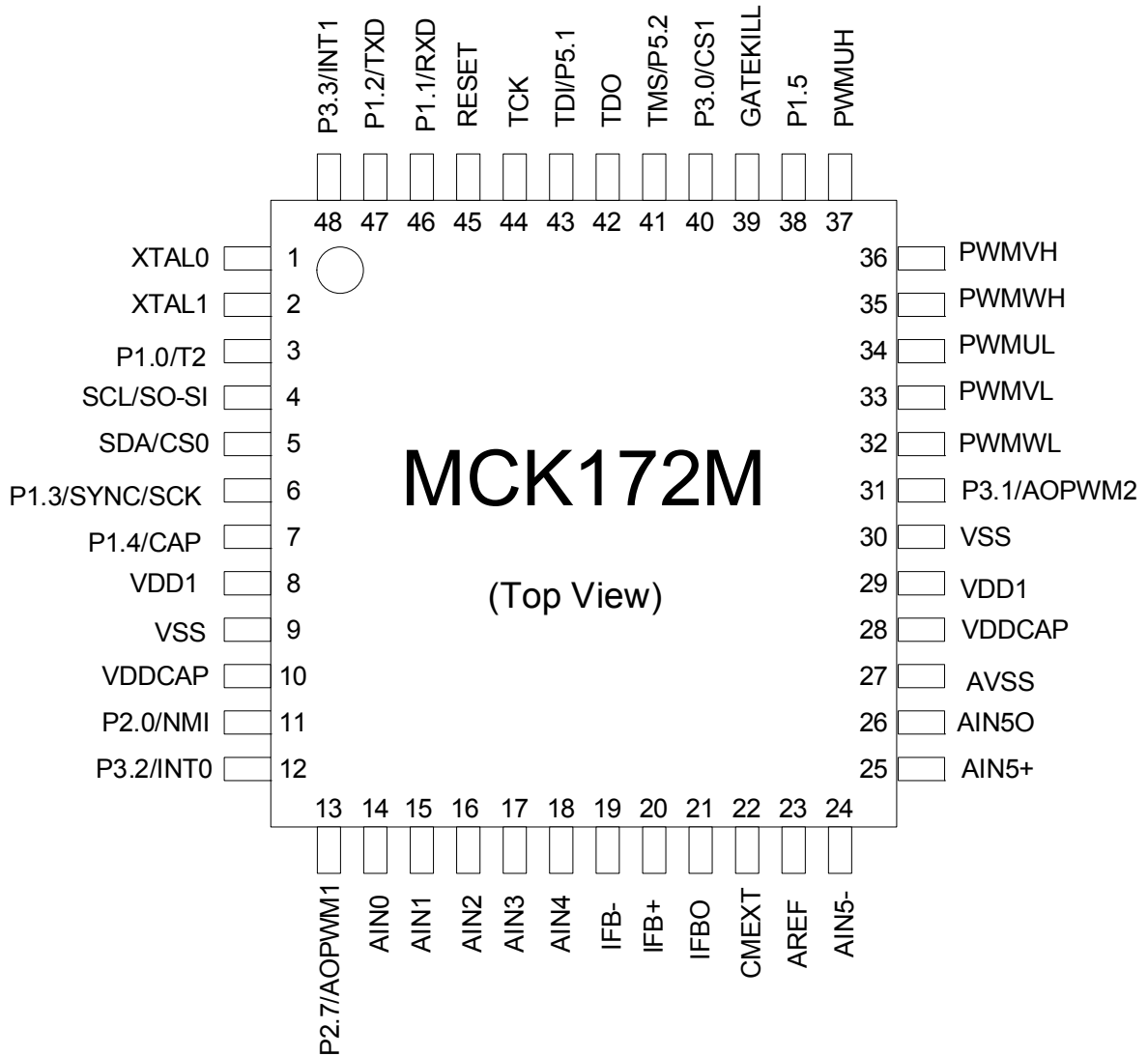


Figure 2 Pinout of IRMCK172M

3 IRMCK172M Block Diagram and Main Functions

IRMCK172M block diagram is shown in Figure 3.

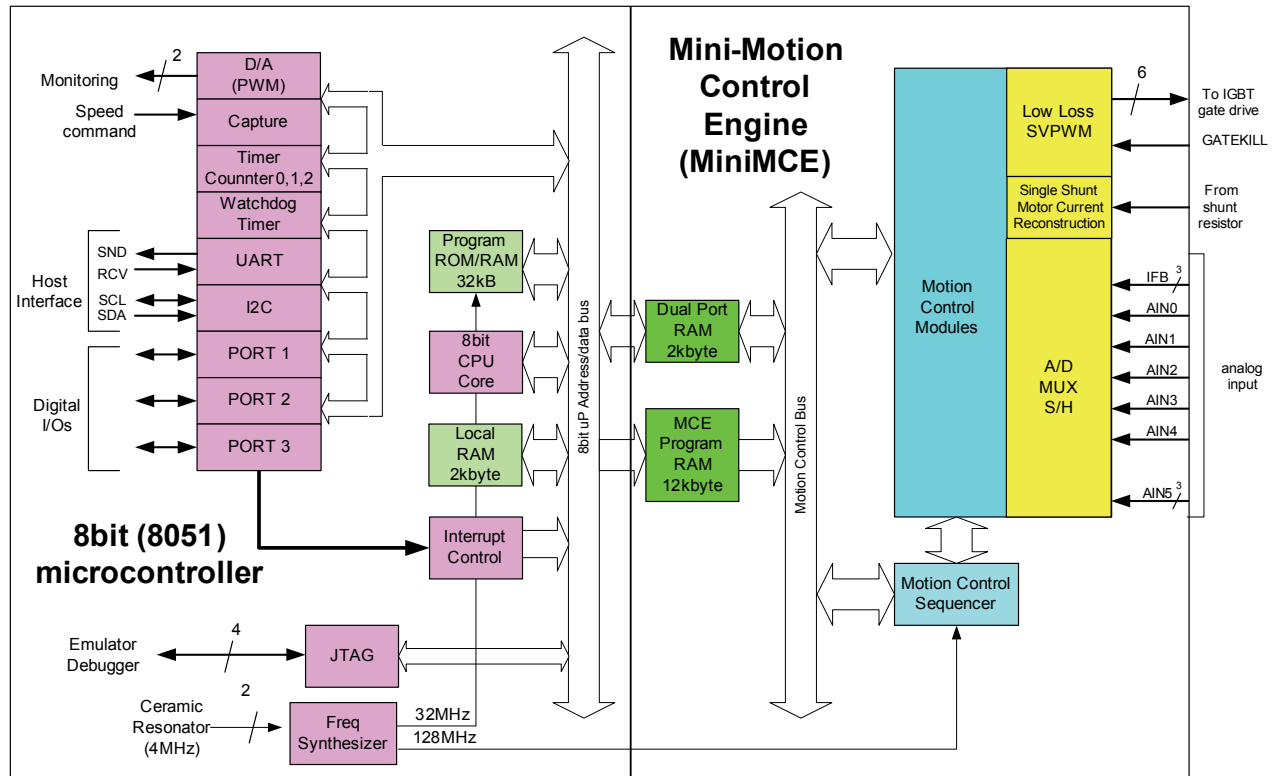


Figure 3 IRMCK172M Block Diagram

IRMCK172M contains the following functions for sensorless AC motor control applications:

- Motion Control Engine (MCE™)
 - Sensorless FOC (complete sensorless field oriented control)
 - Proportional plus Integral block
 - Low pass filter
 - Differentiator and lag (high pass filter)
 - Ramp
 - Limit
 - Angle estimate (sensorless control)
 - Inverse Clark transformation
 - Vector rotator
 - Bit latch

- Peak detect
- Transition
- Multiply-divide (signed and unsigned)
- Divide (signed and unsigned)
- Adder
- Subtractor
- Comparator
- Counter
- Accumulator
- Switch
- Shift
- ATAN (arc tangent)
- Function block (any curve fitting, nonlinear function)
- 16 bit wide Logic operations (AND, OR, XOR, NOT, NEGATE)
- MCE™ program memory and dual port RAM (max 12K+2k byte)
- MCE™ control sequencer
- 8051 microcontroller
 - Two 16 bit timer/counters
 - One 16 bit periodic timer
 - One 16 bit watchdog timer
 - One 16 bit capture timer
 - Up to 24 discrete I/Os
 - Seven-channel 12 bit A/D
 - Buffered (current sensing) two channels (0 – 1.2V input)
 - Unbuffered five channels (0 – 1.2V input)
 - JTAG port (4 pins)
 - Up to three channels of analog output (8 bit PWM)
 - UART
 - I²C/SPI port
 - 32K byte OTP program ROM
 - 2K byte data RAM

4 Application connection and Pin function

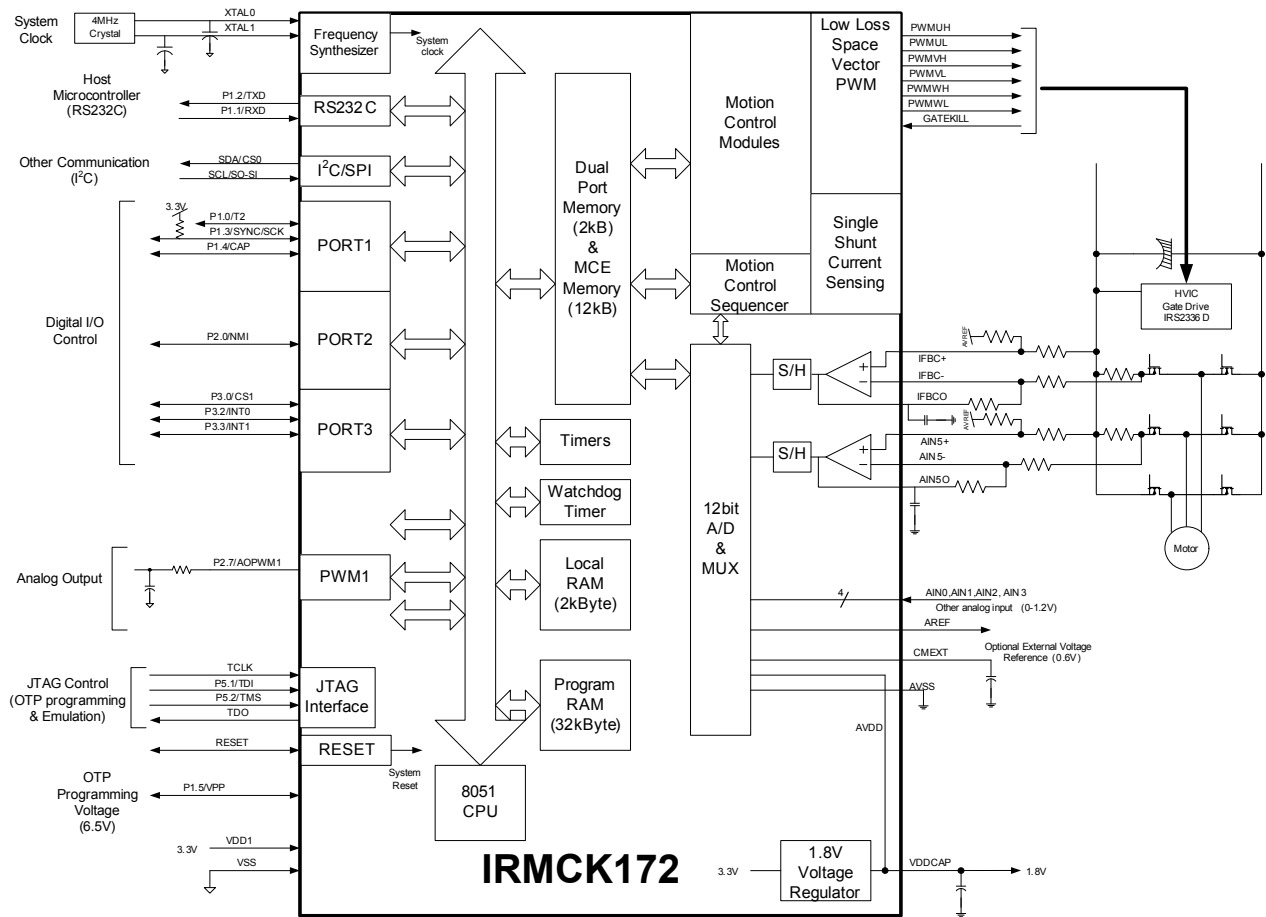


Figure 4 IRMCK172M Connection Diagram

4.1 8051 Peripheral Interface Group

UART Interface

P1.2/TXD

Output, Transmit data from IRMCK172M

P1.1/RXD Input, Receive data to IRMCK172M

Discrete I/O Interface

P1.0/T2 Input/output port 1.0, can be configured as Timer/Counter 2 input
P1.1/RXD Input/output port 1.1, can be configured as RXD input
P1.2/TXD Input/output port 1.2, can be configured as TXD output
P1.3/SYNC/SCK Input/output port 1.3, can be configured as SYNC output or SPI clock output, needs to be pulled up to VDD1 in order to boot from I²C EEPROM
P1.4/CAP Input/output port 1.4, can be configured as Capture Timer input
P1.5/VPP Input/output port 1.5, or OTP programming voltage
P2.0/NMI Input/output port 2.0, can be configured as non-maskable interrupt input
P3.2/INT0 Input/output port 3.2, can be configured as INT0 input
P2.7/AOPWM1 Input/output port 2.7, can be configured as AOPWM1 output
P3.0/INT2/CS1 Input/output port 3.0, can be configured as INT2 input or SPI chip select 1
P3.1/AOPWM2 Input/output port 3.1, can be configured as AOPWM2 output
P3.3/INT1 Input/output port 3.3, can be configured as INT1 input
P5.1/TDI Input port 5.1, configured as JTAG port by default
P5.2/TMS Input port 5.2, configured as JTAG port by default

Analog Output Interface

P2.7/AOPWM1 Input/output, can be configured as 8-bit PWM output 1 with programmable carrier frequency
P3.1/AOPWM2 Input/output, can be configured as 8-bit PWM output 2 with programmable carrier frequency

Crystal Interface

XTAL0 Input, connected to crystal
XTAL1 Output, connected to crystal

Reset Interface

RESET Input and Output, system reset, doesn't require external RC time constant

I²C Interface

SCL/SO-SI Output, I²C clock output, or SPI data
SDA/CS0 Input/output, I²C Data line or SPI chip select 0

I²C/SPI Interface

SCL/SO-SI Output, I²C clock output, or SPI data
SDA/CS0 Input/output, I²C data line or SPI chip select 0
P1.3/SYNC/SCK Input/output port 1.3, can be configured as SYNC output or SPI clock output, needs to be pulled up to VDD1 in order to boot from I²C EEPROM
P3.0/INT2/CS1 Input/output port 3.0, can be configured as INT2 input or SPI chip select 1

4.2 Motion Peripheral Interface Group

PWM

PWMUH	Output, PWM phase U high side gate signal, internally pulled down by 58kΩ
PWMUL	Output, PWM phase U low side gate signal, internally pulled down by 58kΩ
PWMVH	Output, PWM phase V high side gate signal, internally pulled down by 58kΩ
PWMVL	Output, PWM phase V low side gate signal, internally pulled down by 58kΩ
PWMWH	Output, PWM phase W high side gate signal, internally pulled down by 58kΩ
PWMWL	Output, PWM phase W low side gate signal, internally pulled down by 58kΩ

Fault

GATEKILL	Input, upon assertion, this negates all six PWM signals, active low, internally pulled up by 70kΩ
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4.3 Analog Interface Group

AVSS	Analog power return, (analog internal 1.8V power is shared with VDDCAP)
AREF	0.6V buffered output
CMEXT	Unbuffered 0.6V, input to the AREF buffer, capacitor needs to be connected.
IFB+	Input, Operational amplifier positive input for shunt resistor current sensing
IFB-	Input, Operational amplifier negative input for shunt resistor current sensing
IFBO	Output, Operational amplifier output for shunt resistor current sensing
AIN0	Input, Analog input channel 0 (0 – 1.2V), typically configured for DC bus voltage input
AIN1	Input, Analog input channel 1 (0 – 1.2V), needs to be pulled down to AVSS if unused
AIN2	Input, Analog input channel 2 (0 – 1.2V), needs to be pulled down to AVSS if unused
AIN3	Input, Analog input channel 3 (0 – 1.2V), needs to be pulled down to AVSS if unused
AIN4	Input, Analog input channel 4 (0 – 1.2V), needs to be pulled down to AVSS if unused
AIN5+	Input, Operational amplifier positive input for shunt resistor current sensing
AIN5-	Input, Operational amplifier negative input for shunt resistor current sensing
AIN5O	Output, Operational amplifier output for AIN5 output, there is a single sample/hold circuit on the output

4.4 Power Interface Group

VDD1	Digital power (3.3V)
VDDCAP	Internal 1.8V output, requires capacitors to the pin. Shared with analog power pad internally Note: The internal 1.8V supply is not designed to power any external circuits or devices. Only capacitors should be connected to this pin.
VSS	Digital common

4.5 Test Interface Group

P5.2/TMS	JTAG test mode input or input/output digital port
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TDO	JTAG data output
P5.1/TDI	JTAG data input, or input/output digital port
TCK	JTAG test clock

5 DC Characteristics

5.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Condition
V _{DD1}	Supply Voltage	-0.3 V	-	3.6 V	Respect to VSS
V _{IA}	Analog Input Voltage	-0.3 V	-	1.98 V	Respect to AVSS
V _{ID}	Digital Input Voltage	-0.3 V	-	6.0 V	Respect to VSS
V _{PP}	OTP Programming voltage	-0.3V	-	7.0V	Respect to VSS
T _A	Ambient Temperature	-40 °C	-	85 °C	
T _S	Storage Temperature	-65 °C	-	150 °C	

Table 1 Absolute Maximum Ratings

Caution: Stresses beyond those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and function of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

5.2 System Clock Frequency and Power Consumption

C_{AREF} = 1nF, C_{MEXT}= 100nF. VDD1=3.3V, Unless specified, Ta = 25°C.

Symbol	Parameter	Min	Typ	Max	Unit
SYSCCLK	System Clock	32	-	128	MHz
P _D	Power consumption		160 ¹⁾	200	mW

Table 2 System Clock Frequency

Note 1) The value is based on the condition of MCE clock=126MHz, 8051 clock 31.5MHz with a actual motor running by a typical MCE application program and 8051 code.

5.3 Digital I/O DC Characteristics

Symbol	Parameter	Min	Typ	Max	Condition
V_{DD1}	Supply Voltage	3.0 V	3.3 V	3.6 V	Recommended
V_{PP}	OTP Programming voltage	6.70V	6.75V	6.80V	Recommended
V_{IL}	Input Low Voltage	-0.3 V	-	0.8 V	Recommended
V_{IH}	Input High Voltage	2.0 V		3.6 V	Recommended
C_{IN}	Input capacitance	-	3.6 pF	-	(1)
I_L	Input leakage current		± 10 nA	± 1 μ A	$V_O = 3.3$ V or 0 V
$I_{OL1}^{(2)}$	Low level output current	8.9 mA	13.2 mA	15.2 mA	$V_{OL} = 0.4$ V (1)
$I_{OH1}^{(2)}$	High level output current	12.4 mA	24.8 mA	38 mA	$V_{OH} = 2.4$ V (1)
$I_{OL2}^{(3)}$	Low level output current	17.9 mA	26.3 mA	33.4 mA	$V_{OL} = 0.4$ V (1)
$I_{OH2}^{(3)}$	High level output current	24.6 mA	49.5 mA	81 mA	$V_{OH} = 2.4$ V (1)

Table 3 Digital I/O DC Characteristics

Note:

- (1) Data guaranteed by design.
- (2) Applied to SCL/SO-SI, SDA/CS0 pins.
- (3) Applied to all digital I/O pins except SCL/SO-SI and SDA/CS0 pins.

5.4 Analog I/O (IFB+,IFB-,IFBO, AIN5+,AIN5-,AIN5O) DC Characteristics

$C_{\text{AREF}} = 1\text{nF}$, $C_{\text{MEXT}} = 100\text{nF}$. $V_{\text{DD1}} = 3.3\text{V}$, Unless specified, $T_a = 25^\circ\text{C}$.

Symbol	Parameter	Min	Typ	Max	Condition
V_{OFFSET}	Input Offset Voltage	-	-	26 mV	
V_{I}	Input Voltage Range	0 V		1.2 V	Recommended
V_{OUTSW}	OP amp output operating range	50 mV ⁽¹⁾	-	1.2 V	
C_{IN}	Input capacitance	-	3.6 pF	-	⁽¹⁾
R_{FDBK}	OP amp feedback resistor	5 k Ω	-	20 k Ω	Requested between IFBO and IFB-
OP_{GAINCL}	Operating Close loop Gain	80 db	-	-	⁽¹⁾
CMRR	Common Mode Rejection Ratio	-	80 db	-	⁽¹⁾
I_{SRC}	Op amp output source current	-	1 mA	-	$V_{\text{OUT}} = 0.6\text{ V}$ ⁽¹⁾
I_{SNK}	Op amp output sink current	-	100 μA	-	$V_{\text{OUT}} = 0.6\text{ V}$ ⁽¹⁾

Table 4 Analog I/O DC Characteristics

Note:

(1) Data guaranteed by design.

5.5 Under Voltage Lockout DC characteristics

Unless specified, $T_a = 25^\circ\text{C}$.

Symbol	Parameter	Min	Typ	Max	Condition
UV _{CC+}	UV _{CC} positive going Threshold	2.78 V	3.04 V	3.23 V	(1)
UV _{CC-}	UV _{CC} negative going Threshold	2.78 V	2.97 V	3.23 V	
UV _{CCH}	UV _{CC} Hysteresys	-	73 mV	-	(1)

Table 5 UV_{CC} DC Characteristics

Note:

(1) Data guaranteed by design.

5.6 Itrip comparator DC characteristics

Unless specified, VDD1=3.3V, $T_a = 25^\circ\text{C}$.

Symbol	Parameter	Min	Typ	Max	Condition
Itrip ₊	Itrip positive going Threshold	-	1.22V	-	
Itrip ₋	Itrip negative going Threshold	-	1.10V	-	
ItripH	Itrip Hysteresys	-	120mV	-	

Table 6 Itrip DC Characteristics

5.7 CMEXT and AREF Characteristics

$C_{AREF} = 1\text{nF}$, $C_{MEXT} = 100\text{nF}$. Unless specified, $T_a = 25^\circ\text{C}$.

Symbol	Parameter	Min	Typ	Max	Condition
V _{CM}	CMEXT voltage	495 mV	600 mV	700 mV	VDD1 = 3.3 V ⁽¹⁾
V _{AREF}	Buffer Output Voltage	495 mV	600 mV	700 mV	VDD1 = 3.3 V
ΔV_o	Load regulation (V _{DC} -0.6)	-	1 mV	-	(1)
PSRR	Power Supply Rejection Ratio	-	75 db	-	(1)

Table 7 CMEXT and AREF DC Characteristics

Note:

(1) Data guaranteed by design.

6 AC Characteristics

6.1 Digital PLL AC Characteristics

Symbol	Parameter	Min	Typ	Max	Condition
F_{CLKIN}	Crystal input frequency	3.2 MHz	4 MHz	60 MHz	⁽¹⁾ (see figure below)
F_{PLL}	Internal clock frequency	32 MHz	50 MHz	128 MHz	⁽¹⁾
F_{LWPPW}	Sleep mode output frequency	$F_{CLKIN} \div 256$	-	-	⁽¹⁾
J_S	Short time jitter	-	200 psec	-	⁽¹⁾
D	Duty cycle	-	50 %	-	⁽¹⁾
T_{LOCK}	PLL lock time	-	-	500 μ sec	⁽¹⁾

Table 8 PLL AC Characteristics

Note:

(1) Data guaranteed by design.

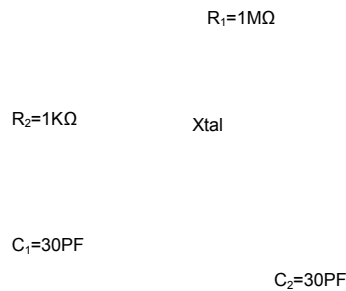


Figure 3 Crystal Circuit Example

6.2 Analog to Digital Converter AC Characteristics

Unless specified, $T_a = 25^\circ\text{C}$.

Symbol	Parameter	Min	Typ	Max	Condition
T_{CONV}	Conversion time	-	-	2.05 μsec	⁽¹⁾
T_{HOLD}	Sample/Hold maximum hold time	-	-	10 μsec	Voltage droop ≤ 15 LSB (see figure below)

Table 9 A/D Converter AC Characteristics

Note:

(1) Data guaranteed by design.

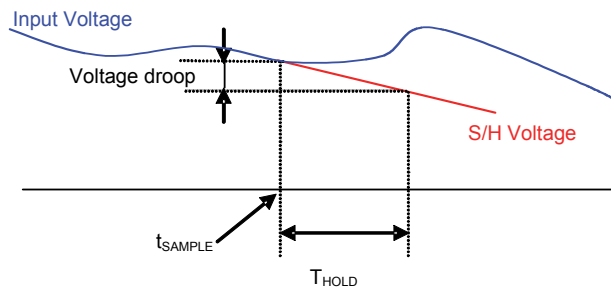


Figure 3 Voltage droop and S/H hold time

6.3 Op amp AC Characteristics

Unless specified, $T_a = 25^\circ\text{C}$.

Symbol	Parameter	Min	Typ	Max	Condition
OP_{SR}	OP amp slew rate	-	10 V/ μsec	-	$V_{DD1} = 3.3\text{ V}$, $CL = 33\text{ pF}$ ⁽¹⁾
OP_{IMP}	OP input impedance	-	$10^8\ \Omega$	-	⁽¹⁾ ⁽²⁾
T_{SET}	Settling time	-	400 ns	-	$V_{DD1} = 3.3\text{ V}$, $CL = 33\text{ pF}$ ⁽¹⁾

Table 10 Current Sensing OP Amp AC Characteristics

Note:

(1) Data guaranteed by design.

(2) To guarantee stability of the operational amplifier, it is recommended to load the output pin by a capacitor of 47pF, see Figure 4. Here only the single shunt current amplifier is show but all op amp outputs should be loaded with this capacitor.

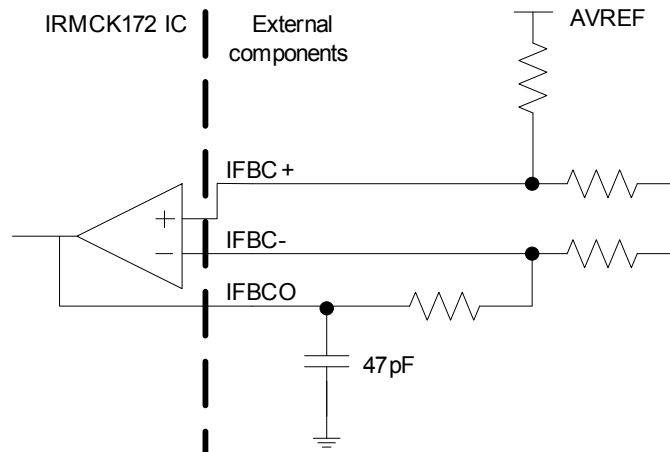


Figure 4 A capacitor of 47pF is recommended at the output pin of all op amps.

6.4 SYNC to SVPWM and A/D Conversion AC Timing

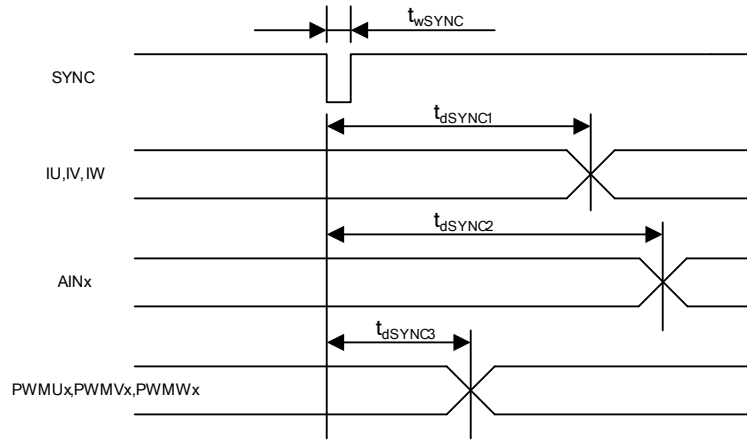


Figure 5 SYNC timing

Unless specified, Ta = 25°C.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{w\text{SYNC}}$	SYNC pulse width	-	32	-	SYSCLK
$t_{d\text{SYNC}1}$	SYNC to current feedback conversion time	-	-	100	SYSCLK
$t_{d\text{SYNC}2}$	SYNC to AIN0-5 analog input conversion time	-	-	200	SYSCLK (1)
$t_{d\text{SYNC}3}$	SYNC to PWM output delay time	-	-	2	SYSCLK

Table 11 SYNC AC Characteristics

Note:

(1) AIN1 through AIN5 channels are converted once every 6 SYNC events

6.5 GATEKILL to SVPWM AC Timing

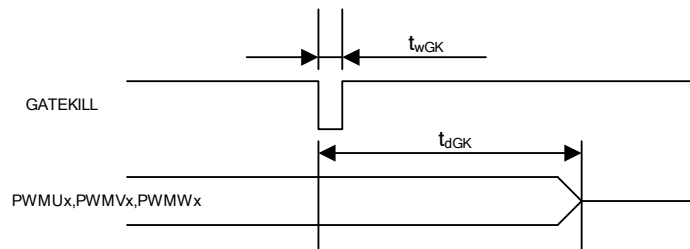


Figure 6 Gatekill timing

Unless specified, $T_a = 25^\circ\text{C}$.

Symbol	Parameter	Min	Typ	Max	Unit
t_{wGK}	GATEKILL pulse width	32	-	-	SYSCCLK
t_{dGK}	GATEKILL to PWM output delay	-	-	100	SYSCCLK

Table 12 GATEKILL to SVPWM AC Timing

6.6 Itrip AC Timing

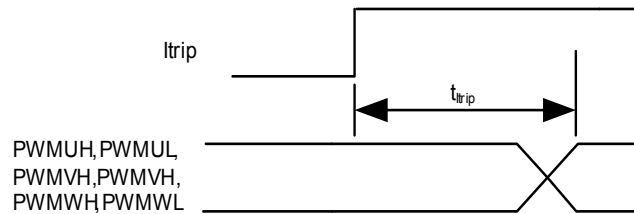


Figure 7 ITRIP timing

Unless specified, $T_a = 25^\circ\text{C}$.

Symbol	Parameter	Min	Typ	Max	Unit
t_{ITRIP}	Itrip propagation delay	-	-	$100(\text{sysclk})+1.0\text{usec}$	SYSCCLK+usec

Table 13 Itrip AC Timing

6.7 Interrupt AC Timing

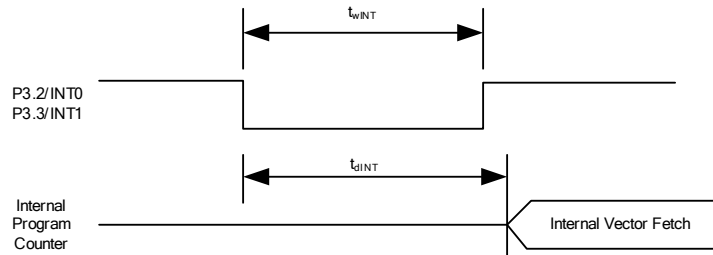


Figure 8 Interrupt timing

Unless specified, $T_a = 25^\circ\text{C}$.

Symbol	Parameter	Min	Typ	Max	Unit
t_{wINT}	INT0, INT1 Interrupt Assertion Time	4	-	-	SYSCCLK
t_{dINT}	INT0, INT1 latency	-	-	4	SYSCCLK

Table 14 Interrupt AC Timing

6.8 I²C AC Timing

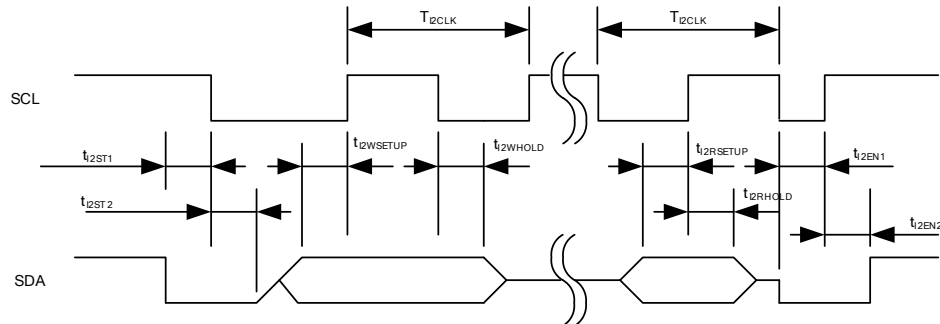


Figure 9 I²C Timing

Unless specified, $T_a = 25^\circ\text{C}$.

Symbol	Parameter	Min	Typ	Max	Unit
T_{I2CLK}	I ² C clock period	10	-	8192	SYSCCLK
t_{I2ST1}	I ² C SDA start time	0.25	-	-	T_{I2CLK}
t_{I2ST2}	I ² C SCL start time	0.25	-	-	T_{I2CLK}
$t_{I2WSETUP}$	I ² C write setup time	0.25	-	-	T_{I2CLK}
$t_{I2WHOLD}$	I ² C write hold time	0.25	-	-	T_{I2CLK}
$t_{I2RSETUP}$	I ² C read setup time	I ² C filter time ⁽¹⁾	-	-	SYSCCLK
$t_{I2RHOLD}$	I ² C read hold time	1	-	-	SYSCCLK

Table 15 I²C AC Timing

Note:

(1) I²C read setup time is determined by the programmable filter time applied to I²C communication.

6.9 SPI AC Timing

SPI Write AC timing

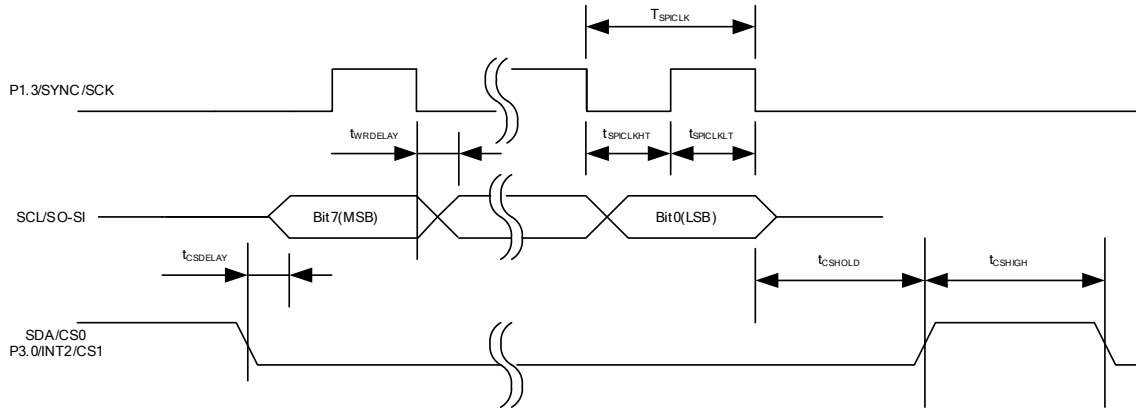
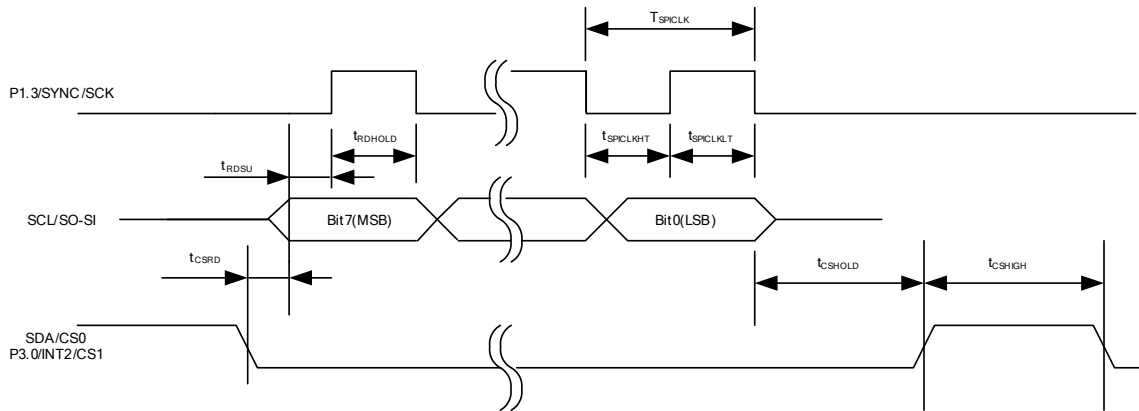


Figure 10 SPI write timing

Unless specified, $T_a = 25^\circ\text{C}$.

Symbol	Parameter	Min	Typ	Max	Unit
T_{SPICLK}	SPI clock period	4	-	-	SYSCLK
$t_{SPICLKHT}$	SPI clock high time	-	1/2	-	T_{SPICLK}
$t_{SPICLKLT}$	SPI clock low time	-	1/2	-	T_{SPICLK}
$t_{CSDELAY}$	CS to data delay time	-	-	10	nsec
$t_{WRDELAY}$	CLK falling edge to data delay time	-	-	10	nsec
t_{CSHIGH}	CS high time between two consecutive byte transfer	1	-	-	T_{SPICLK}
t_{CSHOLD}	CS hold time	-	1	-	T_{SPICLK}

Table 16 SPI Write AC Timing

SPI Read AC Timing

Figure 11 SPI read timing

 Unless specified, $T_a = 25^\circ\text{C}$.

Symbol	Parameter	Min	Typ	Max	Unit
T_{SPICLK}	SPI clock period	4	-	-	SYSClk
t_{SPICLKHT}	SPI clock high time	-	1/2	-	T_{SPICLK}
t_{SPICLKLT}	SPI clock low time	-	1/2	-	T_{SPICLK}
t_{CSRd}	CS to data delay time	-	-	10	nsec
t_{RDSU}	SPI read data setup time	10	-	-	nsec
t_{RDHOLD}	SPI read data hold time	10	-	-	nsec
t_{CSHIGH}	CS high time between two consecutive byte transfer	1	-	-	T_{SPICLK}
t_{CSHOLD}	CS hold time	-	1	-	T_{SPICLK}

Table 17 SPI Read AC Timing

6.10 UART AC Timing

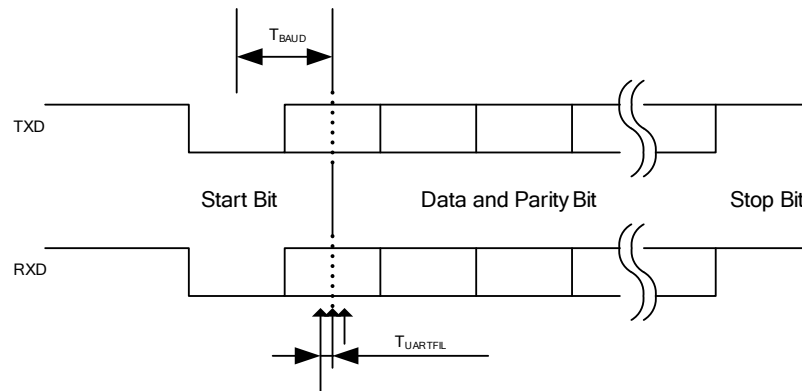


Figure 12 UART timing

Unless specified, $T_a = 25^\circ\text{C}$.

Symbol	Parameter	Min	Typ	Max	Unit
T_{BAUD}	Baud Rate Period	-	57600	-	bit/sec
T_{UARTFIL}	UART sampling filter period ⁽¹⁾	-	1/16	-	T_{BAUD}

Table 18 UART AC Timing

Note:

- (1) Each bit including start and stop bit is sampled three times at center of a bit at an interval of $1/16 T_{\text{BAUD}}$. If three sampled values do not agree, then UART noise error is generated.

6.11 CAPTURE Input AC Timing

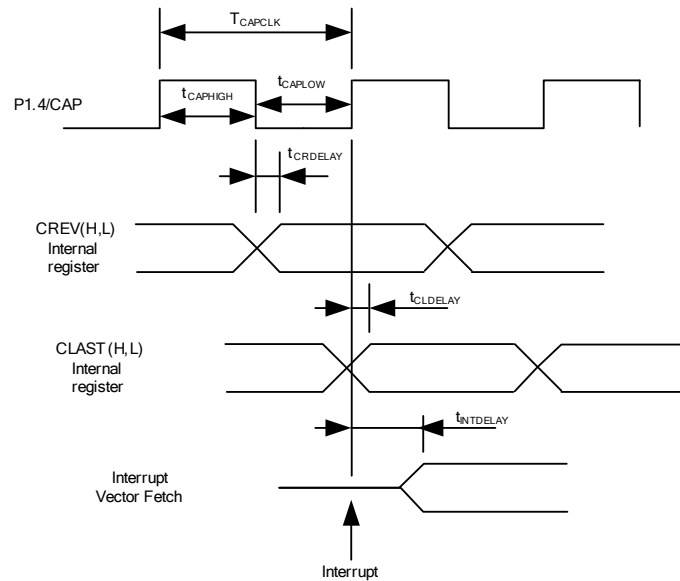


Figure 13 CAPTURE timing

Unless specified, $T_a = 25^\circ\text{C}$.

Symbol	Parameter	Min	Typ	Max	Unit
T_{CAPCLK}	CAPTURE input period	8	-	-	SYSCLK
$t_{CAPHIGH}$	CAPTURE input high time	4	-	-	SYSCLK
t_{CAPLOW}	CAPTURE input low time	4	-	-	SYSCLK
$t_{CRDELAY}$	CAPTURE falling edge to capture register latch time	-	-	4	SYSCLK
$t_{CLDELAY}$	CAPTURE rising edge to capture register latch time	-	-	4	SYSCLK
$t_{INTDELAY}$	CAPTURE input interrupt latency time	-	-	4	SYSCLK

Table 19 CAPTURE AC Timing

6.12 OTP Programming Timing

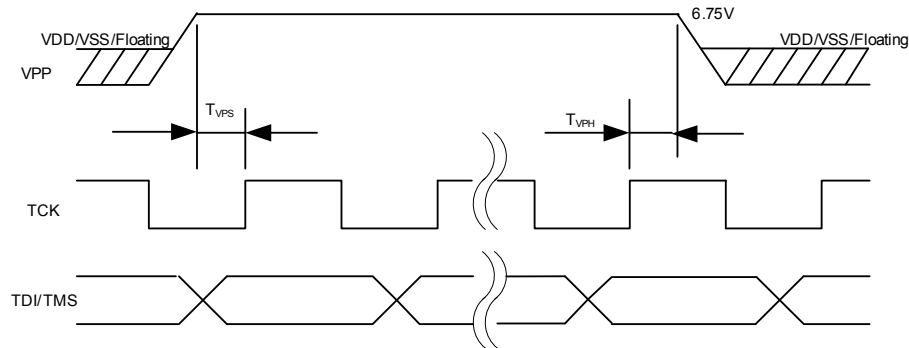


Figure 14 OTP programming timing

Unless specified, $T_a = 25^\circ\text{C}$.

Symbol	Parameter	Min	Typ	Max	Unit
T_{VPS}	VPP Setup Time	10	-	-	nsec
T_{VPH}	VPP Hold Time	15	-	-	nsec

Table 20 OTP Programming Timing

6.13 JTAG AC Timing

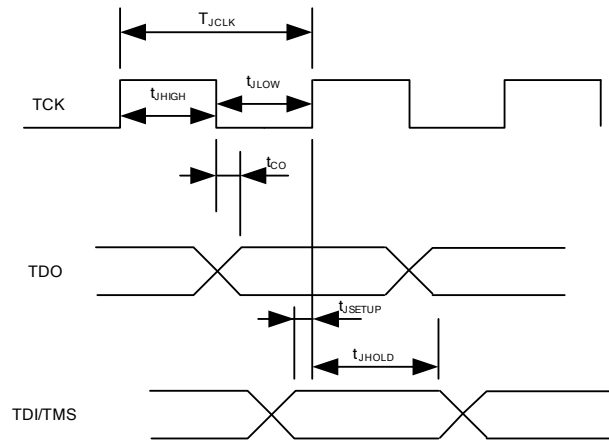


Figure 15 JTAG timing

Unless specified, $T_a = 25^\circ\text{C}$.

Symbol	Parameter	Min	Typ	Max	Unit
T_{JCLK}	TCK Period	-	-	50	MHz
t_{JHIGH}	TCK High Period	10	-	-	nsec
t_{JLOW}	TCK Low Period	10	-	-	nsec
t_{CO}	TCK to TDO propagation delay time	0	-	5	nsec
t_{JSETUP}	TDI/TMS setup time	4	-	-	nsec
t_{JHOLD}	TDI/TMS hold time	0	-	-	nsec

Table 21 JTAG AC Timing

7 I/O Structure

The following figure shows the motor PWM output (PWMUH/PWMUL/PWMVH/PWMVL/PWMWH/PWMWL)

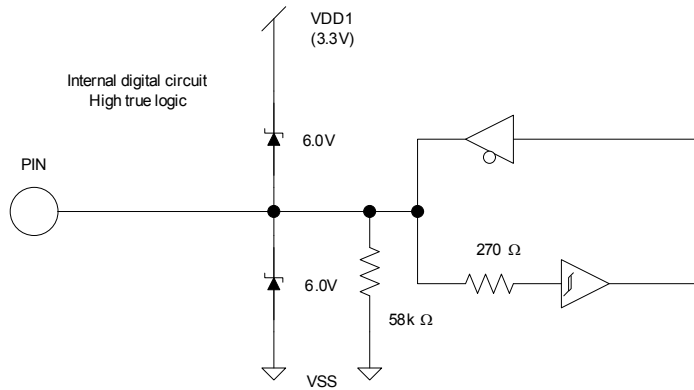


Figure 16 PWMUL/PWMUH/PWMVL/PWMVH/PWMWL/PWMWH output

The following figure shows the digital I/O structure except the motor PWM output

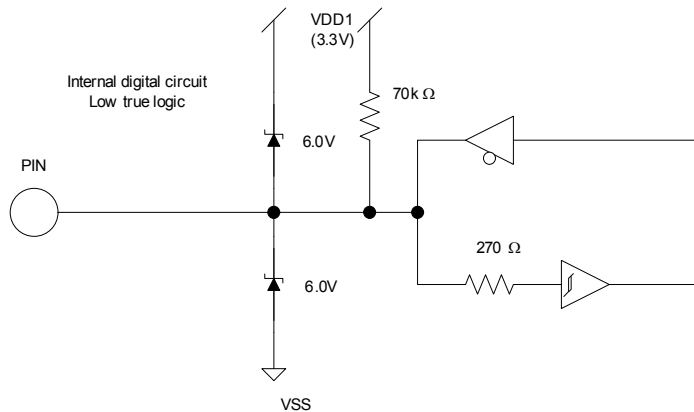


Figure 17 All digital I/O except motor PWM output

The following figure shows RESET and GATEKILL I/O structure.

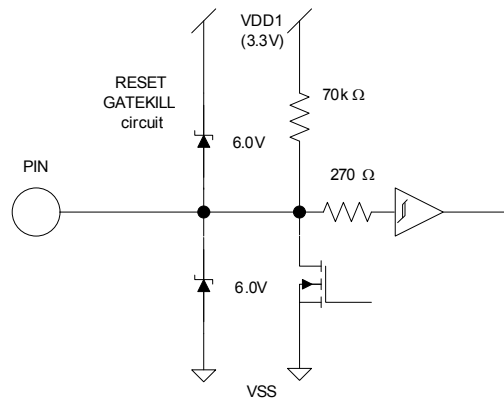


Figure 18 RESET, GATEKILL I/O

The following figure shows the analog input structure.

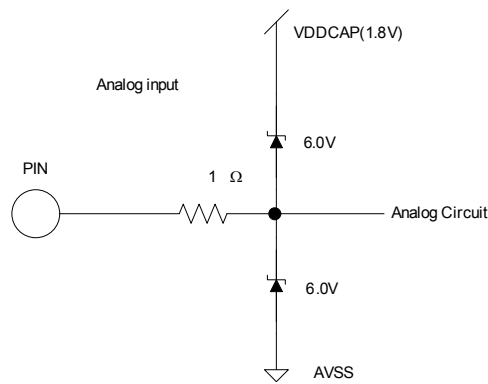


Figure 19 Analog input

The following figure shows all analog operational amplifier output pins and AREF pin I/O structure.

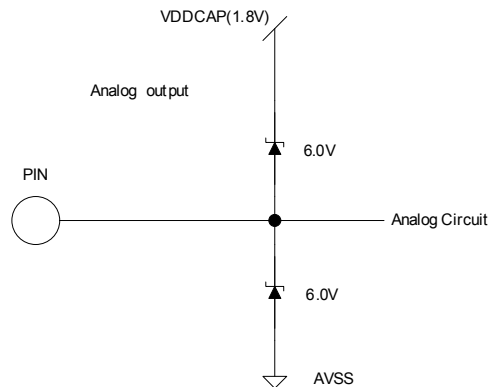


Figure 20 Analog operational amplifier output and AREF I/O structure

The following figure shows the VPP pin structure

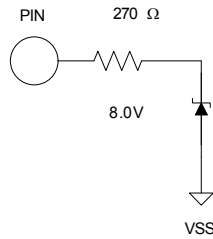


Figure 21 VPP programming pin I/O structure

The following figure shows the VSS and AVSS pins structure

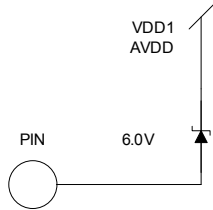


Figure 22 VSS and AVSS pin structure

The following figure shows the VDD1 and VDDCAP pin structure

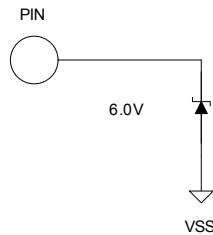


Figure 23 VDD1 and VDDCAP pin structure

The following figure shows the XTAL0 and XTAL1 pins structure

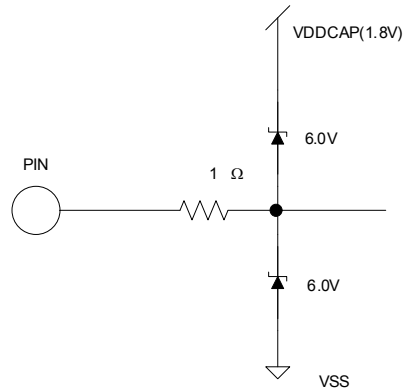


Figure 24 XTAL0/XTAL1 pins structure

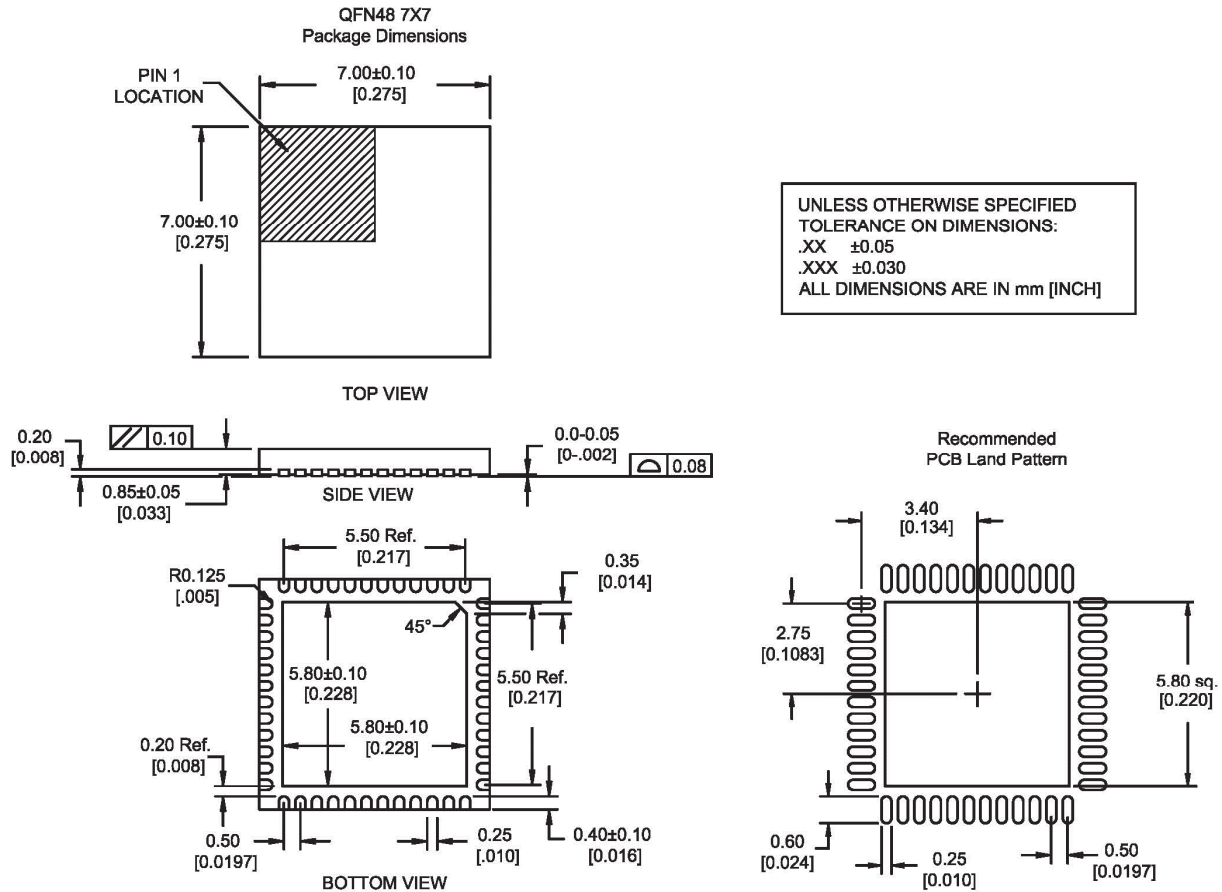
8 Pin List

Pin Number	Pin Name	Internal Pull-up /Pull-down	Pin Type	Description
1	XTAL0		I	Crystal input
2	XTAL1		O	Crystal output
3	P1.0/T2		I/O	Discrete programmable I/O or Timer/Counter 2 input
4	SCL/SO-SI		I/O	I ² C clock output (open drain, need pull up) or SPI data
5	SDA/CS0		I/O	I ² C data (open drain, need pull up) or SPI Chip Select 0
6	P1.3/SYNC/SCK		I/O	Discrete programmable I/O or SYNC output or SPI clock output, needs to be pulled up to VDD1 in order to boot from I ² C EEPROM
7	P1.4/CAP		I/O	Discrete programmable I/O or Capture timer input
8	VDD1		P	3.3V digital power
9	VSS		P	Digital common
10	VDDCAP		P	Internal 1.8V output, Capacitor(s) to be connected
11	P2.0/NMI		I/O	Discrete programmable I/O or Non-maskable Interrupt input
12	P3.2/INT0		I/O	Discrete programmable I/O or Interrupt 0 input
13	P2.7/AOPWM1		I/O	Discrete programmable I/O or PWM 1 digital output
14	AIN0		I	Analog input channel 0, 0-1.2V range, needs to be pulled down to AVSS if unused
15	AIN1		I	Analog input channel 1, 0-1.2V range, needs to be pulled down to AVSS if unused
16	AIN2		I	Analog input channel 2, 0-1.2V range, needs to be pulled down to AVSS if unused
17	AIN3		I	Analog input channel 3, 0-1.2V range, needs to be pulled down to AVSS if unused
18	AIN4		I	Analog input channel 4, 0-1.2V range, needs to be pulled down to AVSS if unused
19	IFB-		I	Single shunt current sensing OP amp input (-)
20	IFB+		I	Single shunt current sensing OP amp input (+)
21	IFBO		O	Single shunt current sensing OP amp output
22	CMEXT		O	Unbuffered 0.6V output. Capacitor needs to be connected.
23	AREF		O	Analog reference voltage output (0.6V)
24	AIN5-		I	Analog input channel 5, 0-1.2V range, needs to be pulled down to AVSS if unused
25	AIN5+		I	Analog input channel 5, 0-1.2V range, needs to be pulled down to AVSS if unused
26	AIN5O		O	Analog output 5, 0-1.2V range,
27	AVSS		P	Analog common

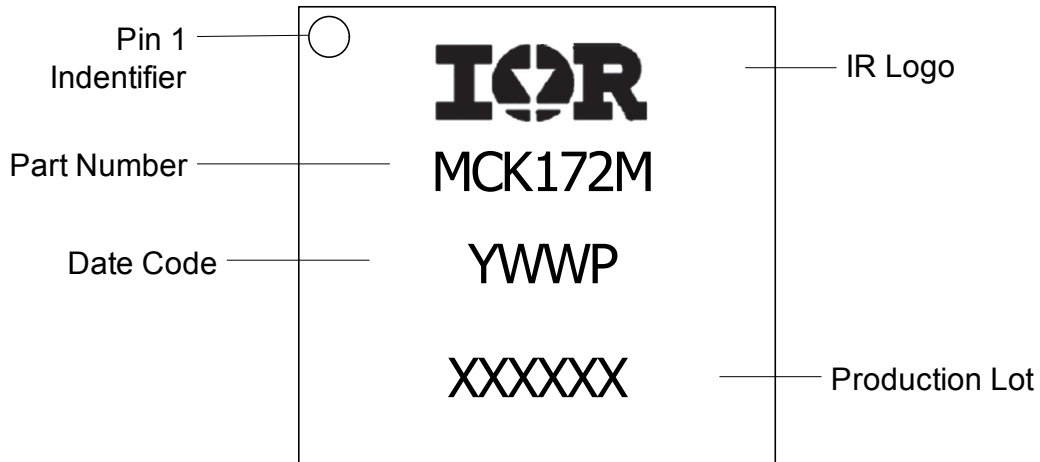
Pin Number	Pin Name	Internal Pull-up /Pull-down	Pin Type	Description
28	VDDCAP		P	Internal 1.8V output, Capacitor(s) to be connected
29	VDD1		P	3.3V digital power
30	VSS		P	Digital common
31	P3.1/AOPWM2		I/O	Discrete programmable I/O or PWM 2 digital output
32	PWMWL	58 kΩ Pull down	O	PWM gate drive for phase W low side, configurable either high or low true.
33	PWMVL	58 kΩ Pull down	O	PWM gate drive for phase V low side, configurable either high or low true
34	PWMUL	58 kΩ Pull down	O	PWM gate drive for phase U low side, configurable either high or low true
35	PWMWH	58 kΩ Pull down	O	PWM gate drive for phase W high side, configurable either high or low true
36	PWMVH	58 kΩ Pull down	O	PWM gate drive for phase V high side, configurable either high or low true
37	PWMUH	58 kΩ Pull down	O	PWM gate drive for phase U high side, configurable either high or low true
38	P1.5/VPP		I/O P	OTP programming power (6.5V) or Discrete programmable I/O.
39	GATEKILL	70 kΩ Pull up	I	PWM shutdown input, 2-μsec digital filter, configurable either high or low true.
40	P3.0/INT2/CS1	70 kΩ Pull up	I/O	Discrete programmable I/O or external interrupt 2 input or SPI Chip Select 1
41	P5.2/TMS		I/O	JTAG test mode select or Discrete I/O
42	TDO		O	JTAG test data output
43	P5.1/TDI		I/O	JTAG test data input or Discrete I/O
44	TCK		I	JTAG test clock
45	RESET		I/O	Reset, low true, Schmitt trigger input
46	P1.1/RXD		I/O	UART receiver input or Discrete programmable I/O
47	P1.1/RXD		I/O	UART transmitter output or Discrete programmable I/O
48	P3.3/INT1		I/O	Interrupt 1 input or Discrete I/O

Table 22 Pin List

9 Package Dimensions



10 Part Marking Information



11 Qualification Information

Qualification Level		Industrial ^{††} (per JEDEC JESD47)
Moisture Sensitivity Level		MSL2 ^{†††} (per IPC/JEDEC J-STD-020)
ESD	Machine Model	Class B (per JEDEC standard JESD22-A115)
	Human Body Model	Class 2 (per ANSI/ESDA/JEDEC JS-001)
	Charged Device Model	Class C2 (per JEDEC standard JESD22-C101)
	Latch-Up	Class I, Level B (per JEDEC standard JESD78)
RoHS Compliant		Yes

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

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