FEATURES

- 3.3 W Into 4Ω from 5.5V power supply at THD+N = 10% (Typ.).
- 2.0 W Into 8Ω from 5.5V power supply at THD+N = 10% (Typ.).
- 2.5V~5.5V Power supply.
- Low shutdown current.
- Low quiescent current.
- Minimum external components.
- No output filter required for inductive loads.
- Output pin short-circuit protection and automatic recovery. (short to output pin, short to GND, short to VDD).
- Low noise during turn-on and turn-off transitions.
- Lead free and green package available. (RoHS Compliant)
- 8-pin DFN package.

GENERAL DESCRIPTION

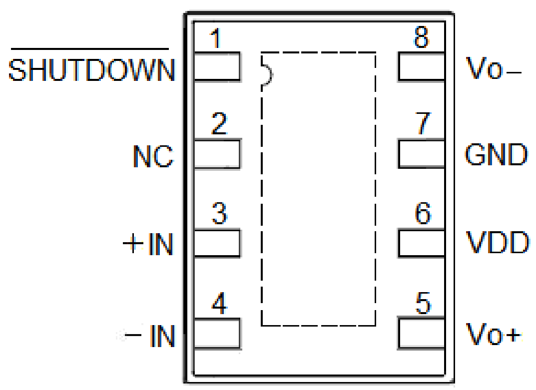
The LY8010 is a high efficiency, 3.3 W mono class D audio power amplifier. It is a low noise, filterless PWM architecture eliminates the output filter, reducing external component count, system cost, and simplify design.
The LY8010 is designed to meet of portable electronic devices. The LY8010 is a single 5.5V power supply, it is capable of driving 4Ω speaker load at a continuous average output of 3.3 W with 10% THD+N. Not external heat-sink is required.
In cellular handsets, the earpiece, speaker phone, and melody ringer can each be driven by the LY8010.The gain of the LY8010 is externally configurable which allows independent gain control from multiple sources by summing the signals.
Output short circuit and thermal overload protection prevent the device from damage during fault conditions.

APPLICATION

- Portable electronic devices
- Mobile Phones
- PDAs

PIN CONFIGURATION

LY8010 DFN8 pin configuration
(TOP VIEW)



PIN DESCRIPTION

SYMBOL	Pin No. DFN	DESCRIPTION
SHUTDOWN	1	Shutdown the device. (when **LOW** level is shutdown mode).
NC	2	No internal connection
AV_{DD}	--	Analog Power supply
+IN	3	Positive input
-IN	4	Negative input
Vo+	5	Positive BTL output
V_{DD}	6	Power supply
GND	7	Ground
Vo-	8	Negative BTL output

ORDERING INFORMATION

Ordering Code	Speaker Channels	Pin/ Package	Output Power (THD+N=10%)	Input Type	Output Type
LY8010BL	Mono	DFN8	3.3W/4Ω @5.5V_BTL 2.7W/4Ω @5.0V_BTL 2.0W/8Ω @5.5V_BTL 1.6W/8Ω @5.0V_BTL	SE/ DF	BTL

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APPLICATION CIRCUIT

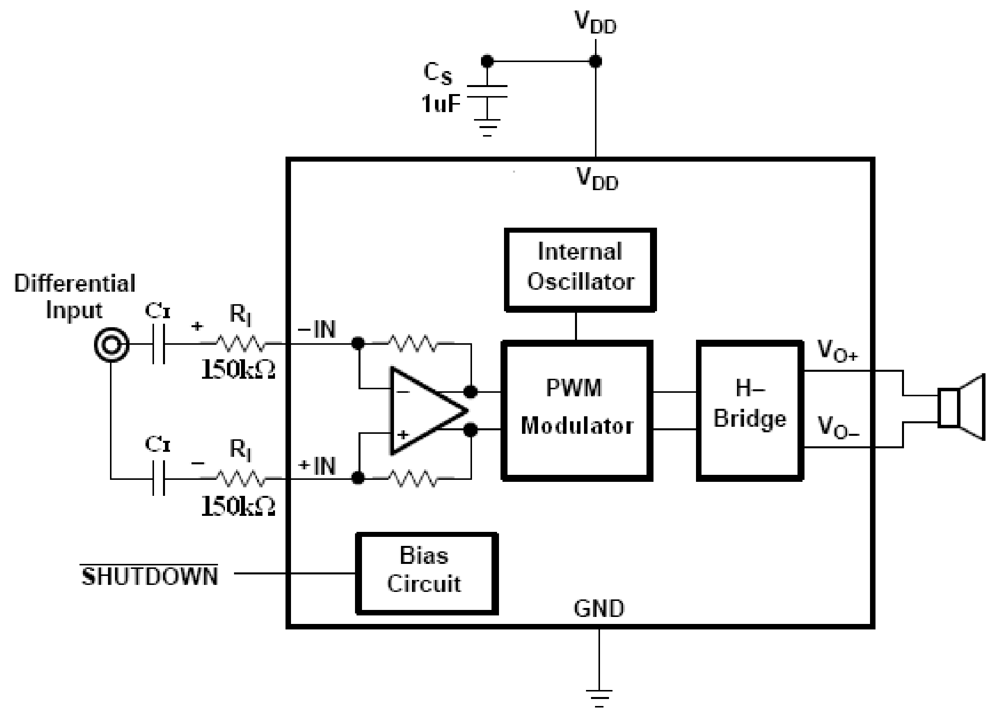

Figure 1. Application Schematic With Differential Input Configuration

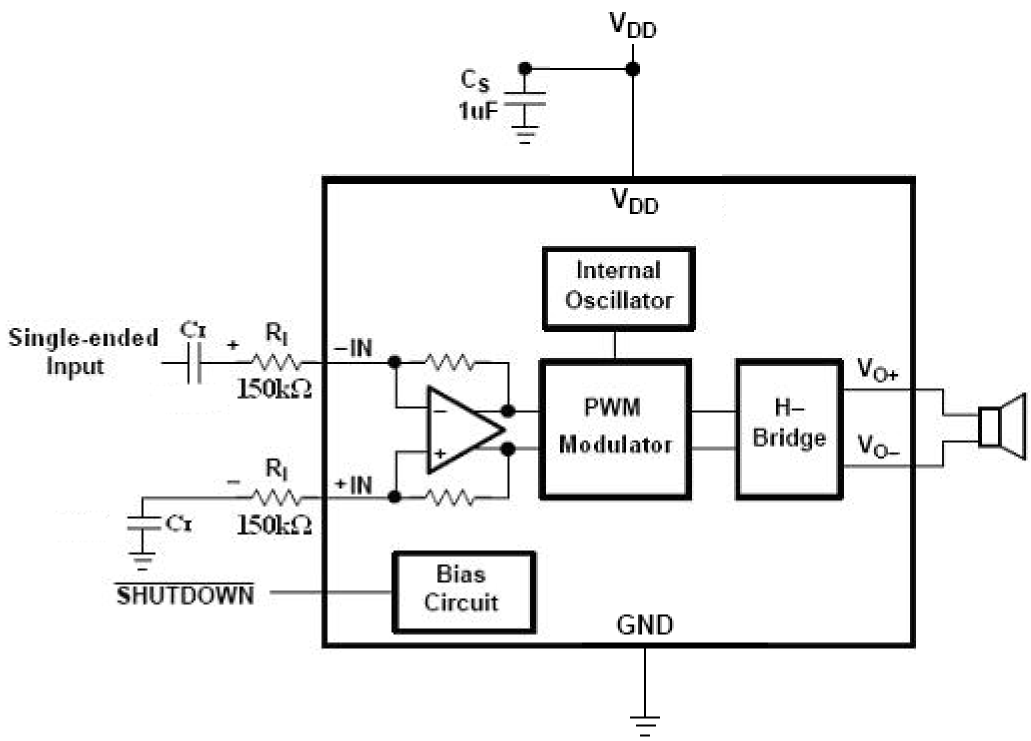

Figure 2. Application Schematic With Single-Ended Input Cofiguration

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ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	6.0	V
Operating Temperature	T_A	-40 to 85 (I grade)	℃
Input Voltage	V_I	-0.3V to V_{DD} +0.3V	V
Storage Temperature	T_{STG}	-65 to 150	℃
Power Dissipation	P_D	Internally Limited	W
ESD Susceptibility	V_{ESD}	2000	V
Junction Temperature	T_{JMAX}	150	℃
Soldering Temperature (under 10 sec)	T_{SOLDER}	260	℃

ELECTRICAL CHARACTERISTICS (TA = 25℃,Unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. *1	MAX.	UNIT
Supply voltage	V_{DD}		2.5	-	5.5	V
High-level input voltage	V_{IH}	$\overline{Shutdown}$	1.3	-	V_{DD}	V
Low-level input voltage	V_{IL}	$\overline{Shutdown}$	0	-	0.35	V
Output offset voltage (measured differentially)	$\lvert V_{OS} \rvert$	V_I = 0 V, Av = 2 V/V, V_{DD} = 2.5 V to 5.5 V	-	-	25	mV
Power supply rejection ratio	PSRR	V_{DD} = 5.0 V, R_L=4Ω, Inputs= GND, Av=2, Vpp=200mV, Cs=Delete. f=217Hz	-	-55	-	dB
Quiescent Current	I_Q	V_{DD} = 5.5V, No Load	-	3.5	-	mA
		V_{DD} = 3.6V, No Load	-	3.0	-	
		V_{DD} = 2.5V, No Load	-	2.5	-	
Shutdown Current	I_{SD}	$V_{SHUTDOWN}$ ≦0.5V, V_{DD} = 2.5V to 5.5V	-	0.1	2.0	μA
Total Gain (*)		V_{DD}= 2.5V to 5.5V R_L = 8Ω	[150KΩ / (5KΩ+Ri)] x2			V/V

(*1)Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at VCC = VCC(TYP.) and T_A = 25℃

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OPERATING CHARACTERISTICS (T_A = 25℃, Gain = 2V/V)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP. *1	MAX.	UNIT
Out Power	P_O	THD+N= 10%, f = 1 kHz, R_L= 4Ω	V_{DD}=5.5V	-	3.3	-	W
			V_{DD}=5.0V	-	2.75	-	
			V_{DD}=3.6V	-	1.4	-	
			V_{DD}=2.5V	-	0.6	-	
		THD+N= 1%, f = 1 kHz, R_L= 4Ω	V_{DD}=5.5V	-	2.6	-	
			V_{DD}=5.0V	-	2.15	-	
			V_{DD}=3.6V	-	1.1	-	
			V_{DD}=2.5V	-	0.1	-	
		THD+N= 10%, f = 1 kHz, R_L= 8Ω	V_{DD}=5.5V	-	2.0	-	
			V_{DD}=5.0V	-	1.6	-	
			V_{DD}=3.6V	-	0.8	-	
			V_{DD}=2.5V	-	0.4	-	
		THD+N= 1%, f = 1 kHz, R_L= 8Ω	V_{DD}=5.5V	-	1.6	-	
			V_{DD}=5.0V	-	1.3	-	
			V_{DD}=3.6V	-	0.7	-	
			V_{DD}=2.5V	-	0.1	-	
Signal-to-noise ratio	SNR	R_L = 4Ω, Input=GND, 1.0W=0dB	V_{DD}=5.0V	-	88	-	dB
Output voltage noise	Vn	Input=GND,R_L=4Ω,Av=2 f = 20 Hz to 20 kHz,	V_{DD}=5.0V	-	79	-	uV_{RMS}
Frequency	Fc	V_{DD} = 2.5V~5.5V		-	250	-	kHz
Start-up time from shutdown	Z_I	V_{DD} = 2.5V~5.5V		-	1	-	ms

(*1)Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at VCC = VCC(TYP.) and T_A = 25℃

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TYPICAL PERFORMANCE CHARACTERISTICS

Figure 3
Total Harmonic Distortion + Noise vs Output Power (4Ω)

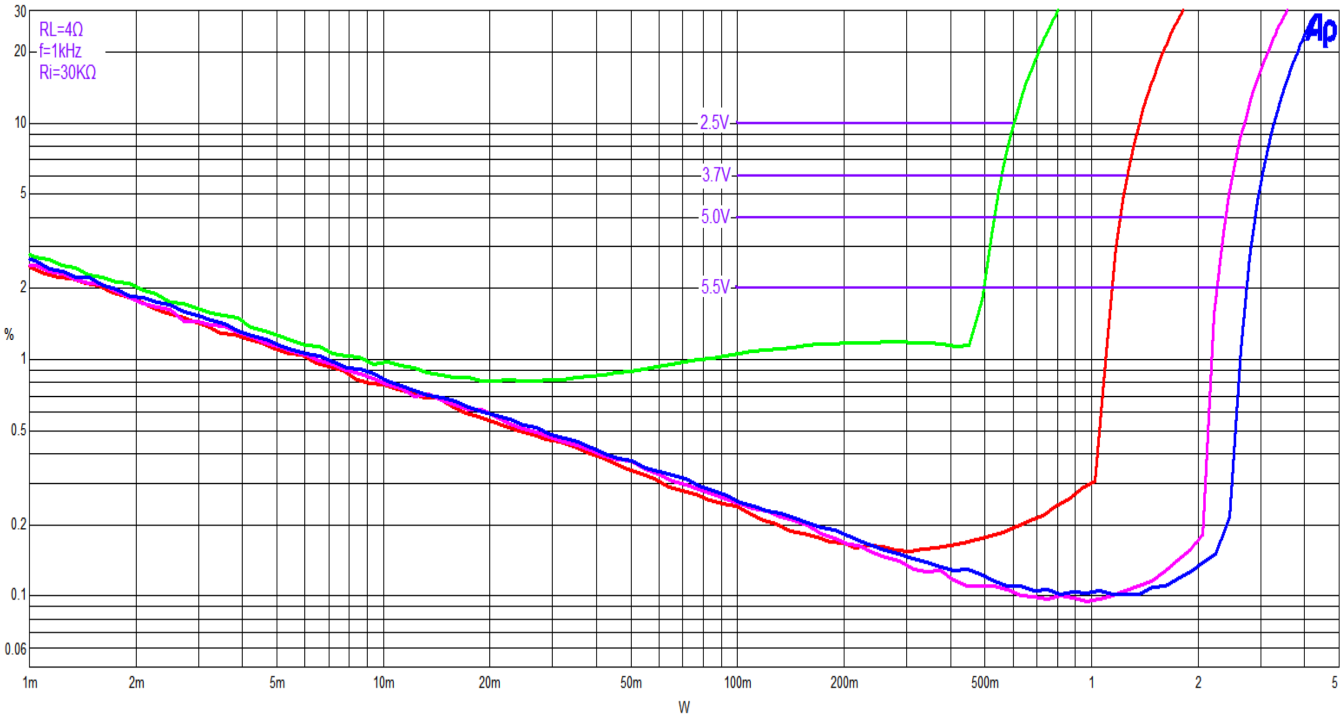


Figure 4
Total Harmonic Distortion + Noise vs Output Power (8Ω)

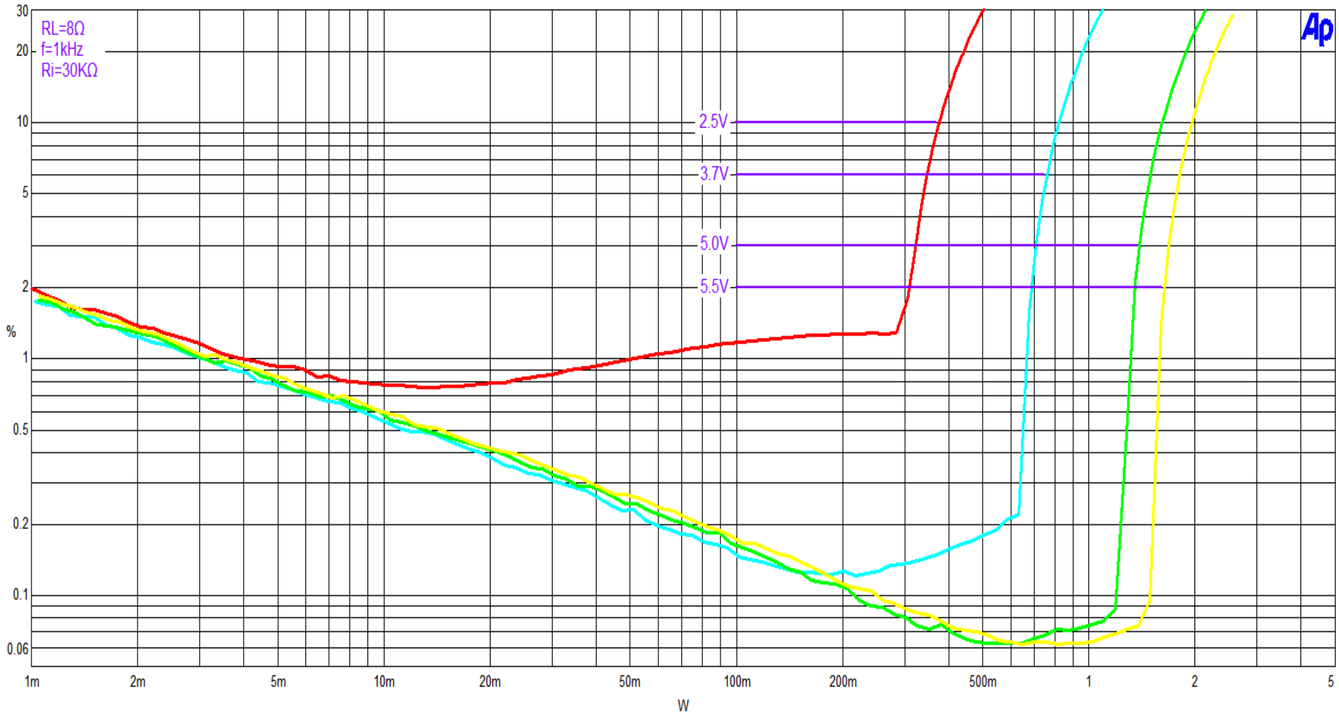


Figure 5
Noise Level

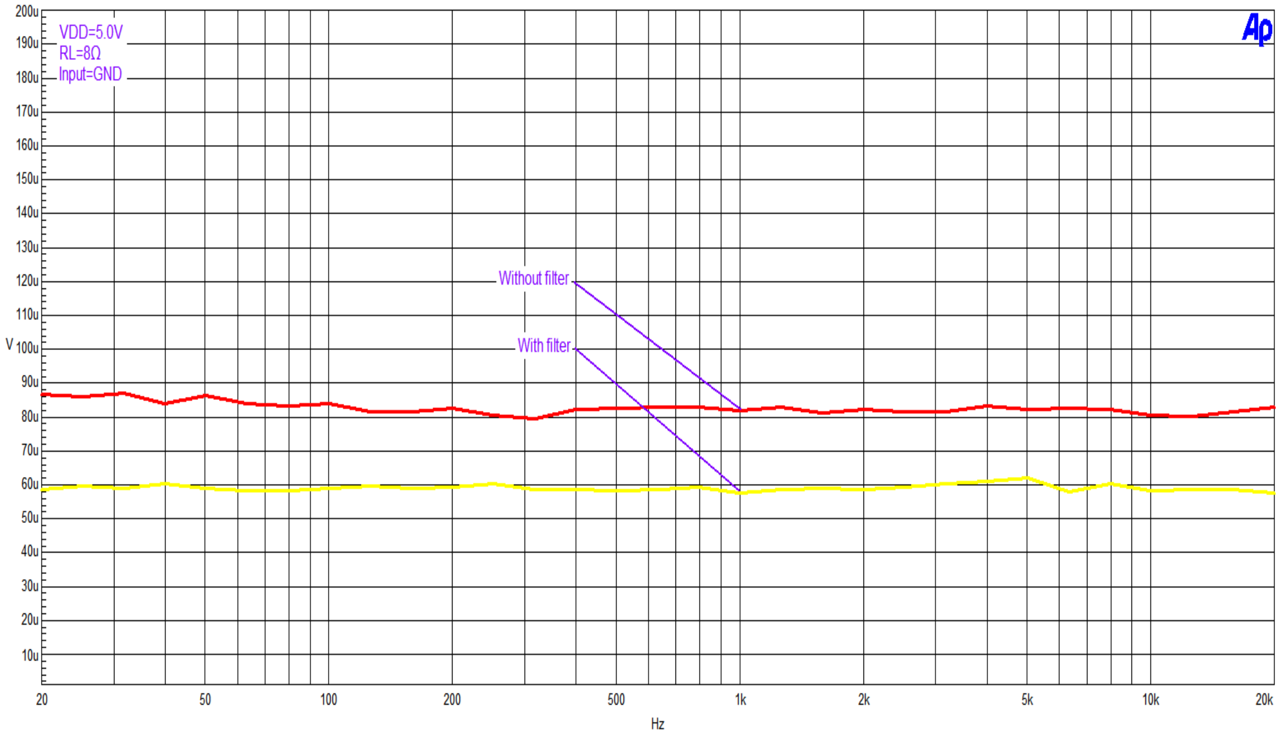
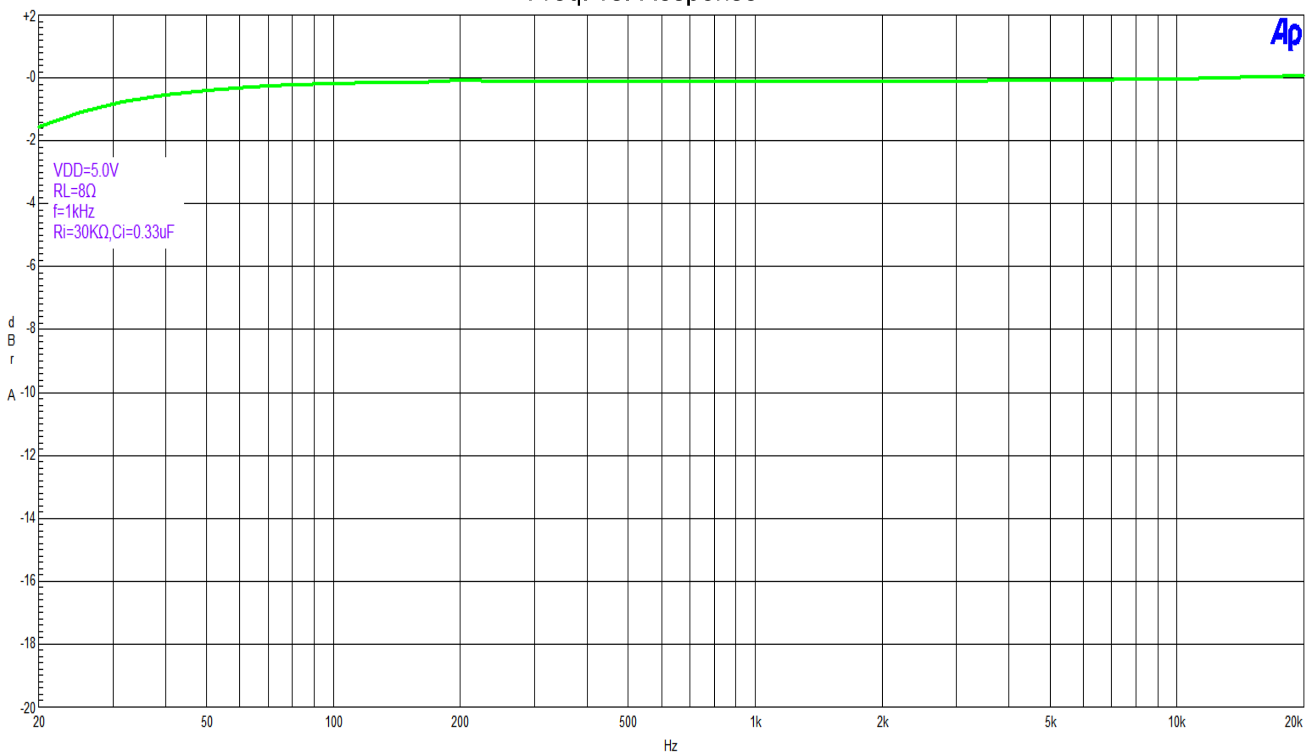
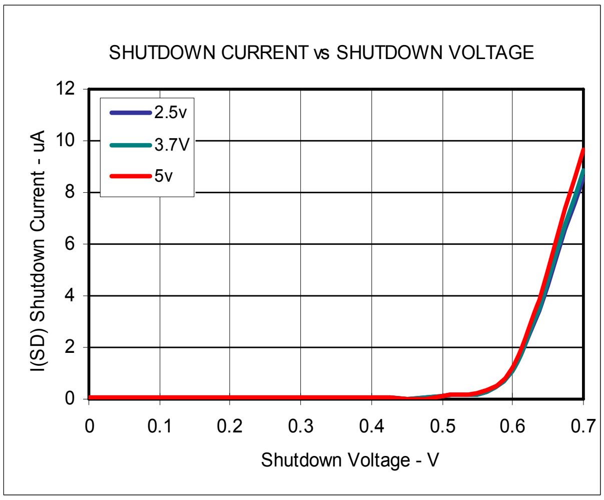


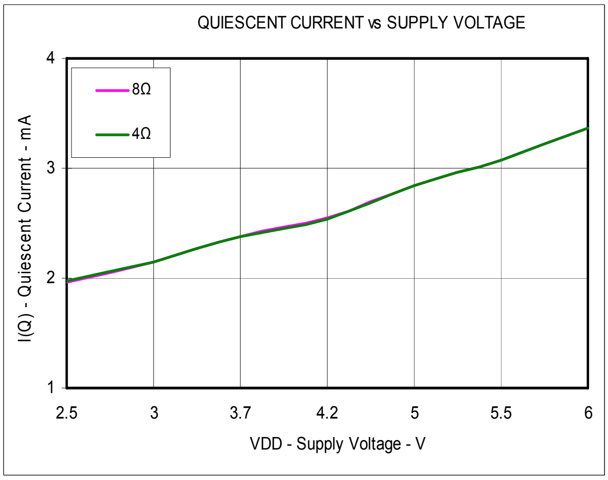
Figure 6
Freq. vs. Response



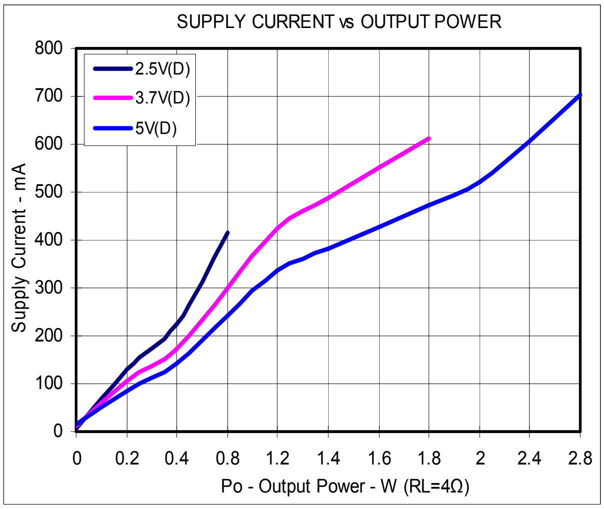
SD Current vs SD Voltage



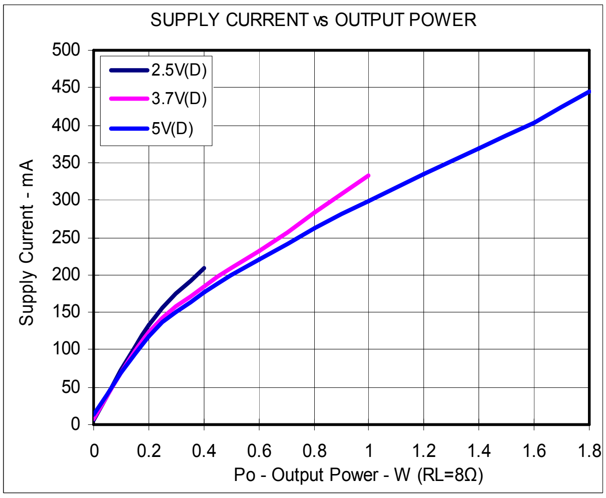
Quiescent vs Supply voltage



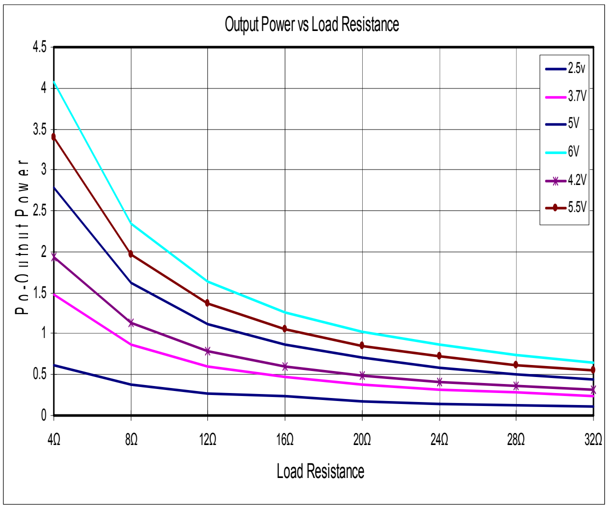
Supply Current vs Output Power (RL=4Ω)



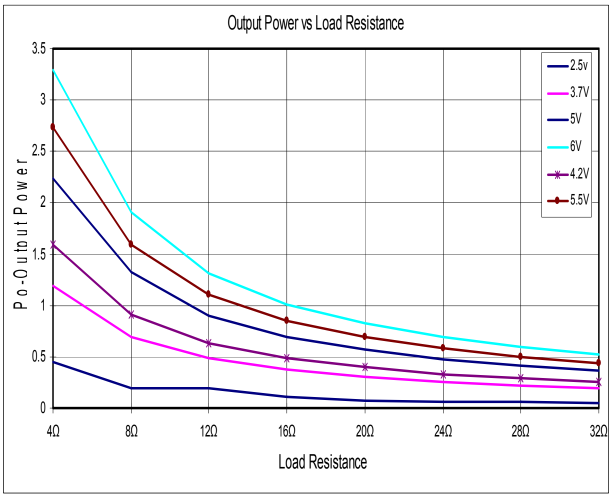
Supply Current vs Output Power (RL=8Ω)



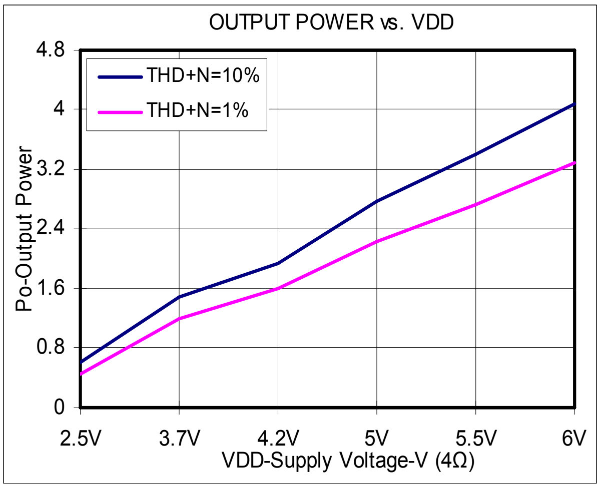
Load Resistance vs Output Power (THD+N=10%)



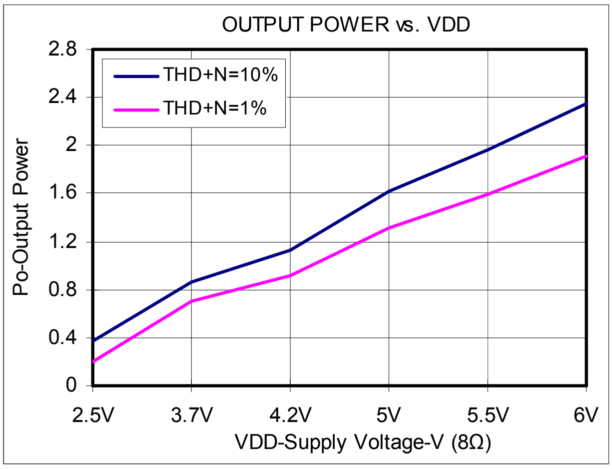
Load Resistance vs Output Power (THD+N=1%)



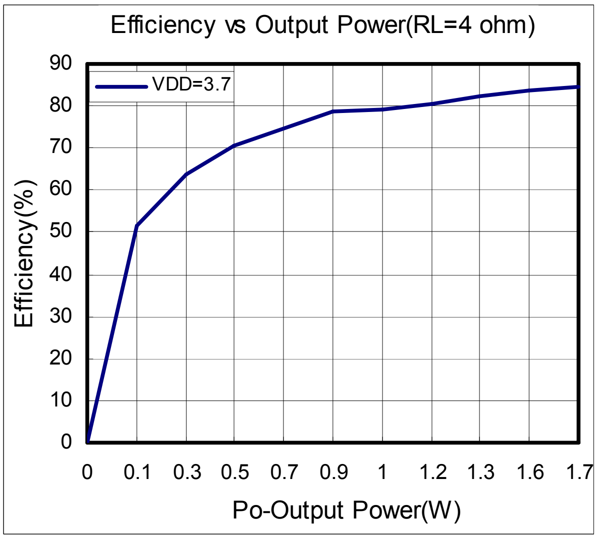
Output Power vs VDD (RL=4Ohm)



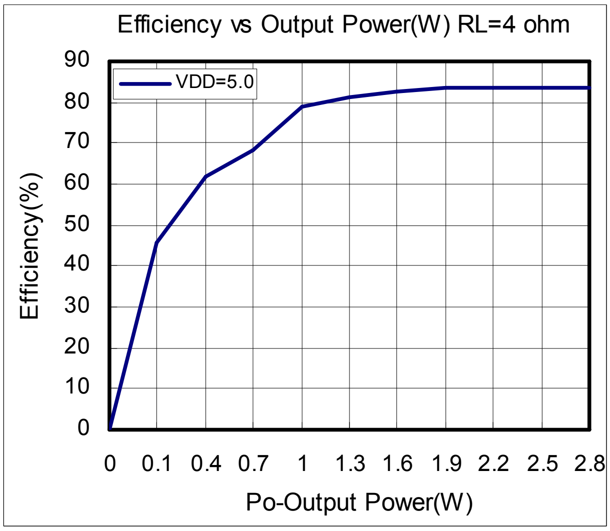
Output Power vs VDD (RL=8Ohm)



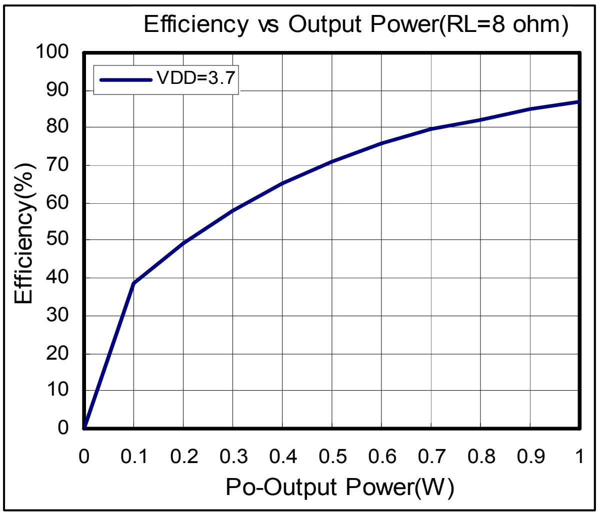
Efficiency and Output Power (4Ohm) 3.7V



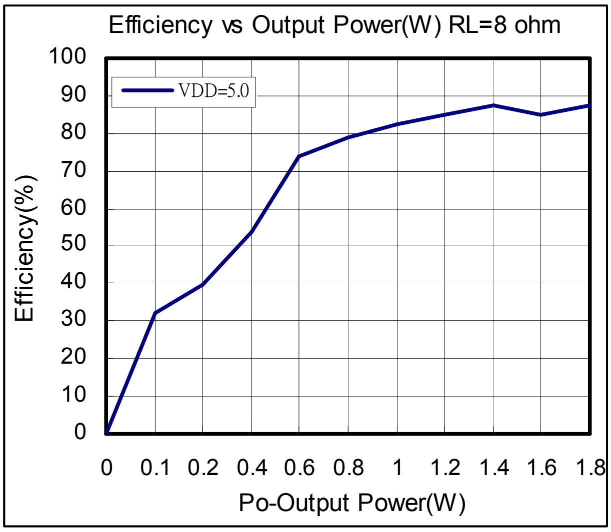
Efficiency and Output Power (4Ohm) 5.0V



Efficiency and Output Power (8Ohm) 3.7V



Efficiency and Output Power (8Ohm) 5.0V



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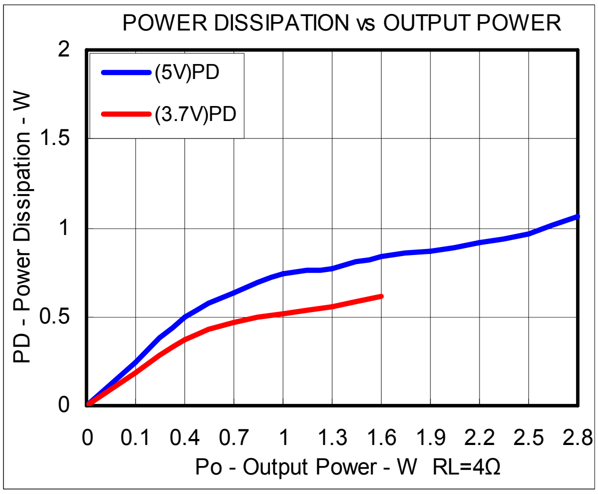
Dissipation vs Output Power (4Ohm)



Dissipation vs Output Power (8Ohm)

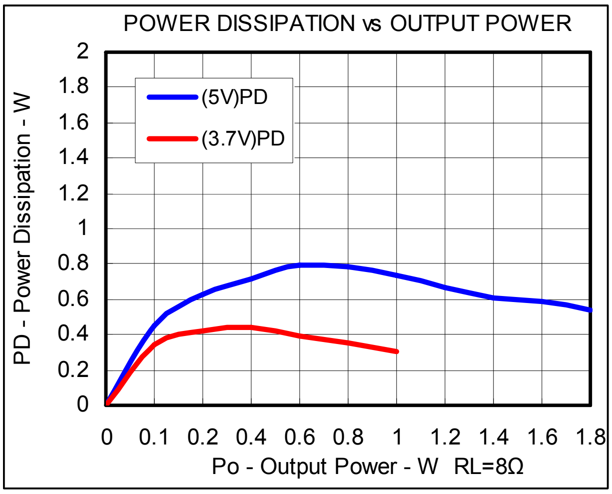


Figure 7
THD+N & Output Power vs Temperature (VDD=3V, RL=8Ω)

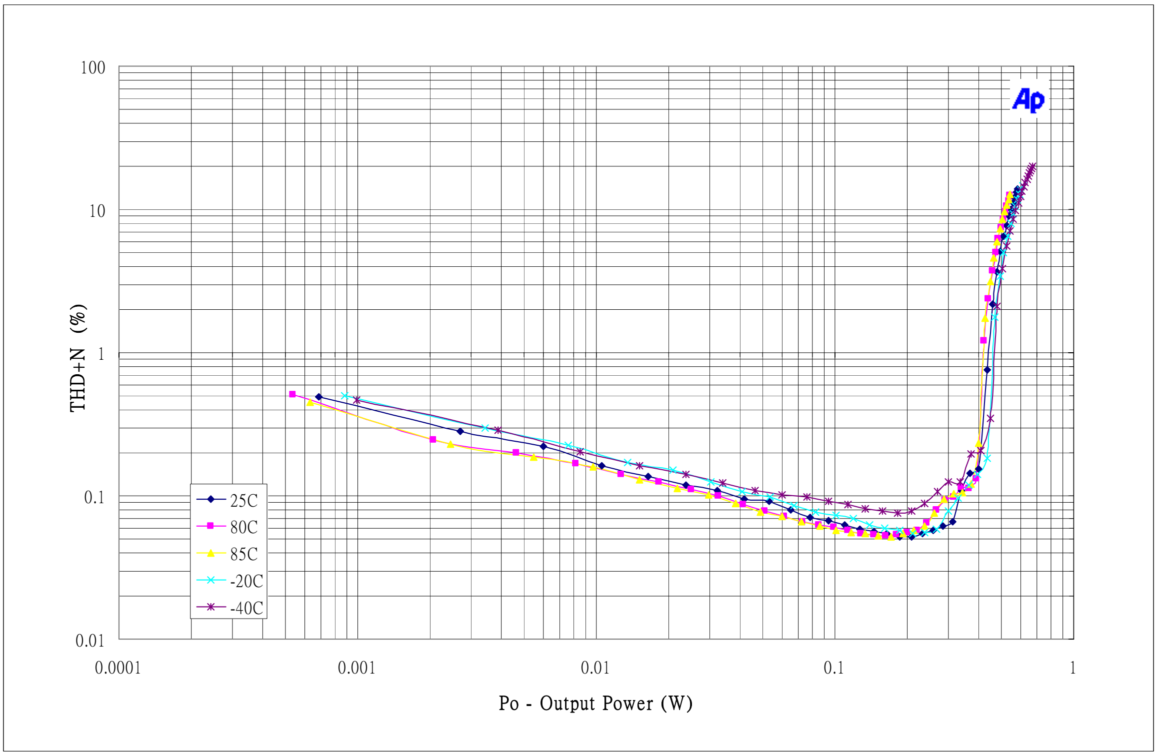


Figure 8
THD+N & Output Power vs Temperature (VDD=4.5V, RL=8Ω)

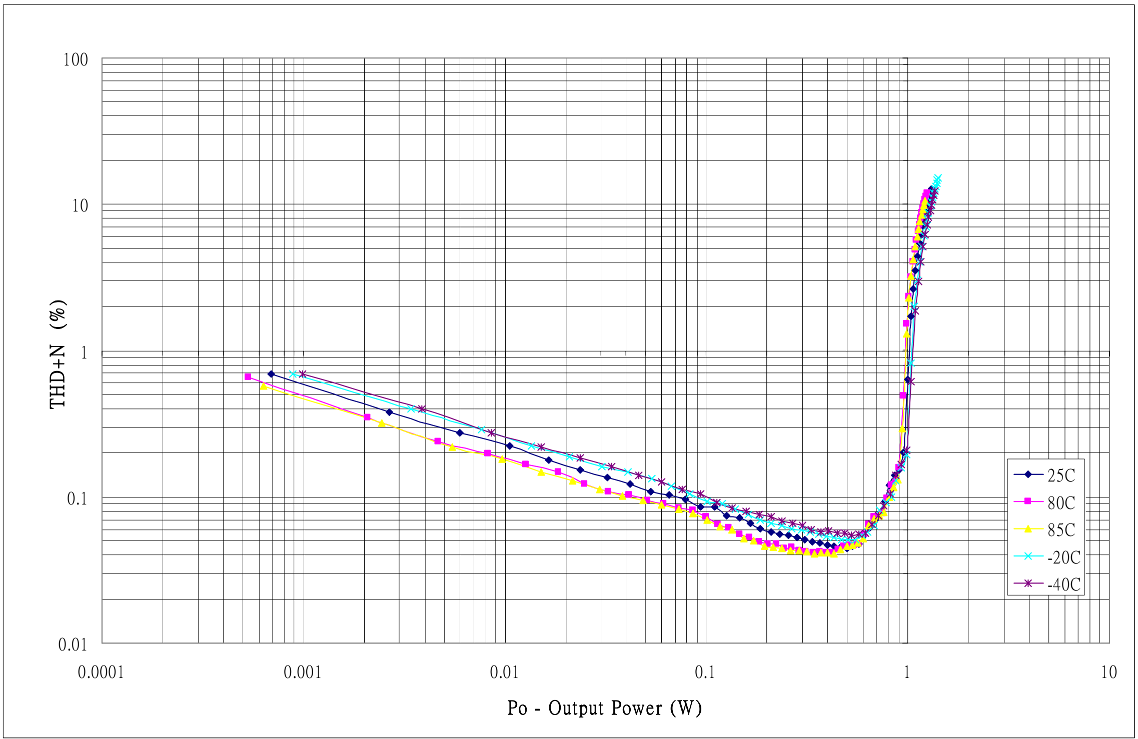


Figure 9
THD+N & Output Power vs Temperature (VDD=5.0V, RL=8Ω)

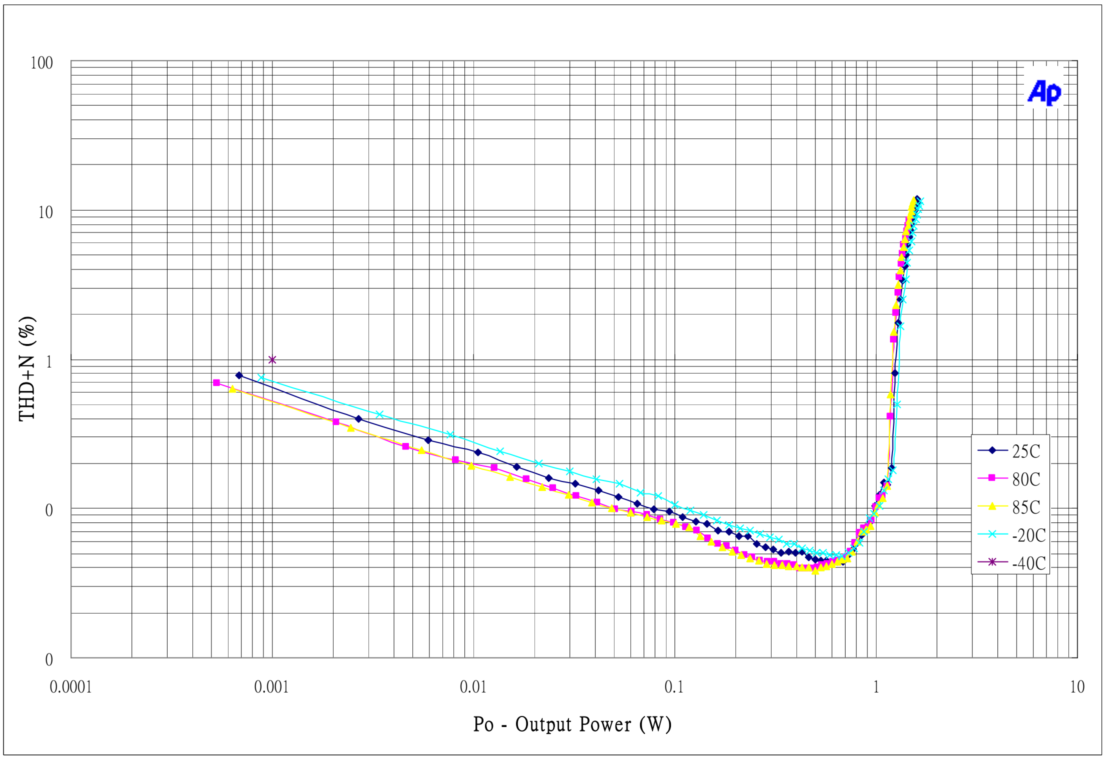


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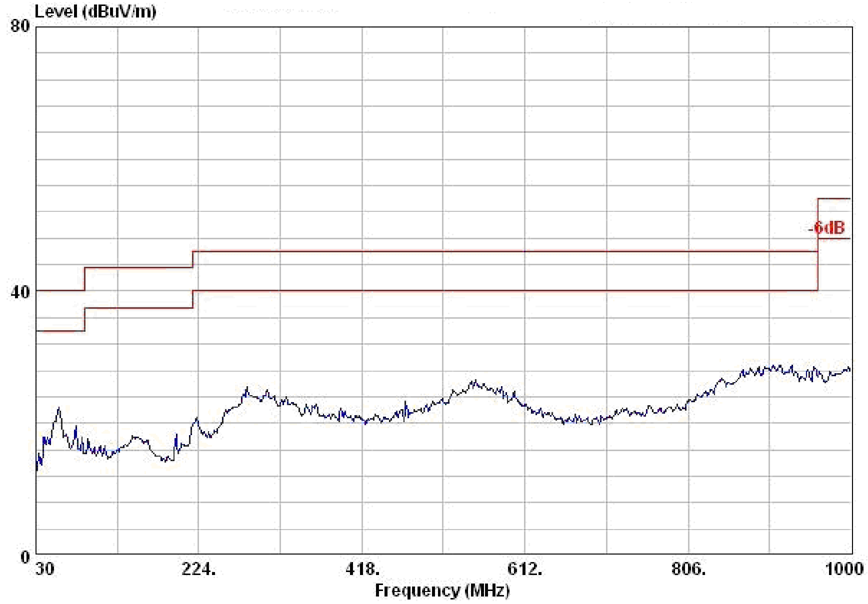
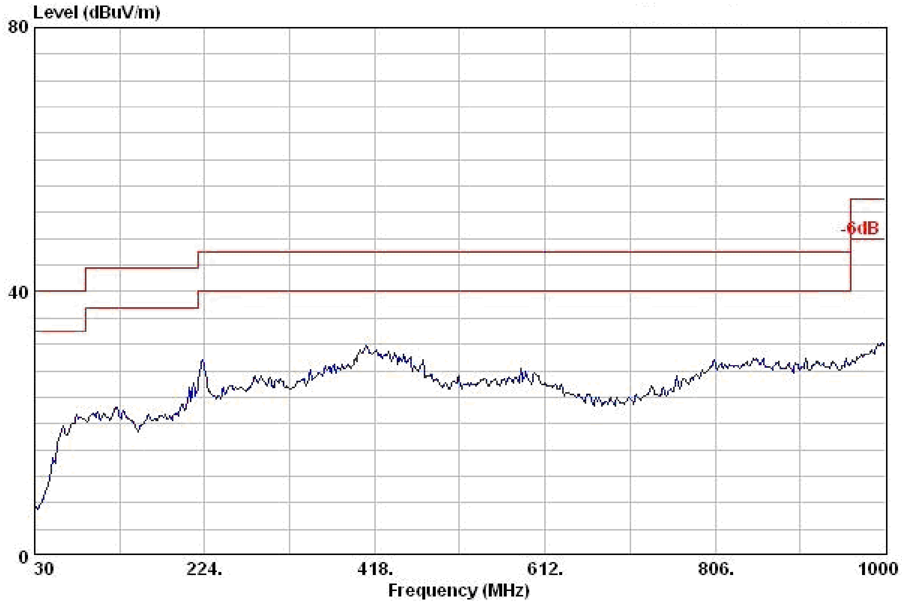
Figure 10
FCC Class-B (Vertical)



Trace: (Discrete)

Site	:	site
Condition	:	FCC CLASS-B 3m VERTICAL
EUT	:	LY8005
Voltage/Freq	:	DC/4.5V
Memo	:	GND+COPPER

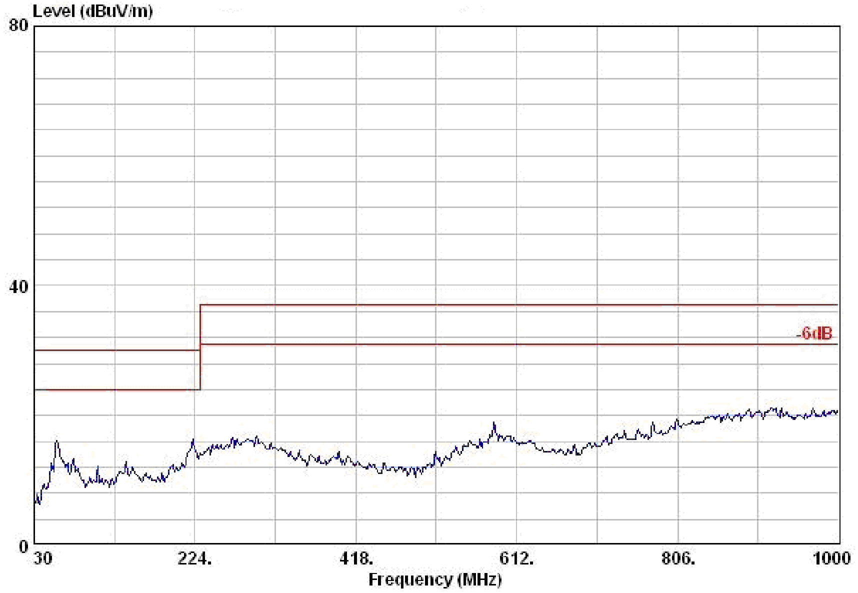
Figure 11
FCC Class-B (Horizontal)



Trace: (Discrete)

Site	:	site
Condition	:	FCC CLASS-B 3m HORIZONTAL
EUT	:	LY8005
Voltage/Freq	:	DC/4.5V
Memo	:	GND+COPPER

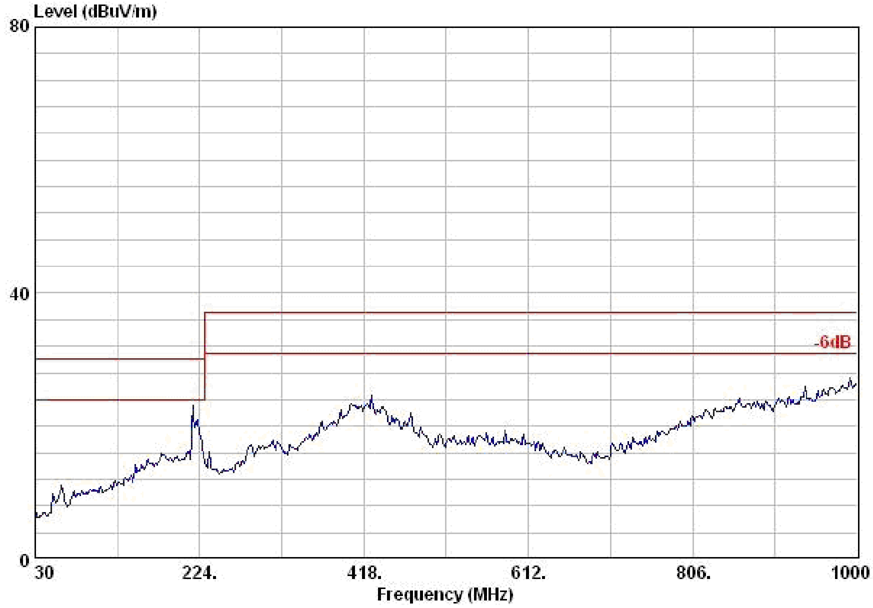
Figure 12
CISPR Class-B (Vertical)



Trace: (Discrete)

Site	:	site
Condition	:	CISPR CLASS-B 10m VERTICAL
EUT	:	LY8005
Voltage/Freq	:	DC/4.5V
Memo	:	GND+COPPER

Figure 13
CISPR Class-B (Horizontal)



Trace: (Discrete)

Site	:	site
Condition	:	CISPR CLASS-B 10m HORIZONTAL
EUT	:	LY8005
Voltage/Freq	:	DC/4.5V
Memo	:	GND+COPPER

APPLICATION INFORMATION

Fully Differential Amplifier

The LY8010 is a fully differential amplifier with differential inputs and outputs. The fully differential amplifier consists of a differential amplifier and a common-mode amplifier. The differential amplifier ensures that the amplifier outputs a differential voltage on the output that is equal to the differential input times the gain. The common-mode feedback ensures that the common-mode voltage at the output is biased around $V_{DD}/2$ regardless of the common-mode voltage at the input. The fully differential LY8010 can still be used with a single-ended input; however, the LY8010 should be used with differential inputs when in a noisy environment, like a wireless handset, to ensure maximum noise rejection.

Advantages of Fully Differential Amplifiers

Input-coupling capacitors not required:
The fully differential amplifier allows the inputs to be biased at voltage other than mid-supply. For example, if a codec has a midsupply lower than the midsupply of the LY8010, the common-mode feedback circuit will adjust, and the LY8010 outputs will still be biased at midsupply of the LY8010. The inputs of the LY8010 can be biased from 0.5 V to V_{DD} - 0.8 V. If the inputs are biased outside of that range, input - coupling capacitors are required.

Midsupply bypass capacitor, $C_{(BYPASS)}$, not required:
The fully differential amplifier does not require a bypass capacitor. This is because any shift in the midsupply affects both positive and negative channels equally and cancels at the differential output.

Better RF-immunity:
GSM handsets save power by turning on and shutting off the RF transmitter at a rate of 217 Hz. The transmitted signal is picked-up on input and output traces. The fully differential amplifier cancels the signal much better than the typical audio amplifier.

Component Selection

Figure 1 shows the LY8010 typical schematic with differential inputs and Figure 2 shows the LY8010 with single-ended inputs.
Differential inputs should be used whenever possible because the single-ended inputs are much more susceptible to noise.

Table 1. Typical Component Values

Reference	Description	Note
Ri	150KΩ	1% tolerance resistors
Cs	1.0uF	+22%,-80%
Ci	3.3 nF	(±10%)

(1) Ci is only needed for single-ended input or if V_{ICM} is not between 0.5 V and VDD - 0.8 V. C_I = 3.3 nF (with Ri = 150KΩ) gives a high-pass corner frequency of 321 Hz.

For example

$fc = 1 / (2\pi RiCi)$

$fc = 1 / (2\pi \times 150K\Omega \times 3.3nF) = 321.524$ Hz

Input Resistors (Ri)

The input resistors (R_I) set the gain of the amplifier according to equation Equation 1.

$$\text{Pre-Amplifier Gain} = \frac{150\ k\Omega}{Ri}$$

$$\text{Total Gain} = 2 \times \frac{150\ k\Omega}{Ri} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(1)$$

$$A_{VD} = 20 \times \log \left[2 \times \left(\frac{150\ k\Omega}{Ri}\right)\right]$$

Resistor matching is very important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistors. CMRR, PSRR, and cancellation of the second harmonic distortion diminish if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to keep the performance optimized. Matching is more important than overall tolerance.
Resistor arrays with 1% matching can be used with a tolerance greater than 1%.
Place the input resistors very close to the LY8010 to limit noise injection on the high-impedance nodes.
For optimal performance the gain should be set to 2 V/V or lower. Lower gain allows the LY8010 to operate at its best, and keeps a high voltage at the input making the inputs less susceptible to noise.

For example

Table 2. Typical Total Gain and A_{VD} Values

Rf (KΩ)	150	150	150	150	150	150
Ri (KΩ)	150	75	50	37.5	25	18.75
Pre AMP. Gain	1	2	3	4	6	8
Total Gain	2	4	6	8	12	16
A_{VD} (db)	6.02	12.04	15.56	18.06	21.58	24.08

Decoupling Capacitor (CS)

The LY8010 is a high-performance class-D audio amplifier that requires adequate power supply decoupling to ensure the efficiency is high and total harmonic distortion (THD) is low. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1 µF, placed as close as possible to the device V_{DD} lead works best. Placing this decoupling capacitor close to the LY8010 is very important for the efficiency of the class-D amplifier, because any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency. For filtering lower-frequency noise signals, a 10 µF or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

Input Capacitors (Ci)

The LY8010 does not require input coupling capacitors if the design uses a differential source that is biased from 0.5 V to V_{DD} - 0.8 V (shown in Figure 1). If the input signal is not biased within the recommended common-mode input range, if needing to use the input as a high pass filter (shown in Figure 1), or if using a single-ended source (shown in Figure 2), input coupling capacitors are required.
The input capacitors and input resistors form a high-pass filter with the corner frequency, f_c, determined in equation Equation 2.

$$f_c = \frac{1}{2\pi R_i C_i} \qquad (2)$$

The value of the input capacitor is important to consider as it directly affects the bass (low frequency) performance of the circuit. Speakers in wireless phones cannot usually respond well to low frequencies, so the corner frequency can be set to block low frequencies in this application.
Equation Equation 3 is reconfigured to solve for the input coupling capacitance.

$$C_i = \frac{1}{2\pi R_i f_c} \qquad (3)$$

For example

In the table 3 shows the external components. Rin in connect with Cin to create a high-pass filter.

Table 3. Typical Component Values

Reference	Description	Note
Ri	150KΩ	1% tolerance resistors
Ci	0.22uF	80%/–20%

Ci = 1 / (2πRifc)

Ci = 1 / (2π x150KΩ x4.8Hz)=0.221uF，Use 0.22uF

Summing Input Signals With The LY8010

Most wireless phones or PDAs need to sum signals at the audio power amplifier or just have two signal sources that need separate gain. The LY8010 makes it easy to sum signals or use separate signal sources with different gains. Many phones now use the same speaker for the earpiece and ringer, where the wireless phone would require a much lower gain for the phone earpiece than for the ringer. PDAs and phones that have stereo headphones require summing of the right and left channels to output the stereo signal to the mono speaker.

Summing Two Single-Ended Input Signals

Four resistors and three capacitors are needed for summing single-ended input signals. The gain and corner frequencies (f_{c1} and f_{c2}) for each input source can be set independently (see equations Equation 11 through Equation 14, and Figure 14). Resistor, R_P, and capacitor, C_P, are needed on the IN+ terminal to match the impedance on the IN- terminal. The single-ended inputs must be driven by low impedance sources even if one of the inputs is not outputting an ac signal.

$$\text{Gain 1} = \frac{V_O}{V_{I1}} = 2 \times \frac{150\ \text{k}\Omega}{R_{I1}} \quad (11)$$

$$\text{Gain 2} = \frac{V_O}{V_{I2}} = 2 \times \frac{150\text{k}\Omega}{R_{I2}} \quad (12)$$

$$C_{I1} = \frac{1}{2\pi R_{I1} f_{c1}} \quad (13)$$

$$C_{I2} = \frac{1}{2\pi R_{I2} f_{c2}} \quad (14)$$

$$C_P = C_{I1} + C_{I2} \quad (15)$$

$$R_P = \frac{R_{I1} \times R_{I2}}{R_{I1} + R_{I2}} \quad (16)$$

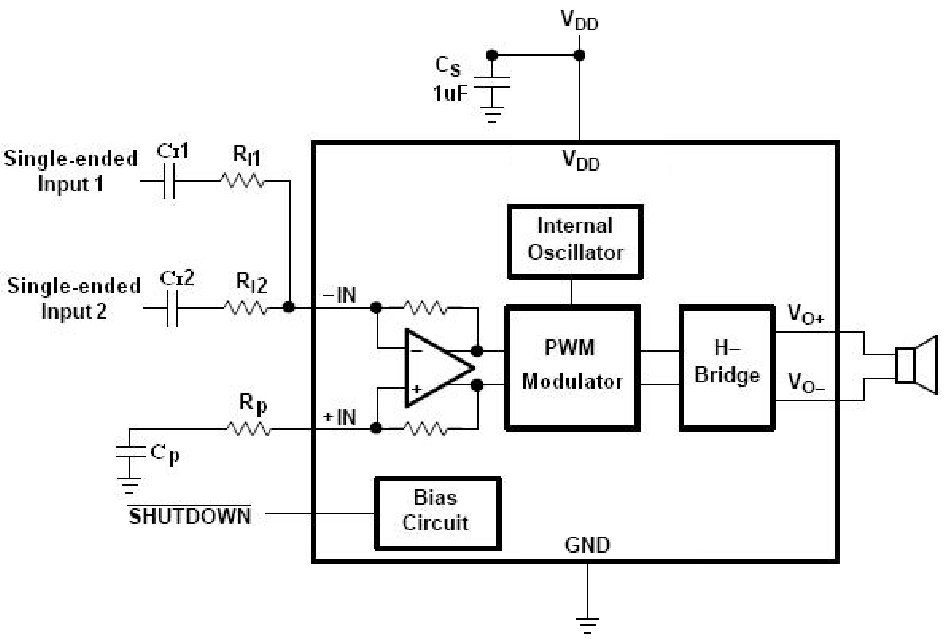


Figure 14. Application Schematic With LY8010 Summing Two Single-ended Input

PCB Layout

All the external components must place very close to the LY8010. The input resistors need to be very close to the LY8010 input pins so noise does not couple on the high impedance nodes between the input resistors and the input amplifier of the LY8010. Then place the decoupling capacitor Cs, close to the LY8010 is important for the efficiency of the class-D amplifier. Any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency.

Making the high current traces going to VDD, GND, V_{O+} and V_{O-} pins of the LY8010 should be as wide as possible to minimize trace resistance. If these traces are too thin, the LY8010's performance and output power will decrease. The input traces do not need to be wide, but do need to run side-by-side to enable common-mode noise cancellation.

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LY8010 Demo Board Artwork

Demo Board Application Circuit

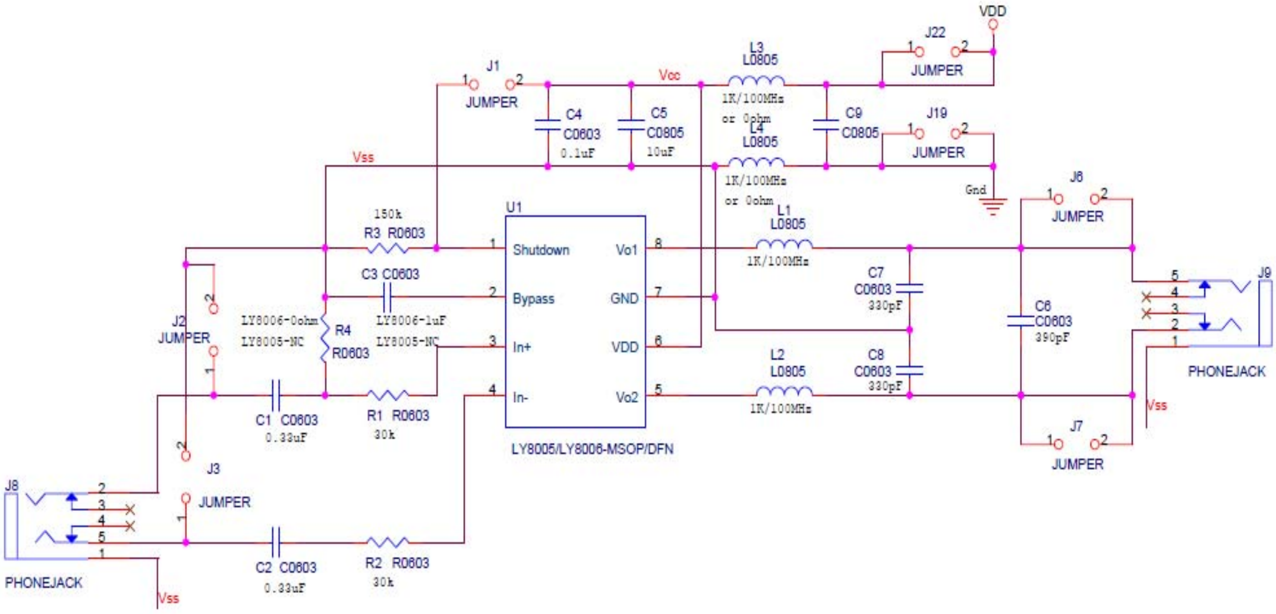

Figure 17. Demo Board Application Circuit

Demo Board BOM List

LY8010 V2.1 BOM List

No.	Description	Reference	Note
1	Resistor, 30KΩ	R1,R2	1/16W,1%
2	Resistor, 150KΩ	R3	1/16W,1%
3	Capacitor, 330pF(Option)	C7,C8	80%/−20%, nonpolarized
4	Capacitor, 390pF(Option)	C6	80%/−20%, nonpolarized
5	Capacitor, 0.1uF	C4	80%/−20%, nonpolarized
6	Capacitor, 0.33uF	C1,C2	80%/−20%, nonpolarized
7	Capacitor, 10.0uF	C5	80%/−20%, 6.3 V
8	Chip Bead 1KΩ/100MHz(Option)	L1,L2,L3,L4	1000Ω(1KΩ)±25%/100MHz
9	IC	U1	LY8010, DFN8
10	1*2 Pin Header	J1	J1, Open → shutdown Mode

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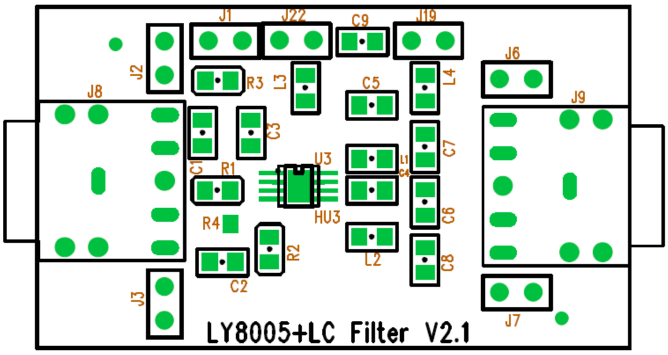
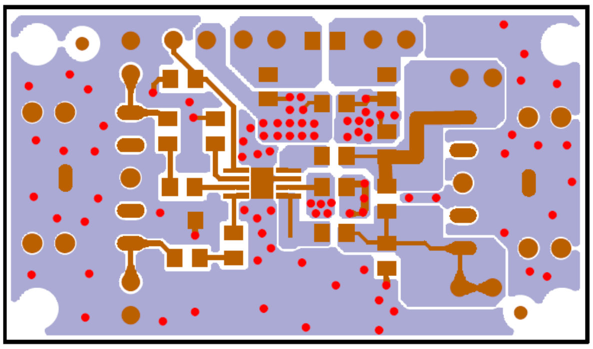
Demo Board Artwork

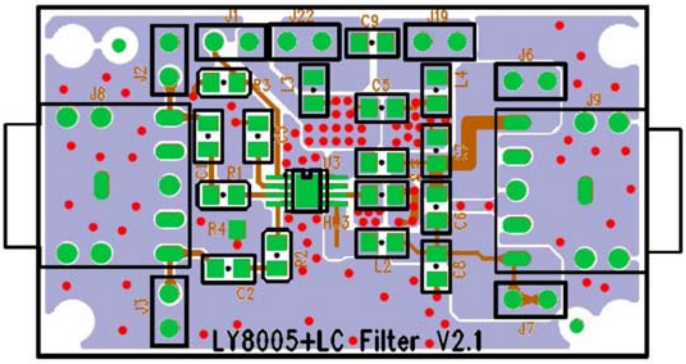
Top Silkscreen



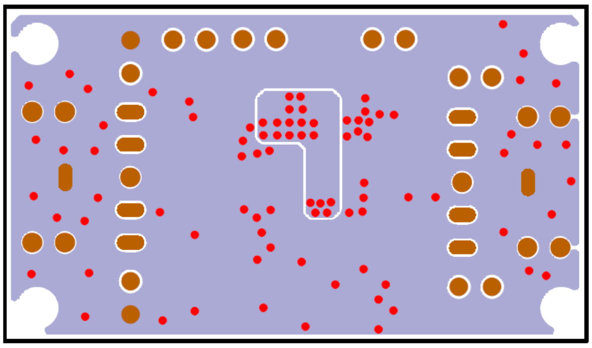
Top Layer



Composite view

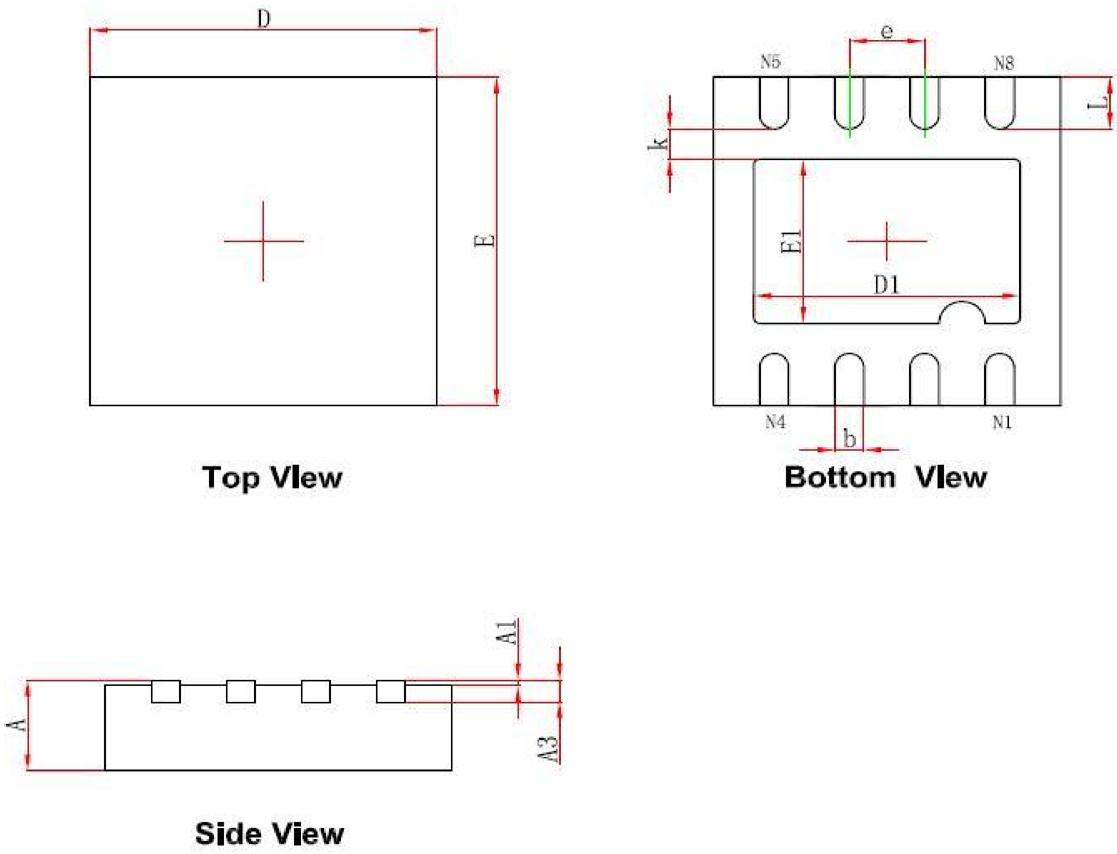


Bottom Layer



PACKAGE OUTLINE DIMENSION

8 Pin DFN Package Outline Dimension



Symbol	Dimensions In Millimeters	
	Min.	Max.
A	0.700/0.800	0.800/0.900
A1	0.000	0.050
A3	0.203REF.	
D	2.900	3.100
E	2.900	3.100
D1	2.200	2.400
E1	1.400	1.600
k	0.200MIN.	
b	0.180	0.300
e	0.650TYP.	
L	0.375	0.575

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