CONSOLIDATOR GA3227

Pre-configured DSP System for Hearing Aids

Description

The CONSOLIDATOR™ GA3227 hybrid is a DSP system based on a two−channel compression circuit. It can be configured as a single channel linear device or a single, or dual, channel WDRC device. It can efficiently replace traditional analog hearing aid compression circuits without compromising fundamental performance requirements.

The Consolidator GA3227 hybrid can be configured as an extended programmable circuit or a trimmer circuit supporting manual configuration. As a trimmer circuit, it continuously monitors trimmer positions and translates them into the hearing aid parameters of choice.

Also included in the Consolidator GA3227 is an in channel squelch circuit used to attenuate microphone and circuit noise in quiet environments, containing low distortion compression limiting, programmable high and low cut filters, and a fully accessible bi−quadratic filter.

The hybrid code programmed into the Consolidator GA3227 controller chip is '2'.

Features

- Efficient, High Fidelity 1 or 2−Channel WDRC Signal Processing
- Fully Programmable via Serial Data Interface
- One DLL Operation
- Four Trimmer Inputs plus Volume Control or Programmer Controlled
- Flexible Trimmer/Parameter Assignments
- Three−Terminal Trimmers
- Wideband Level Detection
- Choice of Two AGC−I Parametric Adjustment Strategies
- 6, 12 or 24 dB/Octave Band Split Filter or Configurable as Single−Channel Compressor
- In−Channel, Low−Level Squelch Control (1:2 Expansion)
- Output Compression Limiting (AGC−O)
- Flexible Pre− and Post−Emphasis Filters
- Three Independent Memories
- Pulse−Density−Modulated Output Stage Drives Zero−Bias 2−Terminal Receivers
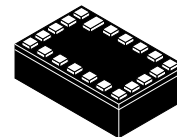- These Devices are Pb−Free and are RoHS Compliant

Standard Packaging

- Hybrid Typical Dimensions:
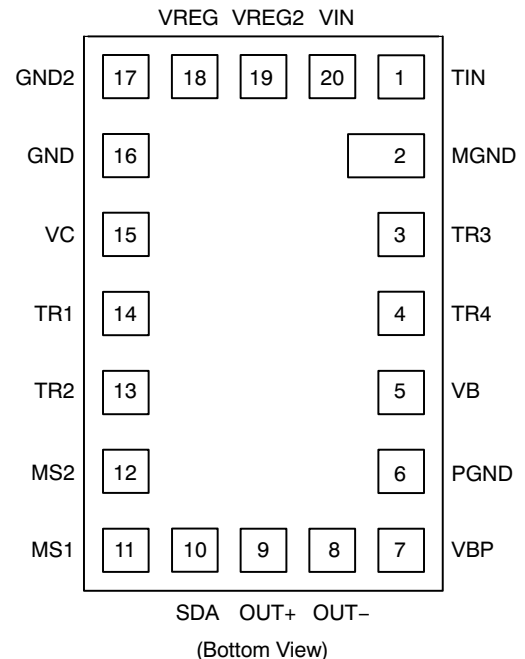 0.150 x 0.250 x 0.046 in.
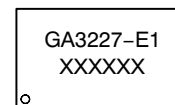 (3.81 x 6.35 x 1.17 mm)

ON Semiconductor®

http://onsemi.com

**20 PAD
HYBRID
CASE TBD**

PAD CONNECTION

VREG VREG2 VIN

GND2	17	18	19	20	1	TIN
GND	16				2	MGND
VC	15				3	TR3
TR1	14				4	TR4
TR2	13				5	VB
MS2	12				6	PGND
MS1	11	10	9	8	7	VBP

SDA OUT+ OUT−

(Bottom View)

MARKING DIAGRAM

GA3227−E1
XXXXXX
o

GA3227	= Specific Device Code
E1	= RoHS Compliant Hybrid
XXXXXX	= Work Order Number

ORDERING INFORMATION

CONSOLIDATOR GA3227

BLOCK DIAGRAM
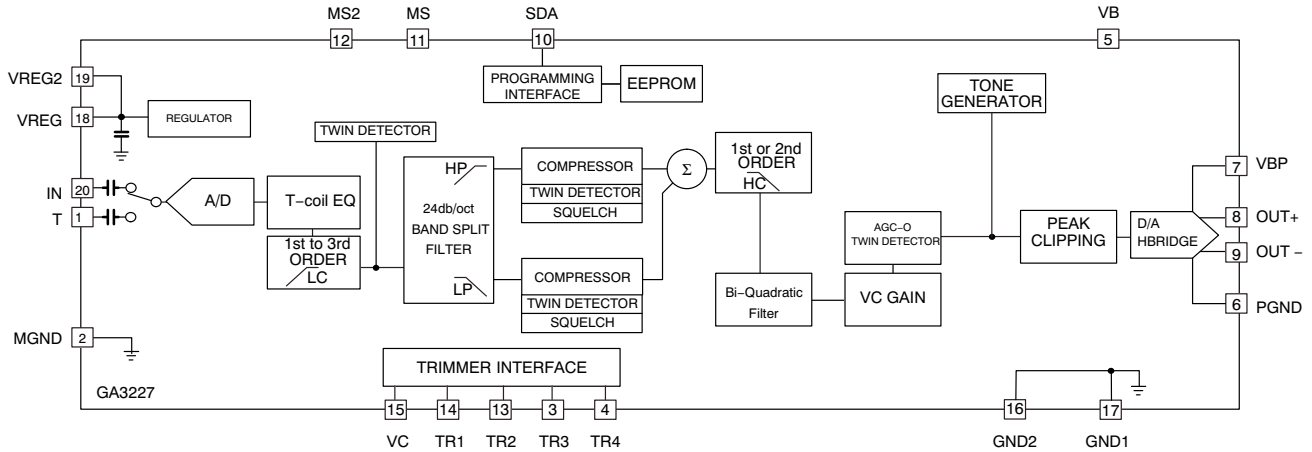
Figure 1. Consolidator GA3227 Hybrid Block Diagram

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Units
Operating Temperature Range	0 to +40	°C
Storage Temperature Range	−20 to +70	°C
Absolute Maximum Power Dissipation	25	mW
Input ESD Voltage	2000	V
Maximum Operating Supply Voltage	1.5	VDC
Absolute Maximum Supply Voltage	2	VDC

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

WARNING: Electrostatic Sensitive Device – Do not open packages or handle except at a static–free workstation.

WARNING: Moisture Sensitive Device – Non–RoHS Compliant – Level 3 MSL; RoHS Compliant – Level 4 MSL. Do not open packages except under controlled conditions.

Table 2. ELECTRICAL CHARACTERISTICS – PART 1

(Conditions: V_{BAT} = 1.25 V; Temperature = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Hybrid Current	I_{AMP}	–	–	550	–	μA
Minimum Operating Supply Voltage	V_{BOFF}	Ramp down	0.95	–	0.980	V
Supply Voltage Turn On Threshold	V_{BON}	Ramp up	1.065	1.10	1.160	V
Supply Voltage Hysteresis	–	$V_{BON} - V_{BOFF}$	–	150	–	mV
Low Battery Warning Voltage	–	Ramp down	1.06	1.10	1.14	V
Supply Voltage During Communication	V_{BC}	During Communication	1.20	1.30	–	V
EEPROM Burn Cycles	–	(Note 2)	100 k	–	–	cycles
Low Frequency System Bandwidth	–	–	–	130	–	Hz
High Frequency System Bandwidth	–	–	–	12	–	kHz
Total Maximum System Gain	A_V	V_{IN} = –95 dBV at 3 kHz; squelch disabled (Note 1)	82	83	84	dB
Converter Gain	A_{CONV}	A/D + D/A gain	28	29	30	dB
Total Harmonic Distortion	THD	V_{IN} = –40 dBV	–	–	1	%
THD at Maximum Input	THD_M	V_{IN} = –14 dBV, HRX – ON	–	–	3	%
Clock Frequency	f_{clk}	–	–	1.536	–	MHz

REGULATOR

Regulator Voltage	V_{REG}	–	0.87	0.90	0.93	V
Regulator Supply Rejection	$PSRR_{REG}$	–	–	36	–	dB

VOLUME CONTROL AND TRIMMERS

Volume Control or Trimmer Resistance	R_{VC}	Three–terminal Trimmer (Note 3)	0.1	–	1	MΩ
Volume Control Range	ΔA	–	–	48	–	dB

MS AND MS2 INPUT

Pull Down / Up Resistance	–	–	–	1	–	MΩ
Logic 1 Voltage	–	–	–	V_{REG}	–	V
Logic 0 Voltage	–	–	–	0	–	V

INPUT

Input Referred Noise	IRN	Bandwidth 100 Hz – 8 kHz	–	–109	–106	dBV
Input Impedance	Z_{IN}	–	13.5	16	18.5	kΩ
Crosstalk	–	Between microphone and telecoil inputs	–	–60	–	dB
Maximum Input Level	–	–	–	–14	–	dBV
Input Dynamic Range	–	HRX – ON, Bandwidth 100 Hz – 8 kHz	–	95	–	dB

OUTPUT

Maximum RMS Output Voltage	–	0 dBFS f = 1 kHz	–	–1	–	dBV
D/A Dynamic Range	–	Bandwidth 100 Hz – 8 kHz	–	83	–	dB
Output Impedance	Z_{OUT}	–	–	10	20	Ω

1. Total System Gain consists of: Wideband System Gain + High and Low Independent Channel Gains + Converter Gain. Total System Gain is calibrated during Cal/Config process.
2. Sample tested.
3. Volume control is log taper, trimmers are linear taper.

Table 2. ELECTRICAL CHARACTERISTICS – PART 1

(Conditions: V_{BAT} = 1.25 V; Temperature = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SDA INPUT						
Logic 0 Voltage	–	(Note 2)	0	–	0.3	V
Logic 1 Voltage	–	(Note 2)	1	–	1.3	V
SDA OUTPUT						
Synchronization Time (Synchronization Pulse Width)	T_{SYNC}	Baud = 0	237	250	263	μs
		Baud = 1	118	125	132	
		Baud = 2	59	62.5	66	
		Baud = 3	29.76	31.25	32.81	
		Baud = 4	14.88	15.63	16.41	
		Baud = 5	7.44	7.81	8.20	
		Baud = 6	3.72	3.91	4.10	
		Baud = 7	1.86	1.95	2.05	

1. Total System Gain consists of: Wideband System Gain + High and Low Independent Channel Gains + Converter Gain.
   Total System Gain is calibrated during Cal/Config process.
2. Sample tested.
3. Volume control is log taper, trimmers are linear taper.

Table 3. ELECTRICAL CHARACTERISTICS – PART 2

Parameter	Min	Max	Units	Accuracy
TELECOIL				
Telecoil Gain	−8	23	dB	Type 3
Low Pass Compensation Filter	0.5	1	kHz	Type 1
FREQUENCY SHAPING				
Crossover Frequency	0.5	4.25	kHz	Type 1, 2
High Cut Filter	1	12	kHz	Type 1, 2
High Cut Filter Order	6 or 12	–	dB/Octave	N/A
Low Cut Filter	0.01	3	kHz	Type 1, 2
Low Cut Filter Order	6, 12 or 18	6, 12 or 18	dB/Octave	–
INDEPENDENT CHANNEL PROCESSING				
Bandsplit Filter Slopes	6, 12 or 24	6, 12 or 24	dB/Octave	Type 1, 2
Low Level Gain	−18	42	dB	Type 3
High Level Gain	−18	42	dB	Type 3
Lower Threshold	30	80	dBSPL	Type 3
Upper Threshold	70	110	dBSPL	Type 3
Compression Ratio	1 : 1	3 : 1	Ratio	Type 3
Squelch Expansion Ratio	1 : 2	1 : 2	Ratio	N/A
Squelch Threshold	20	60	dBSPL	Type 3
Squelch Attack Time Constant	0.25	8192	ms	Type 1, 3
Squelch Release Time Constant	0.25	8192	ms	Type 1, 3
WIDEBAND SYSTEM GAIN				
Wideband System Gain	−36	12	dB	Type 3
Wideband Attack Time Constant (Fast & Slow)	0.25	8192	ms	Type 1, 3

Table 3. ELECTRICAL CHARACTERISTICS – PART 2

Parameter	Min	Max	Units	Accuracy
WIDEBAND SYSTEM GAIN				
Wideband Release Time Constant (Fast & Slow)	0.25	8192	ms	Type 1, 3
External VC	−48	0	dB	Type 3
Internal VC Attenuator	−48	0	dB	Type 3
TOTAL SYSTEM GAIN				
Total System Gain	−19	83	dB	(Note 1)
AGCo				
AGCo Output Limiting	−30	−1	dBFS*	Type 3
AGCo Compression Ratio	∞ : 1	∞ : 1	Ratio	N/A
PEAK CLIPPER				
PC Output Limiting	−40	0	dBFS	Type 3
TONE GENERATOR				
Pure Tone Frequency (memory and low battery indicator)	0.25	12	kHz	Type 1, 2
Pure Tone Amplitude (memory and low battery indicator)	−50	0	dBFS	Type 3

1. Total System Gain consists of: Wideband System Gain + High and Low Independent Channel Gains + Converter Gain and accuracy of this parameter is dependent on accuracy of the components.

*Peak output is defined as largest sine wave possible at the resonant frequency of the receiver.

NOTE: Type 1: Accuracy is determined by the clock frequency deviation

Type 2: Accuracy is determined by the quantization error of 16 bit coefficient and 20 bit or higher data word

Type 3: Accuracy is determined by the quantization error of a parameter word (see Table 2 for word length) and 20 bit or higher data word

TYPICAL APPLICATIONS
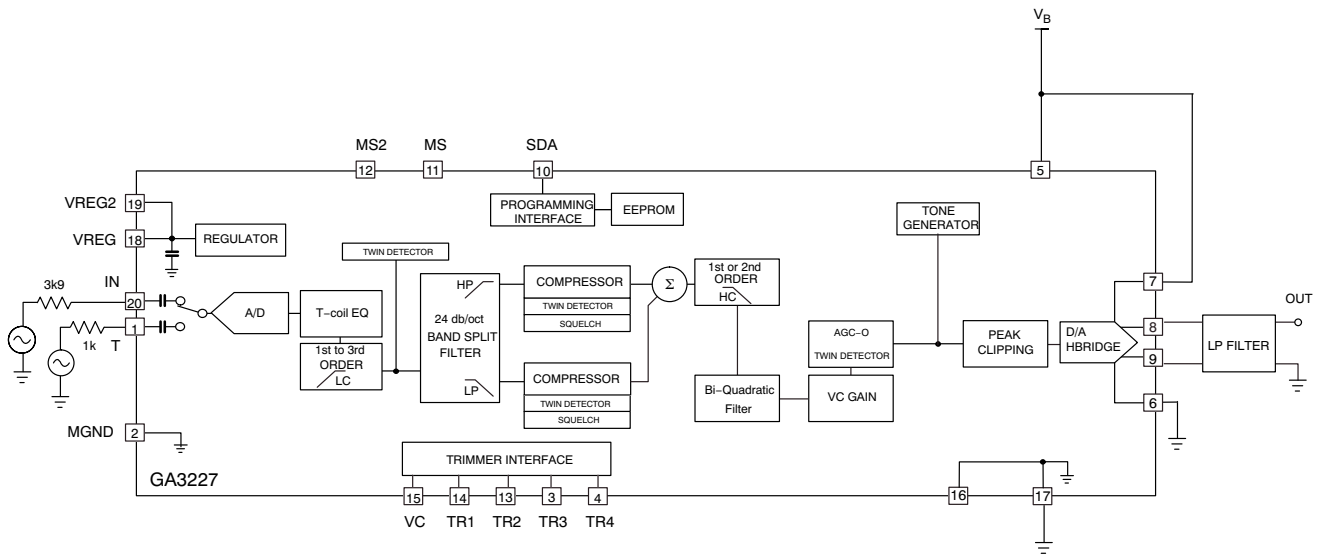
Note: All resistors in ohms and all capacitors in farads, unless otherwise stated.
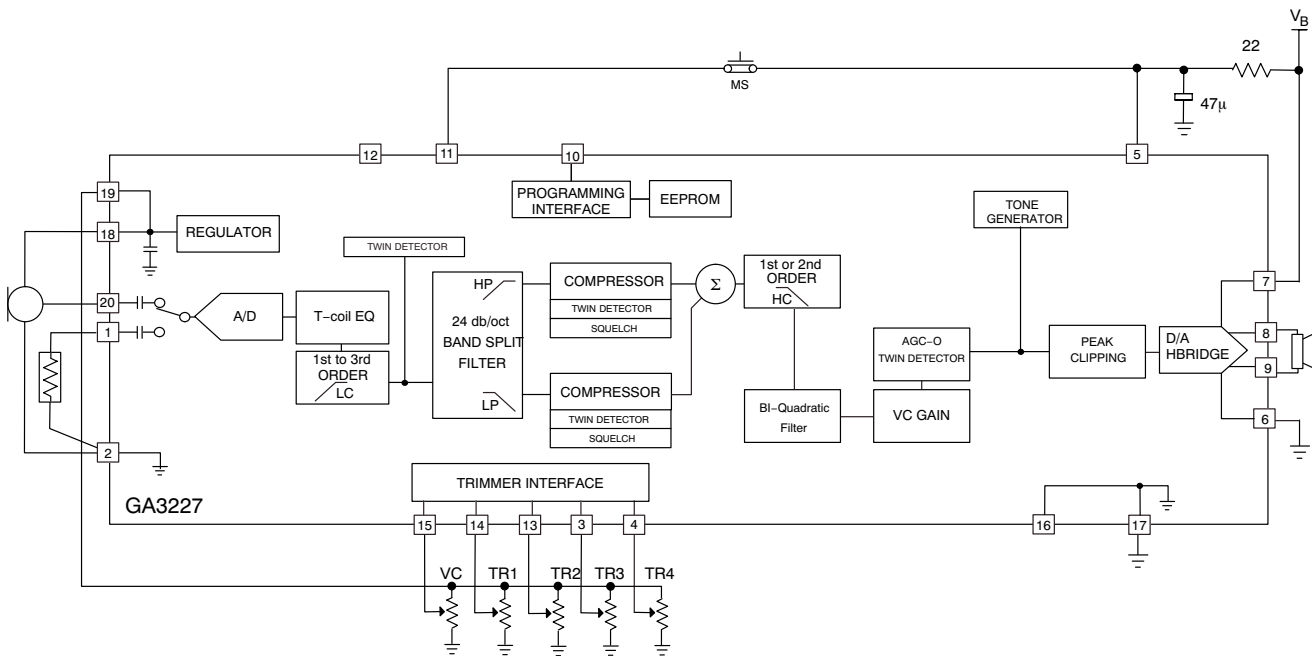
Figure 2. Test Circuit

TYPICAL APPLICATIONS (Cont'd)

Note: All resistors in ohms and all capacitors in farads, unless otherwise stated.

Figure 3. Example of Programmable Application Circuit

Note: All resistors in ohms and all capacitors in farads, unless otherwise stated.

Figure 4. Example of Trimmer Application Circuit
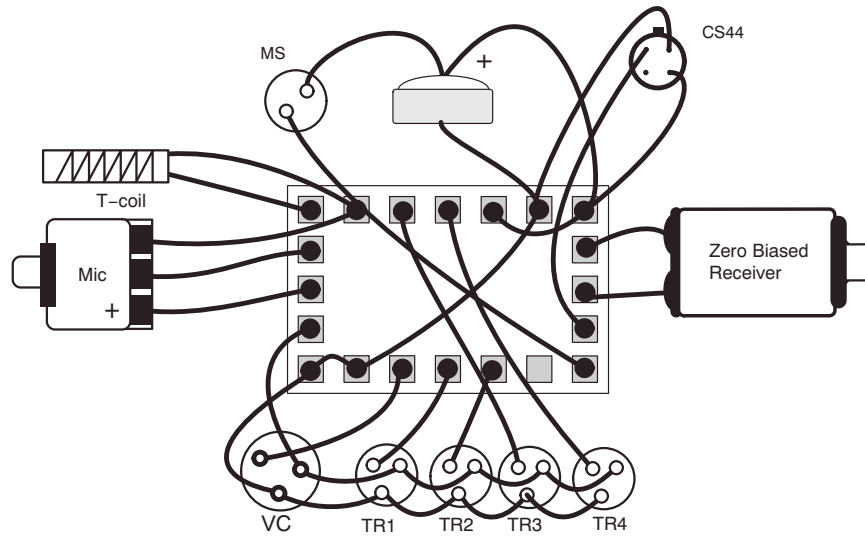
CONSOLIDATOR GA3227

TYPICAL APPLICATIONS (Cont'd)

Figure 5. Typical Assembly Diagram

CONSOLIDATOR GA3227 OVERVIEW

The Consolidator GA3227 hybrid comprises a configurable two−channel compressor circuit with two methods of operation – extended programmable mode and trimmer mode. The device can be configured as a one or two channel device with linear or WDRC processing. Configuration data stored in non−volatile memory defines hearing aid parameters. This data needs to be uploaded to the hybrid before the circuit becomes functional. The Consolidator GA3227 hybrid is programmed via the SDA pin using industry−standard programming boxes.

Configuration data is generated by an ARK product component library (DLL). The Consolidator GA3227 is fully supported by ON Semiconductor's software tools available from the ARK website: http://ark.onsemi.com/

During normal trimmer mode operation, a low−speed A/D circuit monitors the positions of up to four manual trimmers and a VC potentiometer. Trimmer position changes are immediately interpreted and translated into new circuit parameter values, which are then used to update the signal path.

ON Semiconductor's Library Manager tool in ARKonline® enables pre−defining of trimmer assignments for all common functions such as low−cut, high−cut, AGC parameters, wideband gain, and maximum power output (MPO).

SIGNAL PATH

There are two main audio input signal paths. The first path contains the microphone and second path contains the telecoil input, as selected by a programmable MUX. The microphone input is intended as the main audio input for single−microphone applications. The two audio inputs are buffered, sampled and converted into digital form using an A/D converter. The digital output is then converted into a 24 kHz 20−bit digital audio signal.

In Telecoil mode, gains are trimmed during the Cal/Config process to compensate for microphone/telecoil mismatches. The telecoil input can also be used as a second microphone input. In this case, the telecoil compensation

should be disabled. This can be done via the ARKonline wizard.

The wideband detector circuit output is routed to a band−split filter that divides the signal into two frequency bands. There is an option to configure the hybrid as a single channel device that simply shuts down and bypasses the band−split filter. The gain in each channel is a function of the overall detected wide−band energy. The two frequency bands are then summed back into a wide−band signal.

Further processing capabilities include a 1st to 3rd order low cut filter before the band−split filter. After the two channels are summed together, there is a 1st or 2nd order

high cut filter, one bi−quadratic filter followed by volume control, and a low−distortion AGC−O.

All AGC loops use a feed−forward topology to ensure system stability. Detectors in the AGCi path and AGC−O path are twin fast/slow detectors with independently adjustable attack and release time constants. The squelch detector, residing in the AGCi path, is implemented as a single fast/slow detector.

<div align="center">

FUNCTIONAL BLOCK DESCRIPTION
</div>

A/D and D/A Converter

The system's A/D converter is a 2nd−order sigma−delta modulator, operating at a 1.536 MHz sample rate. The system's input is pre−conditioned with anti−alias filtering and a programmable gain pre−amplifier. The analog output is over−sampled and modulated to produce a 1−bit pulse density modulated (PDM) data stream. The digital PDM data is then decimated down to pulse−code modulated (PCM) digital words at the system's sampling rate of 24 kHz.

The D/A is comprised of a digital 3rd−order sigma−delta modulator and an H−bridge. The modulator accepts PCM audio data from the DSP path and converts it into a 32−times over−sampled, 1−bit PDM data stream, which is then supplied to the H−bridge. The H−bridge is a specialized CMOS output driver used to convert the 1−bit data stream into a low−impedance, differential output voltage waveform suitable for driving zero−biased hearing aid receivers.

Channel Processing

Figure 6 represents the I/O characteristic of the AGC channel processing.
- Low input level expansion (squelch) region
- Low input level linear region
- Compression region
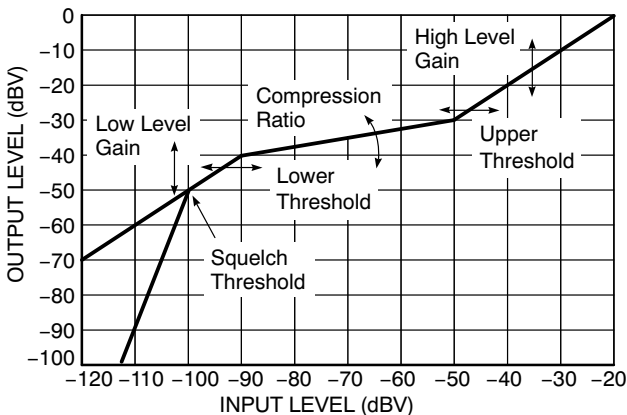- High input level linear region (return to linear)

Figure 6. Independent Channel I/O Curve Flexibility

The I/O characteristic of the AGC channel processing can be adjusted in the following ways:
- Squelch threshold (SQUELCHTH)
- Low level gain (LLGAIN)
- Lower threshold (LTH)
- High level gain (HLGAIN)

- Upper threshold (UTH)
- Compression ratio (CR)

During Parameter Map creation, constraints are applied to the compression parameters to ensure that the I/O characteristics are continuous. In both Extended Programmable mode and Trimmer mode, predefined parameter adjustments support two popular styles of compression ratio adjustment:
- The compression region of the I/O curve pivots about the upper threshold. As the compression ratio trimmer is adjusted, high−level gain remains constant while the low−level gain changes.
- The compression region of the I/O curve pivots about the lower threshold. Low−level gain remains constant as the compression ratio trimmer is adjusted.

Parameters such as low level gain, lower threshold and compression ratio can be combined and controlled by a single trimmer.

The squelch region within each channel implements a low level noise reduction scheme (1:2 expansion) for listener comfort. This scheme operates in quiet listening environments (programmable threshold) to reduce the gain at very low levels.

Single−channel compressor operation is supported by disabling the band split filter and one of the channel compressors. The remaining compressor can be configured as a Wide−Dynamic−Range Compressor (WDRC), or as an Input Compression Limiter (ICL).

HRX™ Head Room Expander

The Consolidator GA3227 has an enhanced Head Room Expander (HRX) circuit that increases the input dynamic range of the Consolidator GA3227 Digital without any unwanted audible artifacts. This is accomplished by dynamically adjusting the preamplifier's gain and the post−A/D attenuation depending on the input level.

Telecoil Path

The telecoil input is calibrated during the Cal/Config process. To compensate for the telecoil/microphone frequency response mismatch, a first order filter with 500 Hz corner frequency is implemented. Through ARKonline, it is possible to implement a telecoil compensation filter with an adjustable corner frequency. To accommodate for the gain mismatch, the telecoil gain is adjusted to match the microphone gain at 500 Hz or 1 kHz (default) and is selectable in ARKonline. There is also a telecoil gain adjustment parameter that can be enabled in

ARKonline and set in IDS, enabling manual adjustment of the telecoil gain compensation.

Volume Control & Trimmers

All parameters can be controlled via the SDA or assigned to the trimmers. The four trimmers have flexible parameter assignments so that any of them can be assigned to any available parameters. A complete list of parameters is available on ARKonline.

Both the external VC and trimmers are configured to work with a three−terminal 0.1 MΩ – 1 MΩ variable resistor. The volume control should have a log taper, while the trimmers should have a linear taper. Hysteresis is built into the circuitry to prevent unintentional level toggling.

Bi−Quadratic Filter

The bi−quadratic filter allows for additional frequency shaping. The filter coefficients can be entered in IDS.

AGC−O

The AGC−O module is an output limiting circuit with a fixed compression ratio of $\infty : 1$. The limiting level is programmable as a level measured as dB from full scale. 0 dBFS is the maximum output of the device. The AGC−O module has its own twin level detector, with programmable attack and release time constants.

MS and MS2 Switches

There are two, two−pole Memory Select (MS) switches available on the Consolidator GA3227, enabling users flexibility in switching between configurations. MS switches can be either momentary or static, as set up in ARKonline, and are configurable to be either pull−up or pull−down through the setting tab in IDS. In extended programmable mode, the switch must be set to pull−down. MS2 is a static switch and is used to select the third memory (Memory C).

Up to three memories can be configured in extended programmable mode, or one memory in trimmer mode. All memory select options are selectable via the ARKonline wizard.

In simple trimmer mode, there is one method for memory select. In this mode, when the telecoil is enabled, MS switches the Consolidator GA3227's input between the microphone and the telecoil using either a momentary or static switch which is selectable using ARKonline.

There are four memory select modes available in programmable and multi−memory trimmer mode as follows:

- Momentary Switch on MS
- Momentary Switch on MS, static switch on MS2 (jump to Memory C)
- Static switch on MS and MS2
- Static switch on MS, static switch on MS2 (jump to Memory C)

Momentary Switch on MS

This mode uses a single momentary switch on MS to change memories. Using this mode causes the part to toggle among memories A, B and C.

Momentary Switch on MS, Static Switch on MS2 (Jump to Memory C)

This mode uses a static switch on MS2 and a momentary switch on MS to change memories. If the static switch is OPEN, the part starts in memory A and toggles between memory A and B. If the static switch on MS2 is set to HIGH, the part automatically jumps to the memory C (occurs on startup or during normal operation). In this setup, the momentary switch's state is ignored. This prevents memory select beeps from occurring. When MS2 is set to OPEN, the part loads in the last select memory.

Table 4. DYNAMIC EXAMPLE WITH 3 VALID MEMORIES

(Conditions: T = momentary switch is toggled; 0 = OPEN; 1 = HIGH)

MS2	0	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0
MS	0	T	T	0	T	T	0	T	T	0	0	T	T	T	T	T
Memory	A	B	A	C	C	C	A	B	A	C	A	B	A	B	A	B

Static Switch on MS and MS2

This mode uses two static switches to change memories.

Table 5 describes which memory is selected depending on the state of the switches.

In this mode, it is possible to jump from any memory to any other memory simply by changing the state of both switches. If both switches are changed simultaneously, then the transition is smooth. Otherwise, if one switch is changed and then the other, the part transitions to an intermediate memory before reaching the final memory.

The part starts in whatever memory the switches are selecting. If a memory is invalid the part defaults to memory A.

Table 5. SWITCH FOR MS and MS2

MS	MS2	Memory
OPEN	OPEN	A
HIGH	OPEN	B (if valid, otherwise A)
OPEN	HIGH	A
HIGH	HIGH	C (if valid, otherwise A)

Static Switch on MS, Static Switch on MS2 (Jump to Memory C)

This mode uses two static switches to change memories.

Unlike in the previous example, this mode switches to the last valid memory when the static switch on MS2 is HIGH. This means that this mode can only use a maximum of three memories (even if four valid memories are programmed). Table 6 describes which memory is selected depending on the state of the switches.

Table 6. STATIC SWITCH ON MS, STATIC SWITCH ON MS2 (Jump to Memory C)

MS	MS2	Memory
OPEN	OPEN	A
HIGH	OPEN	B (if valid, otherwise A)
OPEN	HIGH	C
HIGH	HIGH	C

In this mode, it is possible to jump from any memory to any other memory simply by changing the state of both switches. If both switches are changed simultaneously, then the transition is smooth. Otherwise, if one switch is changed and then the other, the part will transition to an intermediate memory before reaching the final memory.

When MS2 is set HIGH, the state of the switch on MS is ignored. This prevents memory select beeps from occurring when switching MS when MS2 is HIGH.

The part starts in whatever memory the switches are selecting. If the device starts up in a memory other than A, and the memory beep tones are enabled, the device emits the corresponding tones for that memory. If a memory is invalid, the part defaults to memory A.

Audible Memory Change Indicator

The Consolidator GA3227 Digital can be configured to produce tones to indicate a memory change.

Through ARKonline, the Consolidator GA3227 can be configured to either enable or disable the Memory Change Indicator. When the Memory Change Indicator is enabled, there is an option to have a single beep for each memory change or multiple-beeps.

The amplitude and frequency of the memory change tone can be selected independently from the Tone Generator settings and can be individually selected for each memory.

When the memory change multiple-beep is enabled, and the memory change tone is enabled, then during a memory change operation the selected tone beeps a code to indicate which memory was selected. The beep sequence is 150 ms ON, followed by 150 ms OFF, between the beeps. The memory change beeping code is deciphered in Table 7.

Table 7. MEMORY CHANGE BEEPING CODE

Selected Memory	# Beeps
A	1
B	2
C	3

Tone Generator

The tone generator is capable of producing programmable tones. When the Tone Generator is enabled, the Consolidator GA3227 Digital connects the output of the tone generator to the input of the D/A converter. The programmed tone is output until the Tone Generator is disabled. When disabled, the normal audio signal path is connected again. The tone generator produces a beep to indicate a memory select change, a microphone/telecoil selection change, or to warn the user of low battery voltage.

Low Battery Indicator (Power−On / Power−Off)

During power−on, the Consolidator GA3227 Digital is held in a reset state until V_b reaches a turn−ON threshold, and the hybrid's internal control logic determines that the supply is stable. When this occurs, the hybrid begins its power−on sequence.

When a low battery condition is detected, the Consolidator GA3227 Digital sends out a series of three beeps (225 ms ON, 225 ms OFF, 225 ms ON, 225 ms OFF, 225 ms ON) to indicate the battery is low. This is repeated every five minutes until the device reaches the turn−OFF threshold.

If V_b drops below the turn−OFF threshold, then the Consolidator GA3227 Digital is returned to its reset state and the audio output is muted.

There are four reset modes which are selectable through ARKonline.

The first is the shallow−reset mode which, during the power−on sequence, circuit starts when the supply voltage rises above the turn−ON threshold after shutdown. The device functions until the supply voltage drops below the turn−OFF threshold, but recovers when the device rises above the turn−ON threshold again.

The second is deep−reset mode which begins when the supply voltage rises above the turn−ON threshold after shutdown. Once the supply voltage drops below the turn−OFF threshold the Consolidator GA3227 shuts down and remains there until the supply voltage drops below approximately 0.3 V and subsequently rises above the turn−ON threshold after shutdown.

The third is a combination of these two modes, where the device starts up in shallow−reset mode initially, then changes over to deep−reset mode after 5 minutes.

The fourth option is to have the gain reduced as the battery voltage drops. When the supply falls below the low battery threshold the low battery tones will be emitted and the wideband gain will be reduced by 3 dB. As the battery voltage continues to drop, the low battery tones will continue and the wideband gain will continue to be reduced until the turn−OFF threshold is reached when the device will shut down.

An additional option configurable via ARKonline is to have the gain reduced as the battery voltage drops. When the supply falls below the low battery threshold, the low battery tones are emitted and the wideband gain is reduced by 3 dB. As the battery voltage continues to drop, the low battery tones continue and the wideband gain continues to be reduced until the turn−OFF threshold is reached as the device shuts down.

Current Consumption

Typical current consumption of the Consolidator GA3227 Digital, as stated in the Electrical Characteristics section, is measured at a specific configuration and settings.

Software

Full software support is provided for every stage of development from design to manufacturing to fitting. For details, refer to the Getting Started with ARK Software Guide.

SDA Communication

The Consolidator GA3227 Digital is programmed via the SDA pin using industry standard programming boxes. During parameter changes the main audio signal path of the hybrid is temporarily disabled and replaced with a low gain *bypass path* to avoid the generation of disturbing audio transients. Once the changes are complete, the main audio path is re−activated.

Any changes made during programming are lost at power−off unless they are explicitly burned to EEPROM memory.

Power Management

The Consolidator GA3227 Digital was designed to accommodate high power applications. AC ripple on the supply can cause instantaneous reduction of the battery's voltage, potentially disrupting the circuit's function. The Consolidator GA3227 has a separate power supply and ground connection for the output stage. This enables hearing instrument designers to accommodate external RC filters to minimize any AC ripple from the supply line. Reducing this AC ripple greatly improves the stability of the circuit and prevents unwanted reset of the circuit caused by spikes on the supply line. For more information on properly designing a filter to reduce supply ripple, refer to the Using DSP Hybrids in High Power Applications Initial Design Tips information note.

ORDERING INFORMATION

Device	Package	Shipping[†]
GA3227−E1	20 Pad Hybrid	25 Units / Bubble Pack
GA3227−E1−T	20 Pad Hybrid	250 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Hybrid Jig Ordering Information

To order a Hybrid Jig Evaluation Board for Consolidator GA3227 contact your Sales Account Manager or FAE and use part number GA3227GEVB.

Table 8. PAD POSITION AND DIMENSIONS

Pad No.	Pad Position		Pad Dimensions	
	X	Y	Xdim (mil)	Ydim (mil)
1	0	0	20	20
2	36.67	−5	20	30
3	73.33	0	20	20
4	110	0	20	20
5	146.67	0	20	20
6	183.33	0	20	20
7	220	0	20	20
8	220	−29.9	20	20
9	220	−59.8	20	20
10	220	−89.67	20	20
11	220	−119.61	20	20
12	183.33	−119.61	20	20
13	146.67	−119.61	20	20
14	110	−119.61	20	20
15	73.33	−119.61	20	20
16	36.67	−119.61	20	20
17	0	−119.61	20	20
18	0	−89.67	20	20
19	0	−59.8	20	20
20	0	−29.9	20	20
Pad No.	X	Y	Xdim (mm)	Ydim (mm)
1	0	0	0.508	0.508
2	0.9314	−0.1270	0.508	0.762
3	1.8626	0	0.508	0.508
4	2.7940	0	0.508	0.508
5	3.7254	0	0.508	0.508
6	4.6566	0	0.508	0.508
7	5.5880	0	0.508	0.508
8	5.5880	−0.7595	0.508	0.508
9	5.5880	−1.5189	0.508	0.508
10	5.5880	−2.2776	0.508	0.508
11	5.5880	−3.0381	0.508	0.508
12	4.6566	−3.0381	0.508	0.508
13	3.7254	−3.0381	0.508	0.508
14	2.7940	−3.0381	0.508	0.508
15	1.8626	−3.0381	0.508	0.508
16	0.9314	−3.0381	0.508	0.508
17	0	−3.0381	0.508	0.508
18	0	−2.2776	0.508	0.508
19	0	−1.5189	0.508	0.508
20	0	−0.7595	0.508	0.508

CONSOLIDATOR GA3227

PACKAGE DIMENSIONS

0.250
(6.35)

0.150
(3.81)

GA3227−E1
XXXXXX

0.050 MAX
(1.27)

0.015
(0.635)

0.015
(0.635)
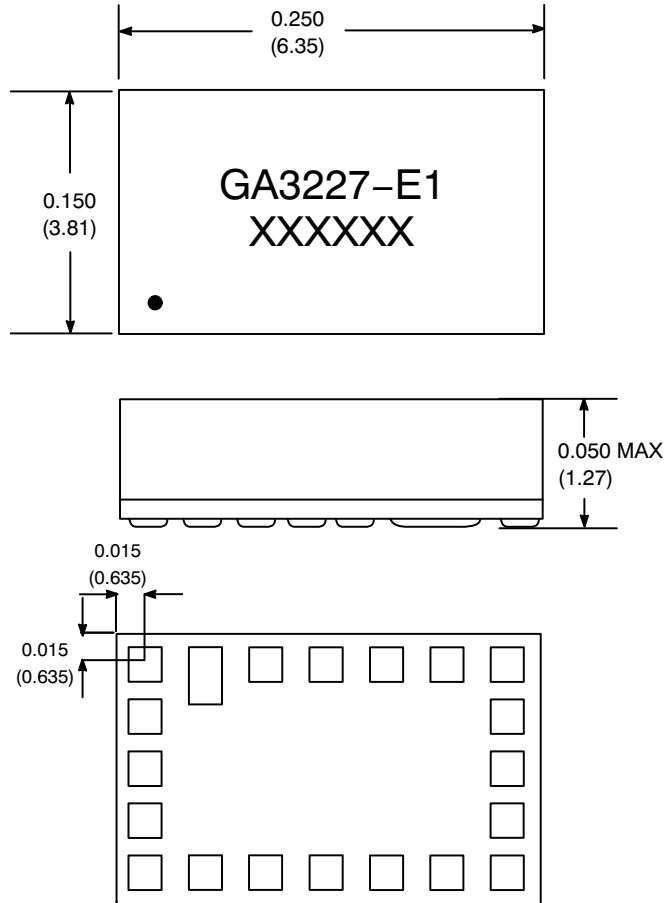
Dimension units are in inches.
Dimensions in parentheses are in millimeters, converted from inches and include minor rounding errors.
1.000 inches = 25.4 mm
Dimension tolerances: ±0.005 (±0.10) unless otherwise stated.
• = location of Pin 1
RoHS compliant hybrid, MSL#4, 240°C peak reflow, SAC305
This Hybrid is designed for either point−to−point manual soldering or for reflow according to ON Semiconductor's reflow process.

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