CLEAR LOGIC

LIBERATOR CL10K200S

Key Features

- Fully Compatible to the Altera® FLEX® 10KS Family
- Prototype Your System With Altera FPGAs
- Seamlessly Migrate Production To Clear Logic
- No ASIC Engineering, No NRE, And No Test Vector Development
- Very Fast, Dense Signal Routing Using Vertical Link Interconnect
- "Gate Array" Option Eliminates Configuration EPROMs
- Fabricated Using 0.25 Micron CMOS Process
- Very Low Power Consumption (Active And Standby)
- High Density
  - 200,000 Usable Gates
  - 9,984 Logic Elements
  - 98,304 RAM Bits
  - 470 Maximum User I/O Pins

CL10KE Product Family Overview

Parameter	CL10K30E	CL10K50E CL10K50S	CL10K100E	CL10K200E CL10K200S
Typical Gates (Logic and RAM)	30,000	50,000	100,000	200,000
Maximum System Gates	119,000	199,000	257,000	513,000
Logic Elements	1,728	2,880	4,992	9,984
Embedded Array Blocks	6	10	12	24
Total RAM Bits	24,576	40,960	49,152	98,304
Max User I/O pins	220	254	338	470
Speed Grades	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2, -3
Packages	144-pin TQFP 208-pin PQFP 256-pin FBGA 484-pin FBGA	144-pin TQFP 208-pin PQFP 240-pin PQFP 256-pin FBGA 356-pin SBGA 484-pin FBGA	208-pin PQFP 240-pin PQFP 256-pin FBGA 356-pin SBGA 484-pin FBGA	240-pin PQFP 356-pin SBGA 484-pin FBGA 600-pin SBGA 672-pin FBGA

10KE tbl 01

Description

The LIBERATOR™ CL10KS family offers you all of the time-to-market benefits of designing with programmable logic. Simply use Altera FLEX 10KS FPGAs to prototype and verify the design. Then, take five minutes to submit the bitstream using Clear Logic's web site! Within eight weeks, your system can be in volume production using compatible Clear Logic devices.

LIBERATOR technology frees you to completely design, prototype, and verify your custom logic using Altera FLEX 10KS products. Clear Logic's innovative technology eliminates NRE costs, test vector development, ordering minimums, and long lead times. No re-simulation or re-layout is required, because Clear Logic offers an architecture that is exactly compatible to the functionality of the FPGA prototype. Clear Logic's NoFault® test technology ensures complete test coverage through the use of special scan test registers.

The LIBERATOR family is based upon an array of logic elements. Each logic element contains a configurable look-up table for combinatorial functions and a register for sequential operations. Eight logic elements in a group form a block. Logic functions and signal routing are defined by Clear Logic's proprietary vertical metal links.

Laser-based configuration allows quick-turn prototyping and eliminates NRE costs for photomasks. Inherent CL10KS family performance benefits include extremely consistent propagation delays, reduced power consumption, and improved immunity to noise and upset events.

Configuration

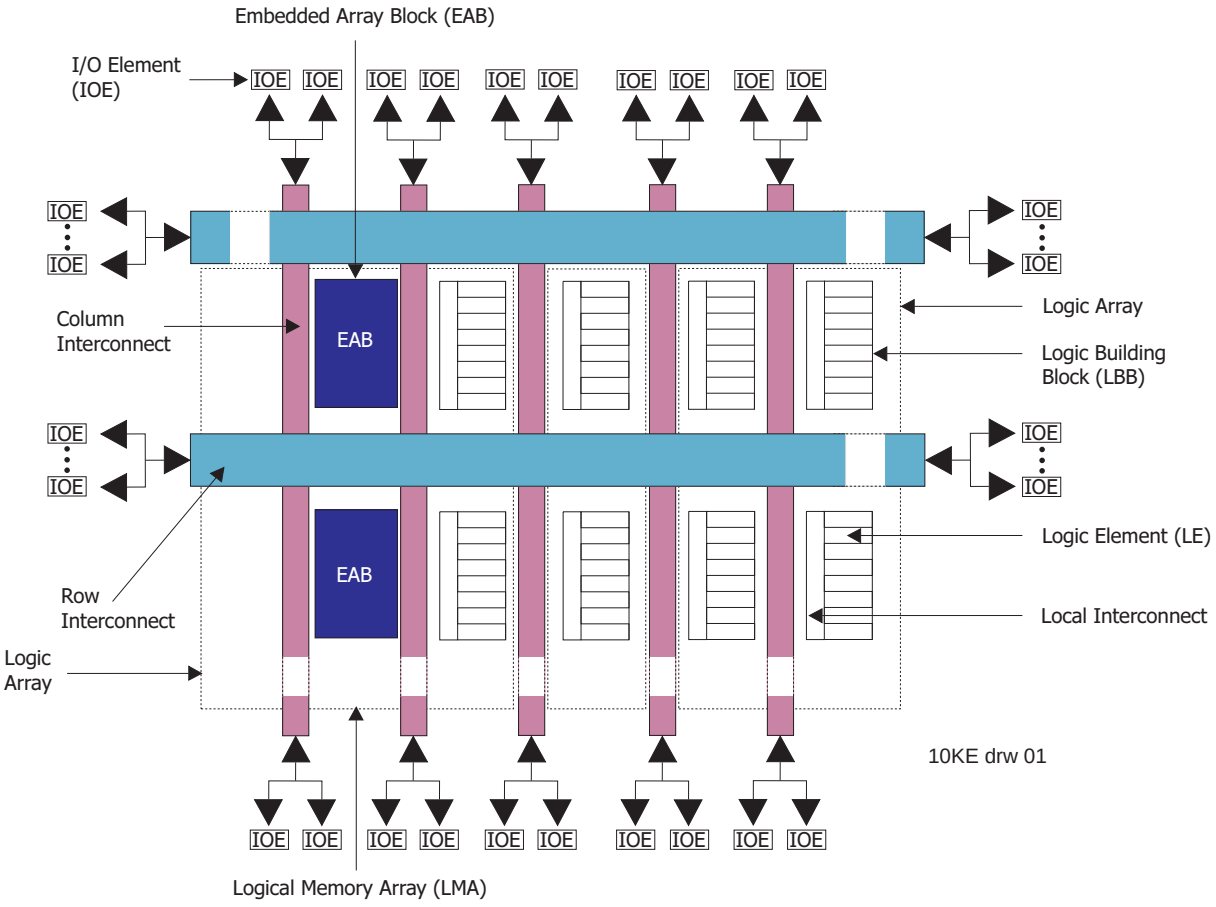
The "Gate Array" configuration mode eliminates the need for external EPROMs or software configuration. The LIBERATOR device is already factory-configured when it is shipped. When using the device in the "Gate Array" mode, it powers up fully configured. In this mode, if the customer selects INIT_DONE option, this pin will always be high.

Additional Information

For further information on designing with the LIBERATOR family, please refer to these documents:

- AN-01: Requesting a First Article. This document provides instructions on how to request first articles by submitting a bitstream file to Clear Logic's web site.
- AN-02: Clear Logic Packaging Guide. This document provides specifications and drawings for packages used by the CL10K family and other Clear Logic devices.
- AN-13: LIBERATOR -- A New Way To Design. This document describes the most efficient path for custom logic designs up to 200K gates using FPGA design techniques and going to production with Clear Logic.
- AN-14: CL10K Technology White Paper. This document outlines the technologies employed by the LIBERATOR family.
- AN-15: LIBERATOR System Configuration. This document contains a detailed discussion of all aspects of configuring CL10K-based systems.
- AN-16: Introduction to the Clear Logic Verilog Model Generator. Clear Logic now has Verilog models of your FPGA converted design. Learn what it is and how it can help you.
- AN-17: Clear Logic LIBERATOR Design Models. This document outlines the capabilities and freedom available in the Clear Logic Verilog and VHDL design models.
- AN-18: Debugging Designs Using Clear Logic Models. This document shows the enhanced troubleshooting capabilities that the Clear Logic LIBERATOR Verilog/VHDL design models bring to the system debugging process.

Block Diagram



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Pin Configuration

Pin Name	240-Pin PQFP/RQFP	356-Pin SBGA	600-Pin SBGA
MSEL0	124	D4	F5
MSEL1	123	D3	C1
nSTATUS	60	D24	D32
nCONFIG	121	D2	D4
DCLK	179	AC5	AP1
CONF_DONE	2	AC24	AM32
INIT_DONE	26	T24	AE32
nCE	178	AC2	AN2
nCEO	3	AC22	AP35
nWS	238	AE24	AR29
nRS	236	AE23	AM28
nCS	240	AD24	AL29
CS	239	AD23	AN29
RDYnBSY	23	U22	AG35
CLKUSR	11	AA24	AM34
DATA7	190	AF4	AM13
DATA6	188	AD8	AR12
DATA5	186	AE5	AN12
DATA4	185	AD6	AP11
DATA3	183	AF2	AM11
DATA2	182	AD5	AR10
DATA1	181	AD4	AN10
DATA0	180	AD3	AM4
TDI	177	AC3	AN1
TDO	4	AC23	AN34

10K200S tbl 01A

Pin Configuration

Pin Name	240-Pin PQFP/RQFP	356-Pin SBGA	600-Pin SBGA
TCK	1	AD25	AL31
TMS	58	D22	C35
TRST	59	D23	C34
Dedicated Inputs	90, 92, 210, 212	A13, B14, AF14, AE13	C18, D18, AM18, AN18
Dedicated Clock Pins	91, 211	A14, AF13	AL18, E18
DEV_CLRn	209	AD13	AR17
DEV_OE	213	AE14	AR19
VCCINT	5, 20, 27, 40, 47, 76, 96, 122, 130, 139, 150, 159, 170, 187, 225	A1, A26, C14, C26, D5, F1, H22, J1, M26, N1, T26, U5, AA1, AD26, AF1, AF26	A11, A19, B1, D24, E2, F31, F35, H1, K32, M2, N34, P5, T35, U3, V32, Y2, AA33, AB5, AD35, AE4, AF32, AG5, AK31, AK35, AL3, AP24, AR11, AR18
VCCIO	16, 37, 57, 77, 112, 140, 160, 189, 205, 224	A7, A23, B3, C15, D25, F4, H24, K5, M23, P2, T25, V2, W22, AB1, AC25, AD18M AF3, AF7, AF16	A20, A27, C2, C3, C4, C8, C15, C23, C32, C33, D5, D31, E5, E12, E31, AL5, AL12, AM5, AM19, AM26, AM31, AN3, AN4, AN8, AN15, AN32, AN33, AP34, AR23
VCC_CKLK	89	C14	B18
GNDINT	10, 22, 32, 42, 52, 69, 85, 93, 104, 125, 135, 145, 155, 165, 176, 197, 216, 232	A2, A10, A20, B1, B13, B22, B25, B26, C2, C9, C13, C25, H23, J26, K1, M1, N26, R1, R26, T1, U26, W1, AD2, AD14, AD20, AE1, AE2, AE7, AE25, AE26, AF11, AF19, AF25	A1, A2, A3, A4, A5, A31, A32, A33, A34, A35, B2, B3, B4, B5, B6, B31, B32, B33, B34, B35, C5, C6, C30, C31, D6, D30, E6, E30, AL6, AL30, AM6, AM30, AN5, AN6, AN30, AN31, AN35, AP2, AP3, AP4, AP5, AP6, AP30, AP31, AP32, AP33, AR1, AR2, AR3, AR4, AR5, AR30, AR31, AR32, AR33, AR34, AR35
GND_CKLK	93	B13	A18
No Connect	-	-	-
Total user I/O Pins	**182**	**274**	**470**

10K200S tbl 01B

Pin Configuration

Pin Name	484-Pin FBGA	672-Pin FBGA
MSEL0	U4	W6
MSEL1	V4	Y6
nSTATUS	W19	AA21
nCONFIG	T7	V9
DCLK	E5	G7
CONF_DONE	F18	H20
INIT_DONE	K19	M21
nCE	E4	G6
nCEO	E19	G21
nWS	E17	G19
nRS	F17	H19
nCS	D19	F21
CS	D18	F20
RDYnBSY	K17	M19
CLKUSR	G18	J20
DATA7	E8	G10
DATA6	G7	J9
DATA5	D7	F9
DATA4	E7	G9
DATA3	F6	H8
DATA2	D5	F7
DATA1	E6	G8
DATA0	D4	F6
TDI	F5	H7
TDO	F19	H21

10K200S tbl 01C

Pin Configuration

Pin Name	484-Pin FBGA	672-Pin FBGA
TCK	E18	G20
TMS	U18	W20
TRST	V19	Y21
Dedicated Inputs	E12, H11, R12, V11	Y13, U14, G14, K13
Dedicated Clock Pins	D12, P11	T13, F14
DEV_CLRn	G11	J13
DEV_OE	F12	H14
VCCINT	C11, C15, H14, J8, J10, J12, J15, L9, L10, L13, M10, M13, M14, N12, P8, P10, P15, R14, V5, W21, Y8, AA12	E13, E17, H2, H25, K16, L10, L12, L14, L17, M2, M25, N11, N12, N15, P12, P15, R14, T2, T10, T12, T17, T25, U16, Y7, AA23, AB10, AC14
VCCIO	A6, A13, B5, E1, G1, G15, H9, H20, J11, J13, K9, K11, K14, K20, L14, M9, N3, N9, N11, N14, N20, P13, R1, R9, T3, T15, T22, V22, AB13	C8, C15, D7, G3, J3, J17, K11, K22, L13, L15, M11, M13, M16, M22, N16, P11, R5, R11, R13, R16, R22, T15, U3, U11, V5, V17, V24, Y2, Y24, AA26, AD15
VCC_CKLK	P12	T14
GND	A1, A8, A22, B1, B2, B17, B21, B22, C2, C21, E21, G3, G21, H2, H8, H15, J9, J14, J20, K3, K10, K12, K13, L11, L12, M11, M12, M20, N10, N13, P9, P14, R8, R15, R22, T1, V3, W20, Y1, Y2, Y3, Y21, Y22, AA1, AA6, AA22, AB11, AB16	A2, A25, B2, B25, C3, C10, C24, D3, D4, D19, D23, D24, E4, E23, G23, J5, J23, K4, K10, K17, L11, L16, L22, M5, M12, M14, M15, N13, N14, P13, P14, P22, R12, R15, T11, T16, U10, U17, U24, V3, Y5, AA22, AB23, AB4, AB5, AB23, AB24, AC3, AC8, AC24, AD13, AD18, AE2, AE25, AF2, AF25
GND_CKLK	W11	AA13
No Connect	-	A4, A5, A6, A10, A11, A12, A13, A14, A15, A16, A17, A18, A19, A20, A21, A22, A23, A24, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B16, B19, B20, B21, B22, B23, B24, C1, AE4, AE5, AE6, AE7, AE8, AE9, AE10, AE11, AE12, AE14, AE15, AE16, AE17, AE19, AE20, AE21, AE22, AE23, AF4, AF5, AF6, AF7, AF8, AF9, AF10, AF12, AF13, AF14, AF15, AF16, AF18, AF20, AF21, AF23, AF24
Total user I/O Pins	**369**	**470**

10K200S tbl 01C

DC Electrical Specifications

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage		-0.5	3.6	V
V_I	DC Input Voltage[1]		-2.0	5.75	V
I_{OUT}	DC Output Current, per Pin		-25	25	mA
T_{STG}	Storage Temperature	No Bias	-65	150	°C
T_{AMB}	Ambient Temperature	Under Bias	-65	135	°C
T_J	Junction Temperature	Under Bias		135	°C

10KE tbl 02

Recommended Operating Conditions [2]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply Voltage, Internal Logic and Input Buffers				
	Commercial Grade Devices		2.375	2.625	V
	Industrial Grade Devices		2.375	2.625	V
V_{CCIO}	DC Input Voltage for 3.3V Operation				
	Commercial Grade Devices		3.00	3.60	V
	Industrial Grade Devices		3.00	3.60	V
V_{CCIO}	DC Input Voltage for 2.5V Operation				
	Commercial Grade Devices		2.375	2.625	V
	Industrial Grade Devices		2.375	2.625	V
V_I	Input Voltage		-0.5	5.75	V
V_O	Output Voltage		0	VCCIO	V
T_A	Operating Temperature				
	Commercial Temperature Range		0	70	°C
	Industrial Temperature Range		-40	85	°C
t_R	Input Signal Rise Time			40	ns
t_F	Input Signal Fall Time			40	ns

10KE tbl 03B

DC Electrical Specifications cont.

DC Electrical Characteristics (over the operating range)

Symbol	Parameter	Conditions	Min	Typ[3]	Max	Unit
V_{IH}	Input HIGH Voltage		Lower of 1.7 or 0.5 x V_{CCINT}		5.75	V
V_{IL}	Input LOW Voltage		-0.5		0.3 x V_{CCIO}	V
V_{OH}	3.3-V High-Level TTL Output Voltage	I_{OH} = -8 mA DC, V_{CCIO} = 3.00 V	2.4			V
	3.3-V High-Level CMOS Output Voltage	I_{OH} = -0.1 mA DC, V_{CCIO} = 3.00 V	V_{CCIO}-0.2			V
	3.3-V High-Level PCI Output Voltage	I_{OH} = -0.5 mA DC, V_{CCIO} = 3 to 3.60 V	0.9 x V_{CCIO}			V
	2.5-V High-Level Output Voltage	I_{OH} = -0.1 mA DC, V_{CCIO} = 2.30 V	2.1			V
		I_{OH} = -1 mA DC, V_{CCIO} = 2.30 V	2.0			V
		I_{OH} = -2 mA DC, V_{CCIO} = 2.30 V	1.7			V
V_{OL}	3.3-V Low-Level TTL Output Voltage	I_{OL} = 9 mA DC, V_{CCIO} = 3.00 V			0.45	V
	3.3-V Low-Level CMOS Output Voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.00 V			0.2	V
	3.3-V Low-Level PCI Output Voltage	I_{OL} = 1.5 mA DC, V_{CCIO} = 3 to 3.60 V			0.1 x V_{CCIO}	V
	2.5-V Low-Level Output Voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 2.30 V			0.2	V
		I_{OL} = 1 mA DC, V_{CCIO} = 2.30 V			0.4	V
		I_{OL} = 2 mA DC, V_{CCIO} = 2.30 V			0.7	V
I_{IN}	Input Leakage Current	V_I = 5.3V to -0.3V	-10		10	µA
I_{OZ}	Output Leakage Current	V_O = 5.3V to -0.3V	-10		10	µA
I_{CC0}	Standby Current	V_I = GND, No Load		5		mA

10KE tbl 04

Capacitance[4]

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

10KE tbl 05

AC Electrical Specifications

I/O Element Timing Parameters [5]

		Speed: -1		Speed: -2		Speed: -3		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IOD}	IOE Register Data Delay		2.4		2.8		3.8	ns
t_{IOC}	IOE Register Control Signal Delay		0.3		0.3		0.5	ns
t_{IOCO}	IOE Register Clock to Output Delay		0.2		0.2		0.3	ns
t_{IOCOMB}	IOE Combinatorial Delay		0.5		0.6		0.8	ns
t_{IOSU}	IOE Register Setup Time Before Clock	2.2		2.6		3.5		ns
t_{IOH}	IOE Register Hold Time After Clock	0.5		0.6		0.8		ns
t_{IOCLR}	IOE Register Clear Delay		0.2		0.2		0.3	ns
t_{OD1}	Output Buffer and Pad Delay Slow Slew Rate = off, VCCIO = V_{CCINT}		1.1		1.3		1.8	ns
t_{OD2}	Output Buffer and Pad Delay Slow Slew Rate = off, VCCIO = Low Voltage		0.6		0.9		1.6	ns
t_{OD3}	Output Buffer and Pad Delay Slow Slew Rate = on		3.0		3.5		4.8	ns
t_{ZX}	Output Buffer Disable Delay[6]		1.1		1.3		1.8	ns
t_{ZX1}	Output Buffer Disable Delay Slow Slew Rate = off, VCCIO = V_{CCINT}[6]		1.1		1.3		1.6	ns
t_{ZX2}	Output Buffer Disable Delay Slow Slew Rate = off, VCCIO = Low Voltage[6]		0.6		0.9		1.6	ns
t_{ZX3}	Output Buffer Disable Delay Slow Slew Rate = on[6]		3.0		3.5		4.8	ns
t_{INREG}	IOE Input Pad and Buffer to IOE Register Delay		5.0		5.9		8.0	ns
t_{IOFD}	IOE Register Feedback Delay		3.0		3.6		4.8	ns
t_{INCOMB}	IOE Input Pad and Buffer to Interconnect Delay		3.0		3.6		4.8	ns

10KE tbl 06A

AC Electrical Specifications cont.

External Timing Parameters[4]

		Speed: -1		Speed: -2		Speed: -3		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{DRR}	Register to Register Delay via Four LEs, Three Row Interconnects, and Four Local Interconnects		10.0		12.0		16.0	ns
t_{INSU}	Setup Time with Global Clock at IOE Register	3.1		3.7		4.7		ns
t_{INH}	Hold time with Global Clock at IOE Register	0.0		0.0		0.0		ns
t_{OUTCO}	Output Data Hold Time After Clock	2.0	3.7	2.0	4.4	2.0	6.3	ns

10KE tbl 07A

Logic Element Timing Parameters[5]

		Speed: -1		Speed: -2		Speed: -3		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{LUT}	Look-up Table Delay for Data-in		0.6		0.8		1.1	ns
t_{CLUT}	Look-up Table Delay for Carry-in		0.5		0.6		0.8	ns
t_{RLUT}	Look-up Table Delay for LE Register Feedback		0.7		0.8		1.1	ns
t_{PACKED}	Data-in to Packed Register Delay		0.5		0.6		0.8	ns
t_{EN}	LE Register Enable Delay		0.6		0.7		0.9	ns
t_{CICO}	Carry-in to Carry-out Delay		0.2		0.2		0.3	ns
t_{CGEN}	Data-in to Carry-out Delay		0.5		0.5		0.8	ns
t_{CGENR}	LE Register Feedback to Carry-out Delay		0.2		0.2		0.3	ns
t_{CASC}	Cascade Chain Routing Ddelay		0.8		0.9		1.2	ns
t_{C}	LE Register Control Signal Delay		0.5		0.6		0.8	ns
t_{CO}	LE Register Clock-to-output Delay		0.5		0.6		0.7	ns
t_{COMB}	Combinatorial Delay		0.5		0.6		0.7	ns
t_{SU}	LE Register Setup Time Before Clock	0.5		0.6		0.8		ns
t_{H}	LE Register Hold Time After Clock	0.9		1.1		1.5		ns
t_{PRE}	LE Register Preset Delay		0.5		0.6		0.8	ns
t_{CLR}	LE Register Clear Delay		0.5		0.6		0.8	ns
t_{CH}	Clock High Time	2.0		2.5		3.0		ns
t_{CL}	Clock Low Time	2.0		2.5		3.0		ns

10KE tbl 08A

AC Electrical Specifications cont.

Interconnect Timing Parameters[5]

		Speed: -1		Speed: -2		Speed: -3		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
$t_{DIN2IOE}$	Delay from Dedicated Input Pin to IOE Control Input		3.5		3.9		4.9	ns
t_{DIN2LE}	Delay from Dedicated Input Pin to LE or EAB Control Input		0.6		0.6		0.9	ns
$t_{DIN2DATA}$	Delay from Dedicated Input or Clock Pin to LE or EAB Data		2.0		2.1		2.9	ns
$t_{DCLK2IOE}$	Delay from Dedicated Clock Pin to IOE Clock		1.7		2.0		2.8	ns
$t_{DCLK2LE}$	Delay from Dedicated Clock Pin to LE or EAB Clock		0.6		0.6		0.9	ns
$t_{SAMELAB}$	Delay from an LE to LE in Same LAB		0.1		0.1		0.2	ns
$t_{SAMEROW}$	Delay for Driving a Row IOE, LE or EAB to a Row IOE, LE or EAB in the Same Row		1.7		1.8		1.7	ns
$t_{SAMECOLUMN}$	Delay from an LE to IOE in the Same Column		1.2		1.1		0.8	ns
$t_{DIFFROW}$	Delay for Driving a Column IOE, LE or EAB to an LE or EAB in a Different Row		2.9		2.9		2.5	ns
$t_{TWOROWS}$	Delay for Driving a Row IOE or EAB to an LE or EAB in a Different Row		4.6		4.7		4.2	ns
$t_{LEPERIPH}$	Delay from an LE to IOE Control Signal via the Peripheral Dontol Bus		4.3		4.9		5.9	ns
$t_{LABCARRY}$	Delay from an LE Carry-out Signal to an LE Carry-in Signal in a Different LAB		0.1		0.1		0.2	ns
$t_{LABCASC}$	Delay from an LE Cascade-out Signal to an LE Cascade-in Signal in a Different LAB		0.3		0.3		0.5	ns

10KE tbl 09A

AC Electrical Specifications cont.

EAB Timing Parameters[5]

		Speed: -1		Speed: -2		Speed: -3		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
$t_{EABDATA1}$	Delay from Data or Address to EAB for Combinatorial Input		1.7		2.0		2.7	ns
$t_{EABDATA2}$	Delay from Data or Address to EAB for Registered Input		0.6		0.7		0.9	ns
t_{EABWE1}	WE Delay to EAB for Combinatorial Input		1.1		1.3		1.8	ns
t_{EABWE2}	WE Delay to EAB for Registered Input		0.4		0.4		0.6	ns
t_{EABCLK}	EAB Register Clock Delay		0.0		0.0		0.0	ns
t_{EABCO}	EAB Register Clock-to-output Delay		0.3		0.3		0.5	ns
$t_{EABBYPASS}$	Bypass Register Delay		0.5		0.6		0.8	ns
t_{EABSU}	EAB Register Setup Time	0.9		1.0		1.4		ns
t_{EABH}	EAB Register Hold Time	0.4		0.4		0.6		ns
t_{AA}	Address Access Delay		3.2		3.8		5.1	ns
t_{WP}	Write Pulse Width	2.5		2.9		3.9		ns
t_{WDSU}	Data Setup Time Before Falling Edge of Write Pulse	0.9		1.0		1.4		ns
t_{WDH}	Data Hold Time After Falling Edge of Write Pulse	0.1		0.1		0.2		ns
t_{WASU}	Address Setup Time Before Rising Edge of Write Pulse	1.7		2.0		2.7		ns
t_{WAH}	Address Hold After Falling Edge of Write Pulse	1.8		2.1		2.9		ns
t_{WO}	Write Enable to Date Output Delay		2.5		2.9		3.9	ns
t_{DD}	Data-in to Date-out Delay		2.5		2.9		3.9	ns
t_{EABOUT}	Data-out Delay		0.5		0.6		0.8	ns
t_{EABCH}	Clock High Time	1.5		2.0		2.5		ns
t_{EABCL}	Clock Low Time	1.5		2.0		2.5		ns

10KE tbl 10A

AC Electrical Specifications cont.

EAB Timing Parameters[5]

		Speed: -1		Speed: -2		Speed: -3		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{EABAA}	EAB Address Access Delay		6.4		7.6		10.2	ns
$t_{EABRCCOMB}$	EAB Asynchronous Read Cycle Time	6.4		7.6		10.2		ns
$t_{EABRCREG}$	EAB Synchronous Read Cycle Time	4.4		5.1		7.0		ns
t_{EABWP}	EAB Write Pulse Width	2.5		2.9		3.9		ns
$t_{EABWCCOMB}$	EAB Asynchronous Write Cycle Time	6.0		7.0		9.5		ns
$t_{EABWCREG}$	EAB Synchronous Write Cycle Time	6.8		7.8		10.6		ns
t_{EABDD}	EAB Data-in to Data-out Delay		5.7		6.7		9.0	ns
$t_{EABDATACO}$	EAB Clock-to-output Delay Using Output Registers		0.8		0.9		1.3	ns
$t_{EABDATASU}$	EAB Data/Address Setup Time Using Input Register	1.5		1.7		2.3		ns
$t_{EABDATAH}$	EAB Data/Address Hold Time Using Input Register	0.0		0.0		0.0		ns
$t_{EABWESU}$	EAB WE Setup When Using Input Register	1.3		1.4		2.0		ns
$t_{EABWESH}$	EAB WE Hold Time When Using Input Register	0.0		0.0		0.0		ns
$t_{EABWDSU}$	EAB Data Setup Time to Falling Edge of Write Pulse When Not Using Input Registers	1.5		1.7		2.3		ns
t_{EABWDH}	EAB Data Hold Time After Falling Edge of Write Pulse When Not Using Input Registers	0.0		0.0		0.0		ns
$t_{EABWASU}$	EAB Address Setup Time to Rising Edge of Write Pulse When Not Using Input Registers	3.0		3.6		4.8		ns
t_{EABWAH}	EAB Address Hold Time After Falling Edge of Write Pulse When Not Using Input Registers	0.5		0.5		0.8		ns
t_{EABWO}	EAB WE to Data Output Delay		5.1		6.0		8.1	ns

10KE tbl 11A

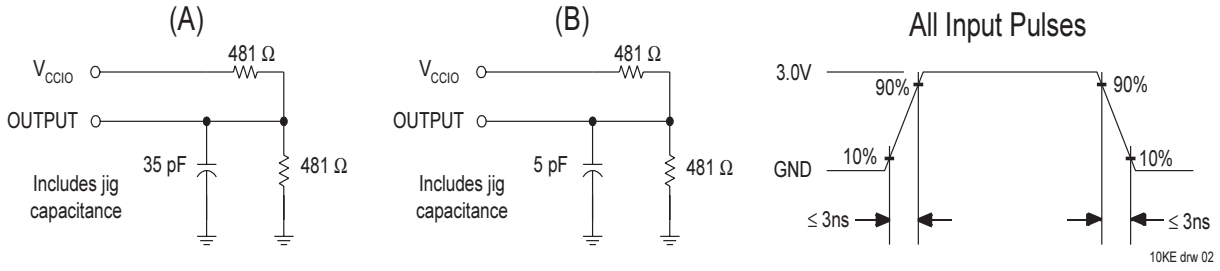
AC Electrical Specifications cont.

External Bidirectional Timing Parameters[5]

		Speed: -1		Speed: -2		Speed: -3		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
$t_{INSUBIDIR}$	Setup for Bi-directional Pins with Global Clock at Adjacent LE Registers	2.5		3.3		4.4		ns
$t_{INHBIDIR}$	Hold Time for Bi-directional Pins with Global Glock at Adjacent LE Registers	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$	Clock-to-output Delay for Bi-directional Pins with Global Clock at IOE Register	2.0	3.7	2.0	4.4	2.0	6.3	ns
$t_{XZBIDIR}$	Synchronous IOE Output Buffer Disable Delay	2.0	5.2	2.0	6.1	2.0	8.3	ns
$t_{ZXBIDIR}$	Synchronous IOE Output Buffer Disable Delay, Slow Slew Rate = off	2.0	4.7	2.0	5.6	2.0	8.1	ns

10KE tbl 12A

AC Test Conditions



A: Test fixture set-up A is for general testing.
B: Test fixture set-up B is for high Z testing ($t_{ZX\#}$).

Notes to Tables

1. During transitions, inputs may undershoot to -2.0V or overshoot to 5.75V for periods shorter than 20ns. Otherwise, minimum DC input voltage is -0.5V.

2. Device inputs may be driven before V_{CCINT} and V_{CCIO} are powered.

3. Typical values are at V_{CC} of 3.3 volts and ambient temperature of 25 ºC.

4. Guaranteed but not tested. Characterized initially, and after any design changes which may affect these parameters.

5. Internal timing delays are based on characterization, and cannot be explicitly tested. Internal timing parameters should be used for performance estimation only.

6. Use AC Test Conditions set-up B for these parameters.

Revision History

02 Dec. 2000: Created new document

Ordering Information

Part Number	Temperature Range	Package Type	Speed	Altera Equivalent
CL10K200SQC240-3	Commercial	240-pin Plastic QFP	-3	EPF10K200SQC240-3
CL10K200SQC240-2			-2	EPF10K200SQC240-2
CL10K200SQC240-2X*			-2	EPF10K200SQC240-2X
CL10K200SQC240-1			-1	EPF10K200SQC240-1
CL10K200SQC240-1X*			-1	EPF10K200SQC240-1X
CL10K200SRC240-3	Commercial	240-pin Power QFP	-3	EPF10K200SRC240-3
CL10K200SRC240-2			-2	EPF10K200SRC240-2
CL10K200SRC240-2X*			-2	EPF10K200SRC240-2X
CL10K200SRC240-1			-1	EPF10K200SRC240-1
CL10K200SRC240-1X*			-1	EPF10K200SRC240-1X
CL10K200SBC356-3	Commercial	356-pin SBGA	-3	EPF10K200SBC356-3
CL10K200SBC356-2			-2	EPF10K200SBC356-2
CL10K200SBC356-2X*			-2	EPF10K200SBC356-2X
CL10K200SBC356-1			-1	EPF10K200SBC356-1
CL10K200SBC356-1X*			-1	EPF10K200SBC356-1X
CL10K200SBI356-2	Industrial		-2	EPF10K200SBI356-2

10K200S tbl 02A

* Contact your local Clear Logic Representative for availability.

Ordering Information

Part Number	Temperature Range	Package Type	Speed	Altera Equivalent
CL10K200SQC240-3	Commercial	240-pin Plastic QFP	-3	EPF10K200SQC240-3
CL10K200SQC240-2			-2	EPF10K200SQC240-2
CL10K200SQC240-2X*			-2	EPF10K200SQC240-2X
CL10K200SQC240-1			-1	EPF10K200SQC240-1
CL10K200SQC240-1X*			-1	EPF10K200SQC240-1X
CL10K200SRC240-3	Commercial	240-pin Power QFP	-3	EPF10K200SRC240-3
CL10K200SRC240-2			-2	EPF10K200SRC240-2
CL10K200SRC240-2X*			-2	EPF10K200SRC240-2X
CL10K200SRC240-1			-1	EPF10K200SRC240-1
CL10K200SRC240-1X*			-1	EPF10K200SRC240-1X
CL10K200SBC356-3	Commercial	356-pin SBGA	-3	EPF10K200SBC356-3
CL10K200SBC356-2			-2	EPF10K200SBC356-2
CL10K200SBC356-2X*			-2	EPF10K200SBC356-2X
CL10K200SBC356-1			-1	EPF10K200SBC356-1
CL10K200SBC356-1X*			-1	EPF10K200SBC356-1X
CL10K200SBI356-2	Industrial		-2	EPF10K200SBI356-2

10K200S tbl 02A

* Contact your local Clear Logic Representative for availability.