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April 1st, 2010 Renesas Electronics Corporation

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MOS FIELD EFFECT TRANSISTOR

2SK3434

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK3434 is N-channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

• Super low on-state resistance

 $R_{DS(on)1} = 20 \text{ m}\Omega \text{ MAX. (Vgs} = 10 \text{ V, Ip} = 24 \text{ A)}$ $R_{DS(on)2} = 31 \text{ m}\Omega \text{ MAX. (Vgs} = 4.0 \text{ V, Ip} = 24 \text{ A)}$

- Low Ciss: Ciss = 2100 pF TYP.
- Built-in gate protection diode

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3434	TO-220AB
2SK3434-S	TO-262
2SK3434-ZJ	TO-263
2SK3434-Z	TO-220SMD ^{Note}

Note TO-220SMD package is produced only in Japan.

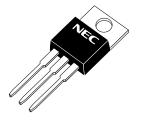
(TO-220AB)

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (Vgs = 0 V)	VDSS	60	V
Gate to Source Voltage (Vps = 0 V)	Vgss	±20	V
Drain Current (DC) (Tc = 25°C)	ID(DC)	±48	Α
Drain Current (pulse) Note1	ID(pulse)	±120	Α
Total Power Dissipation (Tc = 25°C)	Pτ	56	W
Total Power Dissipation (T _A = 25°C)	P⊤	1.5	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 to +150	°C
Single Avalanche Current Note2	las	28	Α
Single Avalanche Energy Note2	Eas	78	mJ

Notes 1. PW \leq 10 μ s, Duty cycle \leq 1%

2. Starting T_{ch} = 25°C, V_{DD} = 30 V, R_G = 25 Ω , V_{GS} = 20 \rightarrow 0 V



(TO-262)



(TO-263, TO-220SMD)



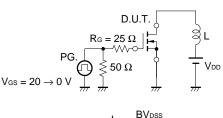
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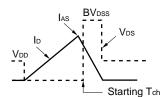


ELECTRICAL CHARACTERISTICS (TA = 25°C)

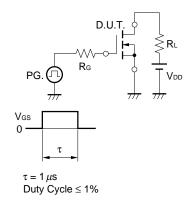
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Drain Current	Ipss	V _{DS} = 60 V, V _{GS} = 0 V			10	μΑ
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	yfs	V _{DS} = 10 V, I _D = 24 A	13	27		S
Drain to Source On-state Resistance	R _{DS(on)1}	Vgs = 10 V, ID = 24 A		16	20	mΩ
	R _{DS(on)2}	Vgs = 4.0 V, Ib = 24 A		22	31	mΩ
Input Capacitance	Ciss	V _{DS} = 10 V		2100		pF
Output Capacitance	Coss	V _G s = 0 V		340		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		170		pF
Turn-on Delay Time	td(on)	V _{DD} = 30 V, I _D = 24 A		40		ns
Rise Time	tr	V _G S = 10 V		400		ns
Turn-off Delay Time	t _{d(off)}	$R_G = 10 \Omega$		120		ns
Fall Time	tr			160		ns
Total Gate Charge	Q _G	V _{DD} = 48 V		40		nC
Gate to Source Charge	Qgs	Vgs = 10 V		7		nC
Gate to Drain Charge	Q _{GD}	ID = 48 A		11		nC
Body Diode Forward Voltage	V _F (S-D)	IF = 48 A, VGS = 0 V		1.0		V
Reverse Recovery Time	trr	IF = 48 A, VGS = 0 V		43		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		61		nC

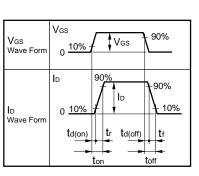
TEST CIRCUIT 1 AVALANCHE CAPABILITY



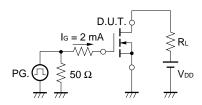


TEST CIRCUIT 2 SWITCHING TIME

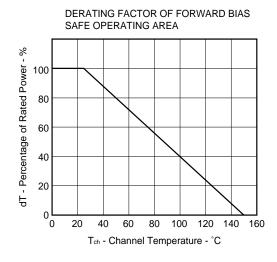


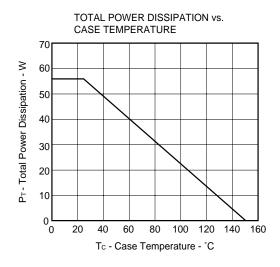


TEST CIRCUIT 3 GATE CHARGE

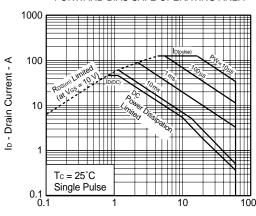


TYPICAL CHARACTERISTICS (TA = 25°C)



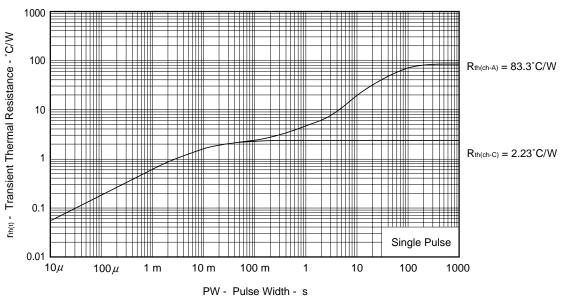


FORWARD BIAS SAFE OPERATING AREA

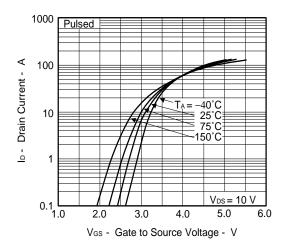


Vps - Drain to Source Voltage - V

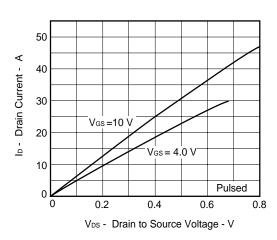
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



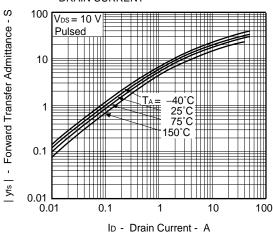
FORWARD TRANSFER CHARACTERISTICS



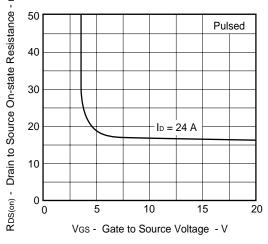
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

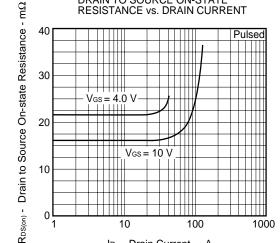


FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

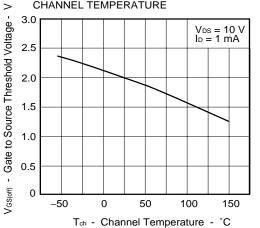




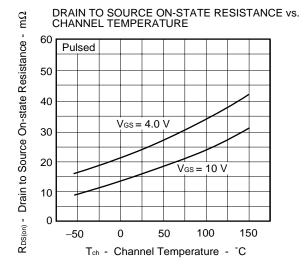
ID - Drain Current - A

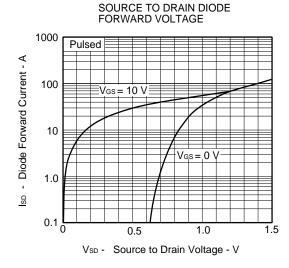
DRAIN TO SOURCE ON-STATE

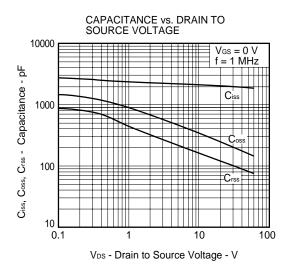
GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE

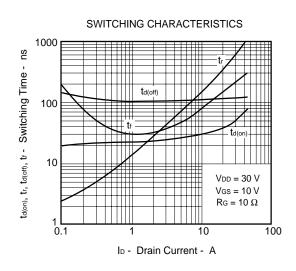


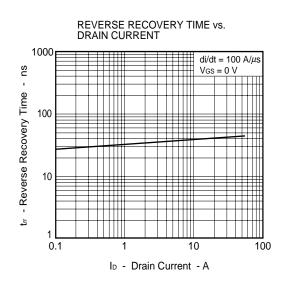


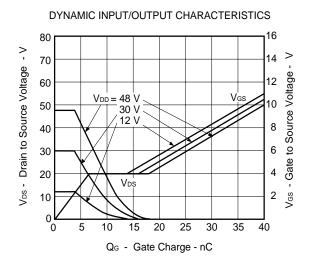


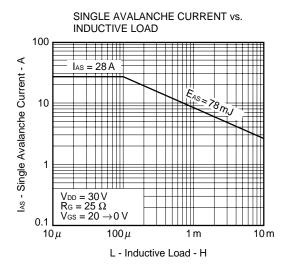


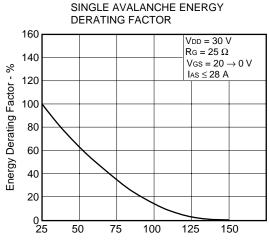






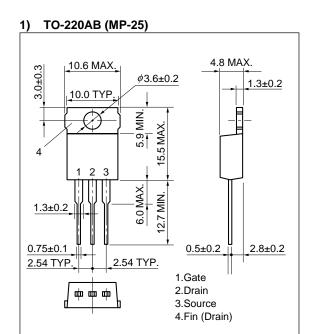


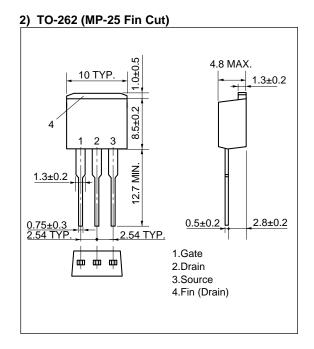




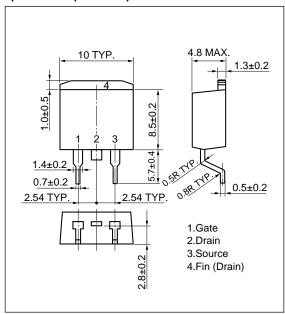
Starting T_{ch} - Starting Channel Temperature - $^{\circ}C$

★ PACKAGE DRAWINGS (Unit: mm)

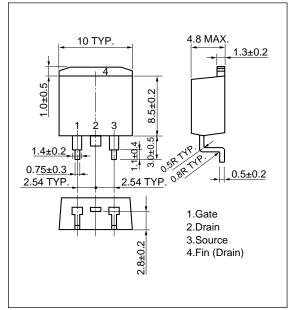




3) TO-263 (MP-25ZJ)

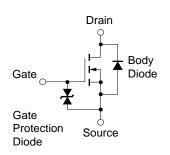


4) TO-220SMD (MP-25Z)^{Note}



Note This package is produced only in Japan.

EQUIVALENT CIRCUIT



Remark

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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