

Introduction

STMicroelectronics manufactures aerospace products at its European dedicated facility in Rennes (France), certified by the ESA-ESCC, DLA QML-V and DLA JANS systems.

In addition to the qualified products, often referred to as “flight parts”, ST proposes for most products (die - package combinations) an Engineering Model (EM) quality level, primarily intended to support development. The present document briefly describes the manufacturing and screening flow of this engineering model quality level.

1 Eligible products

Any ST aerospace qualified product can be proposed for the Engineering Model quality level, whether they are qualified in the ESCC, in the JANS or in the QML system.

The EM quality level is proposed by default for most die - package configurations, with some exceptions, mostly with legacy products and/or rare packages or pinout. Each product datasheet provides the details of the available EM^(a).

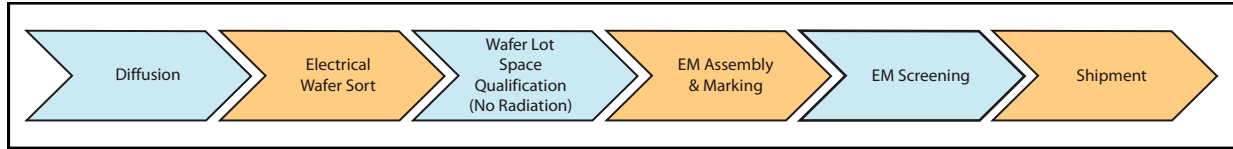
Non aerospace products may also be proposed for EM quality level, with some specific adjustments not discussed in this document.

a. Contact an ST sales office for die - package configurations not listed in the datasheets

2 Production flow

The EM overall simplified production flow is given in *Figure 1* below:

Figure 1. Simplified production flow



With respect to qualified flight models (FMs), EMs:

- use the same design and the same mask set.
- are diffused in the same diffusion line, using the same process.
- go through the same electrical wafer sort (EWS).
- are submitted to the same wafer lot qualification tests, but without radiation tests.
- are assembled on the same space assembly line, using the simplified process flowchart and control plan summarized below.
- use the same packages and piece parts (wires, lid, etc.)
- use the same dice (design, mask set, diffusion line, etc.)
- are not optically sorted.
- are guaranteed against the same ESCC/SMD electrical test tables, in particular, over the full temperature range test (guaranteed by characterization + 100% final test at 25 °C + go/no-go wafer lot qualification sampling at 3 temperatures).
- do not go through any package test (PIND test, thermal cycles, etc.)
- are provided with a specific marking, without agency logo, described in each product datasheet.
- are delivered only with gold-plated terminals.
- are provided with neither certificate of conformance nor traceability.

The simplified EM assembly and screening flow is summarized below:

- Die-attach
- Wire bonding
- Sealing
- Stabilization bake
- Fine/gross leak test
- Marking
- Electrical test go/no-go at 25 °C
- Packing

3 Revision history

Table 1. Document revision history

Date	Revision	Changes
30-May-2014	1	Initial release.

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