2A Single Cell Switchmode Li-Ion/Polymer Battery Charger with System Power-Path Selection and Automatic USB/Charger Detection

DESCRIPTION

The EUP8218 is a highly integrated single cell Li-ion and Li-polymer battery charger. It integrates a constant-frequency PWM controller with high accuracy regulation of input current, charge current, and voltage. It also provides battery detection, pre-conditioning, charge termination, and charge status monitoring.

The EUP8218 provides power path selection function. When the qualified adapter is present, the system is powered by the adapter. Otherwise, the system is powered by the battery. It also integrates an USB-connection-monitoring device used to determine if a standard USB device or a battery-charging device is connected.

The EUP8218 charges the battery in three phases: pre-conditioning, fast-charge constant current and constant voltage. In all stages, an internal control loop monitors the IC junction temperature and reduce charge current if the internal temperature threshold (120°C) is exceeded. Additionally, a battery pack thermistor monitoring input (TS) is included that monitors battery temperature for safety charging.

Charge is terminated when the current reaches 10% of the fast charge rate. A programmable charge timer offers a safety back up. The EUP8218 automatically restarts the charge cycle if the battery voltage falls below an internal threshold, and enters a low-quiescent current sleep mode when the input voltage falls below the battery voltage.

The EUP8218 features Dynamic Power Management (DPM) to reduce the charge current when the input power limit is reached to avoid over-loading the adapter. A highly-accurate current-sense amplifier enables precise measurement of input current from adapter to monitor overall system power.

The EUP8218 is available in a 28-pin, 4mm×4mm TQFN package.

FEATURES

- 4.5V-20V Input Operating Range
- High Integration
  - Automatic Power Path Selector Between Adapter and Battery
  - Automatic USB/Charger Detection
  - Dynamic Power Management
  - Integrated 20V High Side Switching MOSFET
- Safety
  - Thermal Regulation Loop Throttles Back Current to Limit Tj=120°C
  - Thermal Shutdown
  - Battery Thermistor Sense Hot/Cold Charge Suspend & Battery Detect
  - Input Over-Voltage Protection with Programmable Thereshold
- Accuracy
  - ±1% Charge Voltage Regulation
  - ±10% Charge Current Regulation
  - ±10% Input Current Regulation
- Less than 25µA Battery Current with Adapter Removed
- Less than 5mA Input Current with Adapter Present and Charge Disabled
- 4mm×4mm TQFN-28 Package
- RoHS Compliant and 100% Lead (Pb)-Free Halogen-Free

APPLICATIONS

- Mobile and Smart Phones
- Tablet PC
- Handheld Devices

Typical Application Circuit
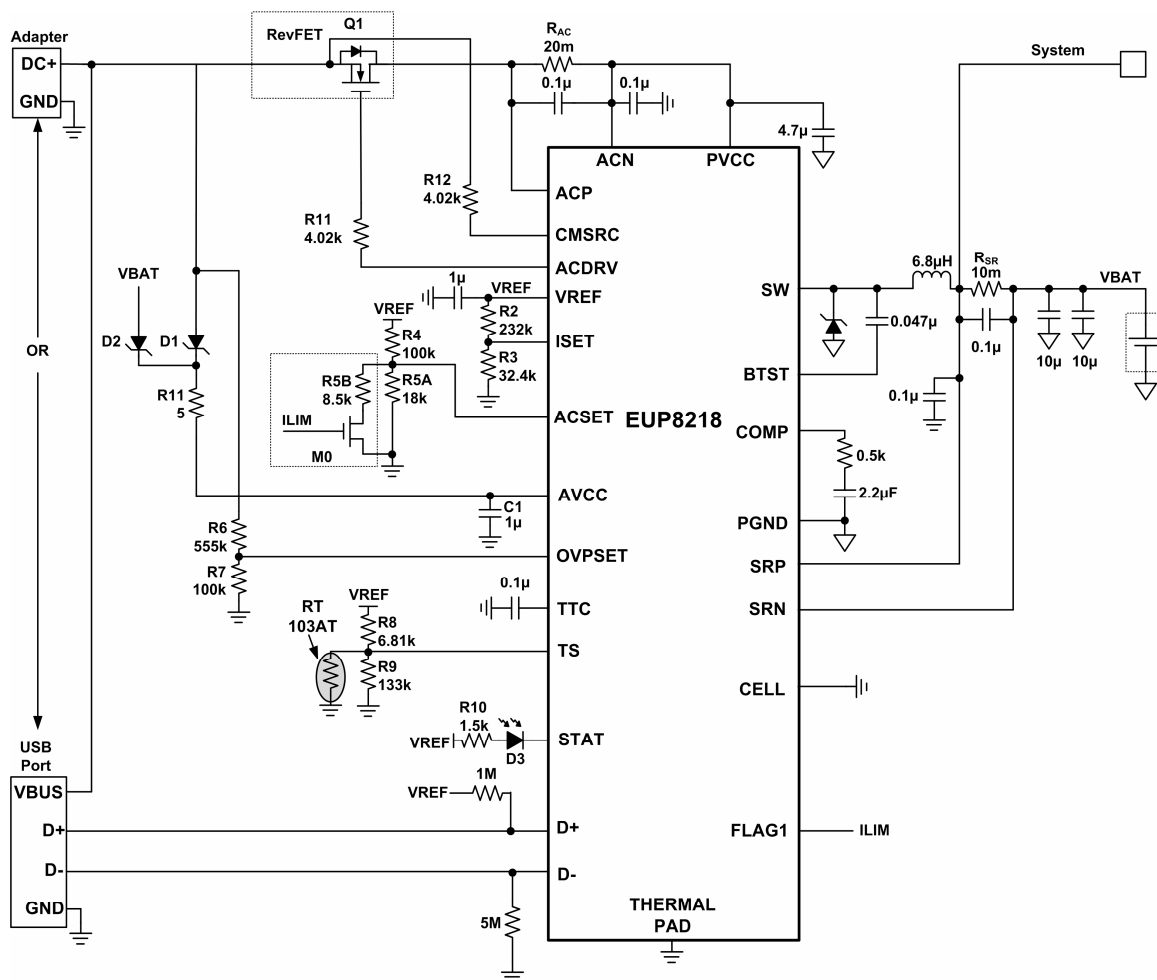
Figure 1. 1-Cell Typical Application Schematic with Single Cell Battery
(USB or adapter with input OVP 10.5V, 2A charge current, 0.2A pre-charge current,
2.5A adapter current or ILIM 0.9A limit current.R5B use 3.8k for 0.5A limit current.)
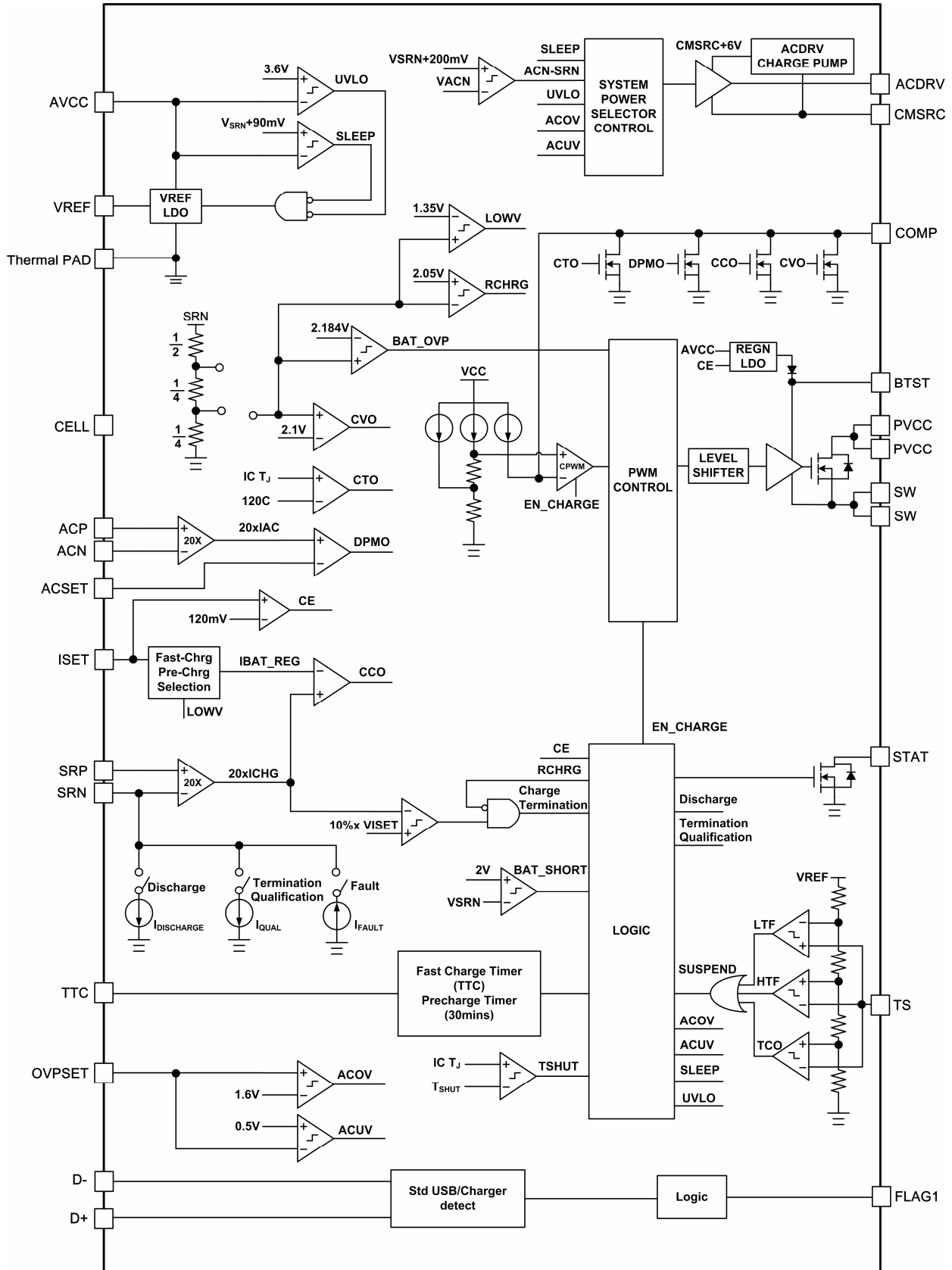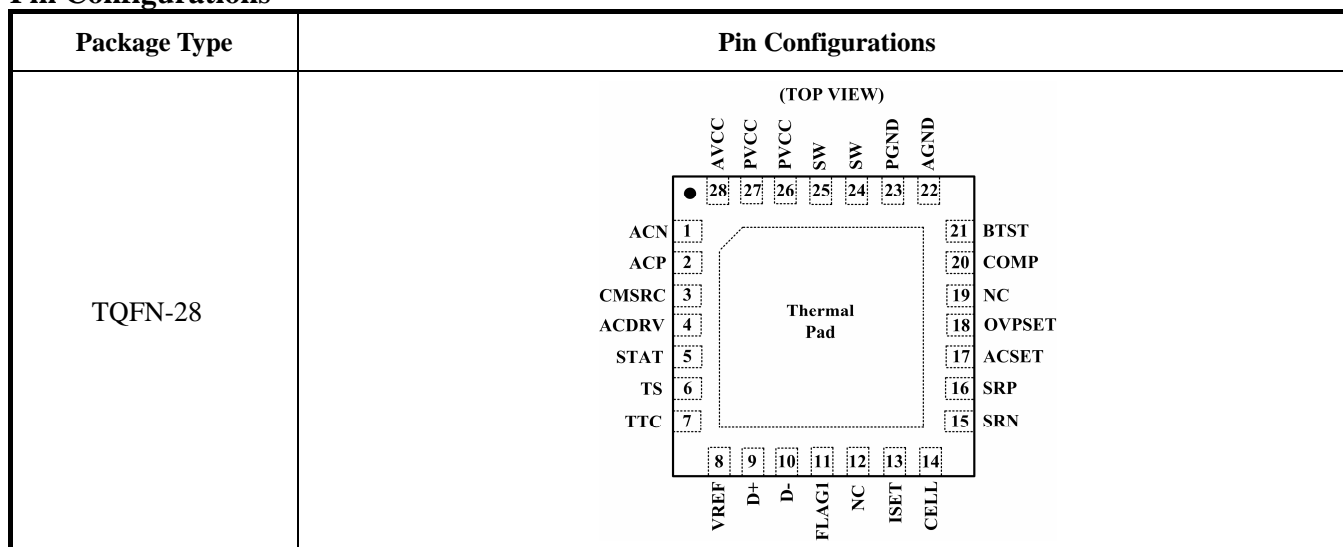
Block Diagram

Figure 2.

Pin Configurations

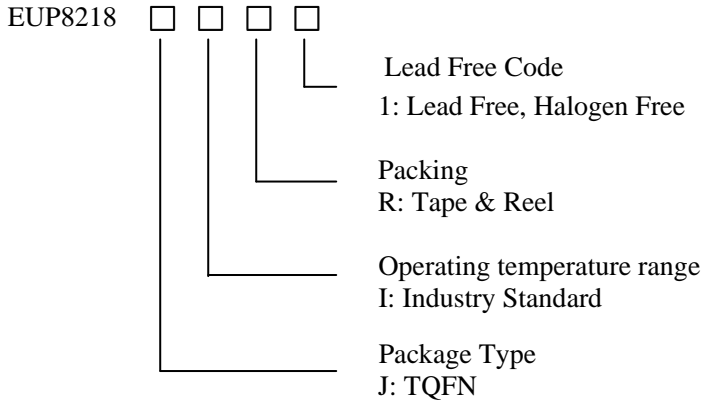| Package Type	Pin Configurations
TQFN-28	

Pin Description

PIN	TQFN-28	I/O/P	DESCRIPTION
ACN	1	I	Adapter current sense resistor negative input. A 0.1μF ceramic capacitor is placed from ACN to ACP to provide differential-mode filtering. An optional 0.1μF ceramic capacitor is placed from ACN pin to AGND for common-mode filtering.
ACP	2	P/I	Adapter current sense resistor positive input. A 0.1μF ceramic capacitor is placed from ACN to ACP to provide differential-mode filtering. A 0.1μF ceramic capacitor is placed from ACP pin to AGND for common-mode filtering.
CMSRC	3	O	Connect to the source of N-channel RevFET. Place 4kΩ resistor from CMSRC pin to the source of RevFET to control the turn-on speed.
ACDRV	4	O	AC adapter to PVCC switch driver output. Connect to 4kΩ resistor then to the gate of the RevFET N-channel power MOSFET.
STAT	5	O	Open-drain charge status pin with 1.5kΩ pull up to power rail. The STAT pin can be used to drive LED or communicate with the host processor. It indicates various charger operations: LOW when charge in progress. HIGH when charge is complete or in SLEEP mode. Blinking at 0.5Hz when fault occurs, including charge suspend, input over-voltage, timer fault and battery absent.
TS	6	I	Temperature qualification voltage input. Connect a negative temperature coefficient thermistor. Program the hot and cold temperature window with a resistor divider from VREF to TS to AGND. The temperature qualification window can be set to 5-40°C or wider. The 103AT thermistor is recommended.
TTC	7	O	Safety Timer and termination control. Connect a capacitor from this node to AGND to set the fast charge safety timer (5.6min/nF). Pre-charge timer is internally fixed to 30 minutes. Pull the TTC to LOW to disable the charge termination and safety timer. Pull the TTC to HIGH to disable the safety timer but allow the charge termination.
VREF	8	P	3.3V reference voltage output. Place a 1μF ceramic capacitor from VREF to AGND pin close to the IC. This voltage could be used for programming ISET and ACSET and TS pins. It may also serve as the pull-up rail of STAT pin and CELL pin.
D+	9	I	D+ and D- Connections for USB Input Adapter Detection-When a charge cycle is initiated by the USB input , and a short is detected between D+ and D- , the FLAG1 is low and the input current limit set by ACSET shall not change. If a short is not detected, the FLAG1 is high and the input current limit is changed to the predetermined USB2 or USB3 current limit.
D-	10	I	
FLAG1	11	O	Charger/standard USB device detect flag-When an USB charger is plugged in, the FLAG1 is low. While a standard USB device is plugged in, the FLAG is high.

Pin Description (continued)

PIN	TQFN-28	I/O/P	DESCRIPTION
ISET	13	I	Fast charge current set point. Use a voltage divider from VREF to ISET to AGND to set the fast charge current: $I_{CHG}=V_{ISET}/(20*R_{SR})$ The pre-charge and termination current is internally as one tenth of the charge current. The charger is disabled when ISET pin voltage is below 40mV and enabled when ISET pin voltage is above 120mV.
CELL	14	I	Cell selection pin. Set CELL pin LOW for 1-cell with a fixed 4.2V.
SRN	15	I	Battery Sense Input. A bypass capacitor of 20μF is required to minimize ripple voltage. When VBAT is within 90mV of AVCC, the EUP8218 is forced into sleep mode.
SRP	16	I/P	Current Amplifier Sense Input. A sense resistor, RSENSE, must be connected between the SRN and SRP pins.
ACSET	17	I	Input current set point. Use a voltage divider from VREF to ACSET to AGND to set this value: $I_{DPM}=V_{ACSET}/(20*R_{AC})$
OVPSET	18	I	Valid input voltage set point. Use a voltage divider from input to OVPSET to AGND to set this voltage. The voltage above internal 1.6V reference indicates input over-voltage, and the voltage below internal 0.5V reference indicates input under-voltage. LED driven by STAT pin keeps blinking, reporting fault condition.
COMP	20	O	Compensation, Soft-Start Pin. Charging begins when the COMP pin reaches 850mV. The recommended compensation components are a 2.2μF (or larger) capacitor and a 0.5k series resistor. A 100μA current into the compensation capacitor also sets the soft-start slew rate.
BTST	21	P	PWM high side driver positive supply.
AGND	22	P	Analog Ground.
PGND	23	P	Power ground. Ground connection for high-current power converter node. On PCB layout, connect directly to ground connection of input and output capacitors of the charger. Only connect to AGND through the Thermal Pad underneath the IC.
SW	24,25	P	Switching node, charge current output inductor connection. Connect the 0.047μF bootstrap capacitor from SW to BTST.
PVCC	26, 27	P	Charger input voltage. Connect at least 10μF ceramic capacitor from PVCC to PGND and place it as close as possible to IC.
AVCC	28	P/I	IC power positive supply. Place a 1μF ceramic capacitor from AVCC to AGND and place it as close as possible to IC. Place a 10Ω resistor from input side to AVCC pin to filter the noise. For 5V input, a 5Ω resistor is recommended.
NC	12,19		No connect
Thermal Pad	AGND	P	Exposed pad beneath the IC. Always solder Thermal Pad to the board, and have vias on the Thermal Pad plane star-connecting to AGND and ground plane for high-current power converter. It dissipates the heat from the IC.

Ordering Information

Order Number	Package Type	Marking	Operating Temperature Range
EUP8218JIR1	TQFN-28	xxxxx P8218	-40°C to +85°C

EUP8218 ☐ ☐ ☐ ☐

Lead Free Code
1: Lead Free, Halogen Free

Packing
R: Tape & Reel

Operating temperature range
I: Industry Standard

Package Type
J: TQFN

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Absolute Maximum Ratings (1)

- PVCC, AVCC, ACP, ACN,ACDRV, CMSRC,BTST,SRP, SRN------------------------------- -0.3V to 20V
- SW --- -2V to 20V
- OVPSET, TS,TTC, CELL, COMP, D+,D-,FLAG1 -- -0.3V to 7V
- VREF, ISET, ACSET, STAT -- -0.3V to 3.6V
- PGND, AGND --- -0.3V to 0.3V
- Maximum Difference Voltage, SRP-SRN, ACP-ACN ----------------------------------- -0.5V to 0.5V
- Package Thermal Resistance ,TQFN-28 ,θ_{JA} --- 40°C/W
- Junction temperature range, T_J --- 150°C
- Storage temperature range, Tstg -- -65°C to 150°C
- Lead temperature (soldering, 10s) --- 260°C

Recommended Operating Conditions (2)

		Min.	Max.	Unit
Input voltage	V_{IN}	4.5	20	V
Output voltage	V_{OUT}		4.5	V
Output current (R_{SR} 10mΩ)	I_{OUT}	0.5	4	A
Maximum difference voltage	ACP-ACN	-200	200	mV
	SRP-SRN	-200	200	mV
Ambient Temperature Range , T_A		-40	85	°C

Note (1): Stress beyond those listed under "Absolute Maximum Ratings" may damage the device.
Note (2): The device is not guaranteed to function outside the recommended operating conditions.

Electrical Characteristics

4.5V ≤V(PVCC, AVCC) ≤20V, –40°C < T_J <+ 125°C, typical values are at T_A = 25°C, with respect to AGND (unless otherwise noted).

Symbol	Parameter	Conditions	EUP8218 Min.	Typ.	Max.	Unit
OPERATING CONDITIONS						
V_{AVCC_OP}	AVCC input voltage operating range during charging		4.5		20	V
QUIESCENT CURRENTS						
I_{BAT}	Battery discharge current (sum of currents into AVCC, PVCC, ACP, ACN)	$V_{AVCC} > V_{UVLO}$, $V_{SRN} > V_{AVCC}$ (SLEEP), T_J = 0°C to 85°C			25	µA
		BTST, SW, SRP, SRN, $V_{AVCC} > V_{UVLO}$, $V_{AVCC} > V_{SRN}$, ISET < 40mV, V_{BAT}=4.2V, Charge disabled			25	
		BTST, SW, SRP, SRN, $V_{AVCC} > V_{UVLO}$, $V_{AVCC} > V_{SRN}$, ISET > 120mV, V_{BAT}=4.2V, Charge done			25	
I_{AC}	Adapter supply current (sum of current into AVCC,ACP, ACN)	$V_{AVCC} > V_{UVLO}$, $V_{AVCC} > V_{SRN}$, ISET < 40mV, V_{BAT}=4.2V, Charge disabled		2.5	5	m A
		$V_{AVCC} > V_{UVLO}$, $V_{AVCC} > V_{SRN}$, ISET > 120mV, Charge enabled, no switching		2.5	5	
		$V_{AVCC} > V_{UVLO}$, $V_{AVCC} > V_{SRN}$, ISET > 120mV, Charge enabled, switching		15		

Electrical Characteristics (continued)

$4.5V \leq V(PVCC, AVCC) \leq 20V$, $-40°C < T_J < +125°C$, typical values are at $T_A = 25°C$, with respect to AGND (unless otherwise noted).

Symbol	Parameter	Conditions	EUP8218			Unit
			Min.	Typ.	Max.	
CHARGE VOLTAGE REGULATION						
V_{BAT_REG}	SRN regulation voltage	CELL to AGND, measured on SRN		4.2		V
	Charge voltage regulation accuracy	$T_J = 0°C$ to 85°C	–1%		1%	
CURRENT REGULATION —FAST CHARGE						
V_{ISET}	ISET Voltage Range	$RSENSE = 10m\Omega$	0.12		0.8	V
K_{ISET}	Charge Current Set Factor (Amps of Charge Current per Volt on ISET pin)	$RSENSE = 10m\Omega$		5		A/V
	ChargeCurrent Regulation Accuracy (with Schottky diode on SW)	$V_{SRP-SRN} = 20$ mV	-10%		10%	
V_{ISET_CD}	Charge Disable Threshold	ISET falling	40	50		mV
V_{ISET_CE}	Charge Enable Threshold	ISET rising		100	120	mV
I_{ISET}	Leakage Current into ISET	VISET = 2V			100	nA
INPUT CURRENT REGULATION						
K_{DPM}	Input DPM Current Set Factor (Amps of Input Current per Volt on ACSET)	$RSENSE = 10m\Omega$		5		A/V
	Input DPM Current Regulation Accuracy (with Schottky diode on SW)	$V_{ACP-ACN} = 60$ mV	-10%		10%	
I_{ACSET}	Leakage Current into ACSET pin	VACSET = 2V			100	nA
CURRENT REGULATION – PRE-CHARGE						
$K_{IPRECHG}$	Precharge current set factor	Percentage of fast charge current		10%		
CHARGE TERMINATION						
K_{TERM}	Termination current set factor	Percentage of fast charge current		10%		
t_{TERM_DEG}	Deglitch time for termination (both edges)			100		ms
t_{QUAL}	Termination qualification time	$V_{SRN} > V_{RECH}$ and $I_{CHG} < I_{TERM}$		250		ms
I_{QUAL}	Termination qualification current	Discharge current once termination is detected		2		mA
INPUT UNDER-VOLTAGE LOCK-OUT COMPARATOR (UVLO)						
V_{UVLO}	AC under-voltage rising threshold	Measure on AVCC	3.4	3.6	3.9	V
V_{UVLO_HYS}	AC under-voltage hysteresis, falling	Measure on AVCC		300		mV
SLEEP COMPARATOR (REVERSE DISCHARGING PROTECTION)						
V_{SLEEP}	SLEEP mode threshold	$V_{AVCC} - V_{SRN}$ falling	30	90	150	mV
V_{SLEEP_HYS}	SLEEP mode hysteresis	$V_{AVCC} - V_{SRN}$ rising		200		mV
$t_{SLEEP\_FALL\_CD}$	SLEEP deglitch to disable charge	$V_{AVCC} - V_{SRN}$ falling		1		ms

Electrical Characteristics (continued)

4.5V $\leq$ V(PVCC, AVCC) $\leq$ 20V, $-40°C < T_J < + 125°C$, typical values are at $T_A = 25°C$, with respect to AGND (unless otherwise noted).

Symbol	Parameter	Conditions	EUP8218			Unit
			Min.	Typ.	Max.	
SLEEP COMPARATOR (REVERSE DISCHARGING PROTECTION)						
$t_{SLEEP\_FALL\_FETOFF}$	SLEEP deglitch to turn off input FETs	$V_{AVCC} - V_{SRN}$ falling		5		ms
t_{SLEEP_FALL}	Deglitch to enter SLEEP mode, disable VREF and enter low quiescent mode	$V_{AVCC} - V_{SRN}$ falling		100		ms
t_{SLEEP_PWRUP}	Deglitch to exit SLEEP mode, and enable VREF	$V_{AVCC} - V_{SRN}$ rising		30		ms
BAT LOWV COMPARATOR						
V_{LOWV}	Precharge to fast charge transition	CELL to AGND, measure on SRN	2.85	2.9	2.95	V
V_{LOWV_HYS}	Fast charge to precharge hysteresis	CELL to AGND, measure on SRN		200		mV
$t_{pre\_to\_fas}$	VLOWV rising deglitch	Delay to start fast charge current		25		ms
$t_{fast\_to\_pre}$	VLOWV falling deglitch	Delay to start precharge current		25		ms
RECHARGE COMPARATOR						
V_{RECHG}	Recharge Threshold, below regulation voltage limit, VBAT_REG-VSRN	CELL to AGND, measure on SRN	70	100	130	mV
$t_{RECH\_RISE\_DEG}$	VRECHG rising deglitch	V_{SRN} decreasing below VRECHG		10		ms
$t_{RECH\_FALL\_DEG}$	VRECHG falling deglitch	V_{SRN} increasing above VRECHG		10		ms
BAT OVER-VOLTAGE COMPARATOR						
V_{OV_RISE}	Over-voltage rising threshold	As percentage of V_{BAT_REG}		104%		
V_{OV_FALL}	Over-voltage falling threshold	As percentage of V_{SRN}		102%		
INPUT OVER-VOLTAGE COMPARATOR (ACOV)						
V_{ACOV}	AC Over-Voltage Rising Threshold to turn off RevFET	OVPSET rising	1.55	1.6	1.65	V
V_{ACOV_HYS}	AC over-voltage falling hysteresis	OVPSET falling		50		mV
$t_{ACOV\_RISE\_DEG}$	AC Over-Voltage Rising Deglitch to turn off RevFET and Disable Charge	OVPSET rising		1		µs
$t_{ACOV\_FALL\_DEG}$	AC Over-Voltage Falling Deglitch to Turn on RevFET	OVPSET falling		30		ms
INPUT UNDER-VOLTAGE COMPARATOR (ACUV)						
V_{ACUV}	AC Under-Voltage Falling Threshold to turn off RevFET	OVPSET falling	0.45	0.5	0.55	V
V_{ACUV_HYS}	AC Under-Voltage Rising Hysteresis	OVPSET rising		100		mV

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Electrical Characteristics (continued)

$4.5V \leq V(PVCC, AVCC) \leq 20V$, $-40°C < T_J < +125°C$, typical values are at $T_A = 25°C$, with respect to AGND (unless otherwise noted).

Symbol	Parameter	Conditions	EUP8218			Unit
			Min.	Typ.	Max.	
INPUT UNDER-VOLTAGE COMPARATOR (ACUV)						
$t_{ACOV\_FALL\_DEG}$	AC Under-Voltage Falling Deglitch to turn off RevFET and Disable Charge	OVPSET falling		1		µs
$t_{ACOV\_RISE\_DEG}$	AC Under-Voltage Rising Deglitch to turn on RevFET	OVPSET rising		30		ms
THERMAL REGULATION						
T_{J_REG}	Junction Temperature Regulation Accuracy	ISET > 120mV, Charging		120		°C
T_{SHUT}	Thermal shutdown rising temperature	Temperature rising		150		°C
THERMAL SHUTDOWN COMPARATOR						
$t_{SHUT\_RISE\_DEG}$	Thermal shutdown rising deglitch	Temperature rising		100		µs
$t_{SHUT\_FALL\_DEG}$	Thermal shutdown falling deglitch	Temperature falling		10		ms
THERMISTOR COMPARATOR						
V_{LTF}	Cold Temperature Threshold, TS pin Voltage Rising Threshold	Charger suspends charge. As percentage to V_{VREF}	71.5%	73.5%	75.5%	
V_{LTF_HYS}	Cold Temperature Hysteresis, TS pin Voltage Falling	As percentage to V_{VREF}		0.4%		
V_{HTF}	Hot Temperature TS pin voltage rising Threshold	As percentage to V_{VREF}	45.6%	47.2%	49.8%	
V_{TCO}	Cut-off Temperature TS pin voltage falling Threshold	As percentage to V_{VREF}	43.2%	44.7%	46.2%	
$t_{TS\_CHG\_SUS}$	Deglitch time for Temperature Out of Range Detection	$V_{TS} > V_{LTF}$, or $V_{TS} < _{VTCO}$, or $V_{TS} < _{VHTF}$		20		ms
$t_{TS\_CHG\_RESUME}$	Deglitch time for Temperature in Valid Range Detection	$V_{TS} < V_{LTF} - V_{LTF\_HYS}$ or $V_{TS} > V_{TCO}$, or $V_{TS} => V_{HTF}$		400		ms
CHARGE OVER-CURRENT COMPARATOR (CYCLE-BY-CYCLE)						
V_{OCP_CHRG}	Charge Over-Current Rising Threshold, VSRP>2.2V	Current as percentage of fast charge current		160%		
BAT SHORT COMPARATOR						
V_{BATSHT}	Battery short falling threshold	Measure on SRN		2		V
V_{BATSHT_HYS}	Battery short rising hysteresis	Measure on SRN		200		mV
t_{BATSHT_DEG}	Deglitch on both edges			1		µs
V_{BATSHT}	Charge Current during BATSHORT	Percentage of fast charge current		10%		
VREF REGULATOR						
V_{VREF_REG}	VREF regulator voltage	$V_{AVCC} > V_{UVLO}$, No load	3.267	3.3	3.333	V
I_{VREF_LIM}	VREF current limit	$V_{VREF} = 0$ V, $V_{AVCC} > V_{UVLO}$	35		90	mA

Electrical Characteristics (continued)

$4.5V \leq V(\text{PVCC, AVCC}) \leq 20V$, $-40°C < T_J < +125°C$, typical values are at $T_A = 25°C$, with respect to AGND (unless otherwise noted).

Symbol	Parameter	Conditions	EUP8218			Unit
			Min.	Typ.	Max.	
TTC INPUT						
$t_{prechrg}$	Precharge Safety Timer	Precharge time before fault occurs	1620	1800	1980	Sec
$t_{fastchrg}$	Fast Charge Timer Range	$T_{chg} = C_{TTC} * K_{TTC}$	1		10	hr
	Fast Charge Timer Accuracy		-10%		10%	
K_{TTC}	Timer Multiplier			5.6		min /nF
V_{TTC_LOW}	TTC Low Threshold	TTC falling			0.4	V
I_{TTC}	TTC Source/Sink Current		45	50	55	µA
$V_{TTC\_OSC\_HI}$	TTC oscillator high threshold			1.5		V
$V_{TTC\_OSC\_LO}$	TTC oscillator low threshold			1		V
AC SWITCH (RevFET) DRIVER						
V_{ACDRV_REG}	Gate Drive Voltage on RevFET	$V_{ACDRV} - V_{CMSRC}$ when $V_{AVCC} > V_{UVLO}$		4		V
BATTERY DETECTION						
t_{WAKE}	Wake timer	Max time charge is enabled		500		ms
I_{WAKE}	Wake current	$RSENSE = 10\ m\Omega$	50	125	200	m A
$t_{DISCHARGE}$	Discharge timer	Max time discharge current is applied		1		sec
$I_{DISCHARGE}$	Discharge current			8		m A
I_{FAULT}	Fault current after a timeout fault			2		m A
V_{WAKE}	Wake threshold with respect to VREG To detect battery absent during WAKE	Measure on SRN		100		mV/cell
V_{DISCH}	Discharge Threshold to detect battery absent during discharge	Measure on SRN		2.9		V/cell
INTERNAL PWM						
fsw	PWM Switching Frequency		450	500	550	kHz
CHARGER SECTION POWER-UP SEQUENCING						
t_{CE_DELAY}	Delay from ISET above 120mV to start charging battery			1.5		s
LOGIC IO PIN CHARACTERISTICS						
V_{OUT_LO}	STAT Output Low Saturation Voltage	Sink Current = 5mA			0.5	V
LOGIC IO PIN CHARACTERISTICS						
V_{CELL_LO}	CELL pin input low threshold, 1 cell	CELL pin voltage falling edge			0.5	V
INPUT CHARACTERISTICS						
$I_{off}\ D+$	Off Leakage Current	D+=5V			1	µA
$I_{off}\ D-$	Off Leakage Current	D-=5V			1	µA
OUTPUT CHARACTERISTICS						
$V_{OL}\ FLAG1$	Maximum LOW Output Voltage	$V_{AVCC}=5V$, $I_{OL}=20µA$			0.3	V

Electrical Characteristics (continued)

$4.5V \leq V(PVCC, AVCC) \leq 20V$, $-40°C < T_J < +125°C$, typical values are at $T_A = 25°C$, with respect to AGND (unless otherwise noted).

Symbol	Parameter	Conditions	EUP8218			Unit
			Min.	Typ.	Max.	
OUTPUT CHARACTERISTICS						
D+/D- Threshold			1.025	1.300	1.400	V
t_{off}	Flag1 HIGH to LOW	100pF Load		10		ns
t_{on}	Flag1 LOW to HIGH	100pF Load		50		ns

Truth Table

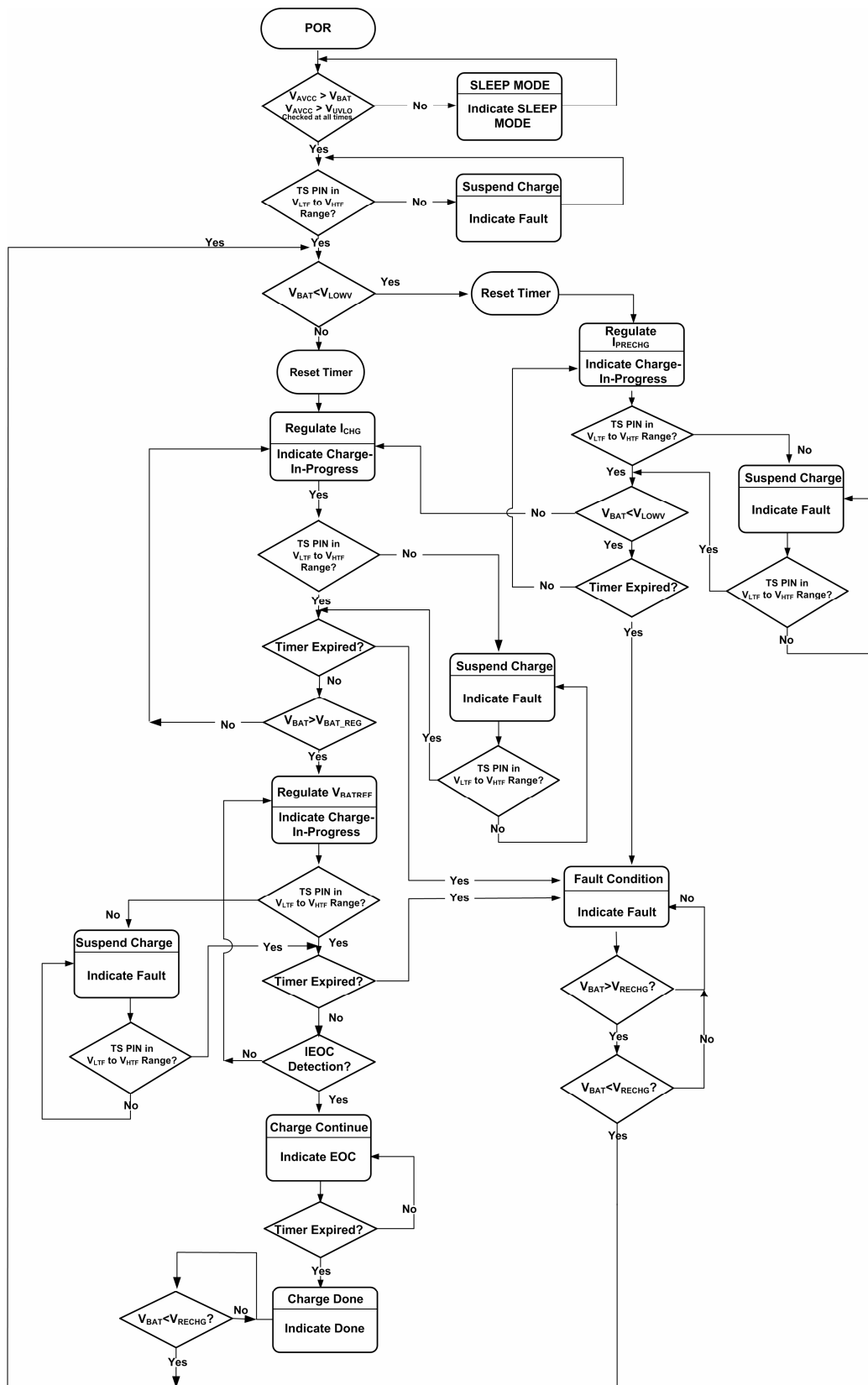| Connection State	V_{AVCC}	D-	D+	FLAG1
STD USB Device	5V	R to Gnd	R to V_{REF}	HIGH
USB Charger	5V	Short to D+	Short to D-	LOW

Operational Flow Chart

Figure 3.

FUNCTIONAL DESCRIPTION

Battery Current Regulation

The ISET input sets the maximum charging current. Battery current is sensed by current sensing resistor RSR connected between SRP and SRN. The full-scale differential voltage between SRP and SRN is 40mV max. The equation for charge current is:

$$I_{CHARGE} = \frac{V_{ISET}}{20 \times R_{SR}} \qquad (1)$$

The valid input voltage range of ISET is up to 0.8V. With 10mΩ sense resistor, the maximum output current is 4A. With 20mΩ sense resistor, the maximum output current is 2A.

The charger is disabled when ISET pin voltage is below 40mV and is enabled when ISET pin voltage is above 120mV. For 10mΩ current sensing resistor, the minimum fast charge current must be higher than 600mA.

Under high ambient temperature, the charge current will fold back to keep IC temperature not exceeding 120°C.

Battery Precharge Current Regulation

On Power-up, if the battery voltage is below the VLOWV threshold, the EUP8218 applies the pre-charge current to the battery. This pre-charge feature is intended to revive deeply discharged cells. If the VLOWV threshold is not reached within 30 minutes of initiating pre-charge, the charger turns off and a FAULT is indicated on the status pins.

For EUP8218, the pre-charge current is set as 10% of the fast charge rate set by ISET voltage.

$$I_{PRECHARGE} = \frac{V_{ISET}}{200 \times R_{SR}} \qquad (2)$$

Input Current Regulation

The total input current from an AC adapter or other DC sources is a function of the system supply current and the battery charging current. System current normally fluctuated as portions of the systems are powered up or down. Without Dynamic Power Management (DPM), the source must be able to supply the maximum system current and the maximum available charger input current simultaneously. By using DPM, the input current regulator reduces the charging current when the summation of system power and charge power exceeds the maximum input power. Therefore, the current capability of the AC adapter can be lowered, reducing system cost.

Input current is set by the voltage on ACSET pin using the following equation:

$$I_{DPM} = \frac{V_{ACSET}}{20 \times R_{AC}} \qquad (3)$$

The ACP and ACN pins are used to sense across RAC with default value of 20mΩ. However, resistors of other values can also be used. A larger sense resistor will give a larger sense voltage and higher regulation accuracy, at the expense of higher conduction loss.

Charge Termination, Recharge, and Safety Timers

The charger monitors the charging current during the voltage regulation phase. Termination is detected when the SRN voltage is higher than recharge threshold and the charge current is less than the termination current threshold, as calculated below:

$$I_{TERM} = \frac{V_{ISET}}{200 \times R_{SR}} \qquad (4)$$

where V_{ISET} is the voltage on the ISET pin and RSR is the sense resistor. There is a 25ms deglitch time during transition between fast-charge and pre-charge.

As a safety backup, the charger also provides an internal fixed 30 minutes pre-charge safety timer and a programmable fast charge timer. The fast charge time is programmed by the capacitor connected between the TTC pin and AGND, and is given by the formula:

$$t_{TTC} = C_{TTC} \times K_{TTC} \qquad (5)$$

Where C_{TTC} is the capacitor connected to TTC and K_{TTC} is the constant multiplier.

A new charge cycle is initiated when one of the following conditions occurs:
• The battery voltage falls below the recharge threshold
• A power-on-reset (POR) event occurs
• ISET pin toggled below 40mV (disable charge) and above 120mV (enable charge)

Pull TTC pin to AGND to disable both termination and fast charge safety timer (reset timer). Pull TTC pin to VREF to disable the safety timer, but allow charge termination.

Power Up

The charge uses a SLEEP comparator to determine the source of power on the AVCC pin, since AVCC can be supplied either from the battery or the adapter. With the adapter source present, if the AVCC voltage is greater than the SRN voltage, the charger exits SLEEP mode. If all conditions are met for charging, the charger then starts charge the battery (see ***the Enabling and Disabling Charging*** section). If SRN voltage is greater than AVCC, the charger enters low quiescent current SLEEP mode to minimize current drain from the battery. During SLEEP mode, the VREF output turns off and the STAT pin goes to high impedance.

If AVCC is below the UVLO threshold, the device is disabled.

Input Under-Voltage Lock-Out (UVLO)

The system must have a minimum AVCC voltage to allow proper operation. This AVCC voltage could come from either input adapter or battery, since a conduction path exists from the battery to AVCC through D2. When AVCC is below the UVLO threshold, all circuits on the IC are disabled.

Input Over-Voltage/Under-Voltage Protection

ACOV provides protection to prevent system damage due to high input voltage. In EUP8218, once the voltage on OVPSET is above the 1.6V ACOV threshold or below the 0.5V ACUV threshold, charge is disabled and input MOSFETs turn off. The EUP8218 provides flexibility to set the input qualification threshold.

Enable and Disable Charging

The following conditions have to be valid before charging is enabled:
• ISET pin above 120mV
•Device is not in Under-Voltage-Lock-Out (UVLO) mode (i.e. $V_{AVCC} > V_{UVLO}$)
• Device is not in SLEEP mode (i.e. $V_{AVCC} > V_{SRN}$)
• OVPSET voltage is between 0.5V and 1.6V to qualify the adapter
• 1.5s delay is complete after initial power-up
• VREF LDO voltages are at correct levels
• Thermal Shut down (TSHUT) is not valid
• TS fault is not detected
• RevFET turns on (See *System Power Selector* for details)
One of the following conditions stops on-going charging:
• ISET pin voltage is below 40mV
• Device is in UVLO mode
• Adapter is removed, causing the device to enter SLEEP mode
• OVPSET voltage indicates the adapter is not valid
• VREF LDO voltage is overloaded
• TSHUT temperature threshold is reached
• TS voltage goes out of range indicating the battery temperature is too hot or too cold
• RevFET turns off
• TTC timer expires or pre-charge timer expires

System Power Selector

The IC automatically switches adapter or battery power to the system load. The battery is connected to the system by default during power up or during SLEEP mode. When the adapter plugs in and the voltage is above the battery voltage, the IC exits SLEEP mode, the adapter supply the system and battery. When the adapter is absent, the battery supply the system.

The ACDRV is used to drive a n-channel power MOSFETs between adapter and ACP. The n-channel FET with the drain connected to the ACP (Q1) provides reverse battery discharge protection, and minimizes system power dissipation with its low-RDS$_{ON}$.

Converter Operation

The EUP8218 employs a 500KHz constant-frequency step-down switching regulator. The fixed frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current, and temperature, simplifying output filter design and keeping it out of the audible noise region.

Both the current loop and the voltage loop share a common, high impedance, compensation node (COMP pin). A series capacitor and resistor on this pin compensates both loops. The resistor is included to provide a zero in the loop response and boost the phase margin. The compensation capacitor also provides a soft-start function for the charger. Upon start-up, then ramp at a rate set by the internal 100μA pullup current source and the external capacitor. Battery charge current starts ramping up when the COMP pin voltage reaches 0.85V. With a 2.2μF capacitor, time to start charge is about 18ms. Capacitance can be increased if a longer start-up time is needed.

Charge Over-Current Protection

The charger monitors top side MOSFET current by high side sense FET. When peak current exceeds MOSFET limit, it will turn off the top side MOSFET and keep it off until the next cycle. The charger has a secondary cycle-to-cycle over-current protection. It monitors the charge current, and prevents the current from exceeding 160% of the programmed charge current. The high-side gate drive turns off when either over-current condition is detected, and automatically resumes when the current falls below the over-current threshold.

Charge Under-Current Protection

After the recharge, if the SRP-SRN voltage decreases below 5mV, the low side FET will be turned off for the rest of the switching cycle. During discontinuous conduction mode (DCM), the low side FET will only turn on for a short period of time when high side FET turn on every four times to provide refresh charge for the capacitor. This is important to prevent negative inductor current from causing any boost effect in which the input voltage increases as power is transferred from the battery to the input capacitors. This can lead to an over-voltage on the AVCC node and potentially cause damage to the system.

Battery Detection

For applications with removable battery packs, IC provides a battery absent detection scheme to reliably detect insertion or removal of battery packs. The battery detection routine runs on power up, or if battery voltage falls below recharge threshold voltage due to removing a battery or discharging a battery.
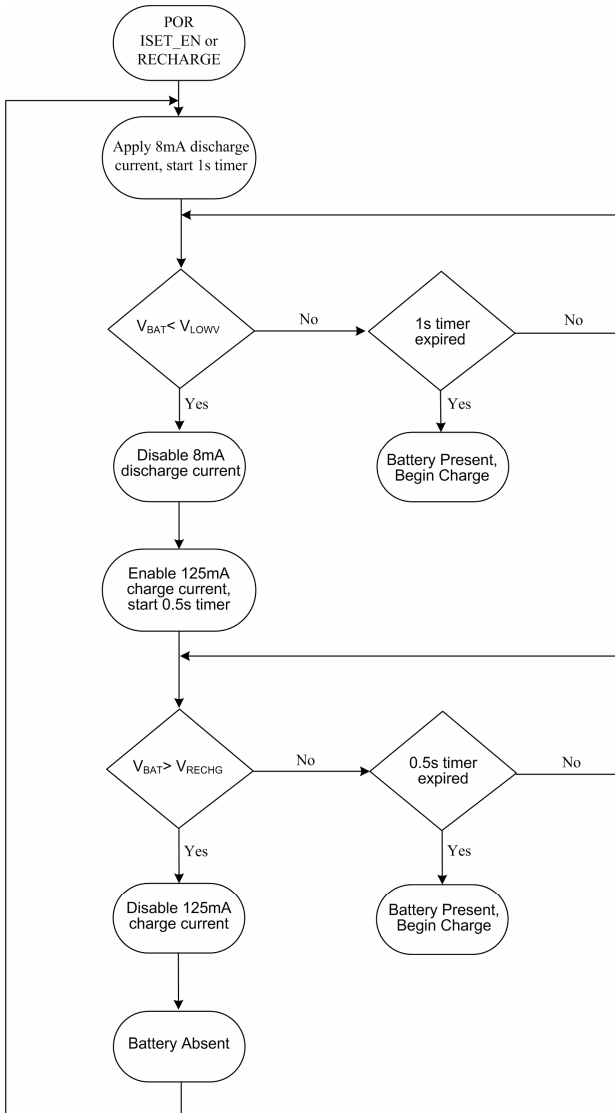
Figure 4.

Once the device has powered up, a 8-mA discharge current is applied to the SRN terminal. If the battery voltage falls below the LOWV threshold within 1 second, the discharge source is turned off, and the charger is turned on at low charge current (125mA). If the battery voltage gets up above the recharge threshold within 500ms, there is no battery present and the cycle restarts. If either the 500ms or 1 second timer time out before the respective thresholds are hit, a battery is detected and a charge cycle is initiated.
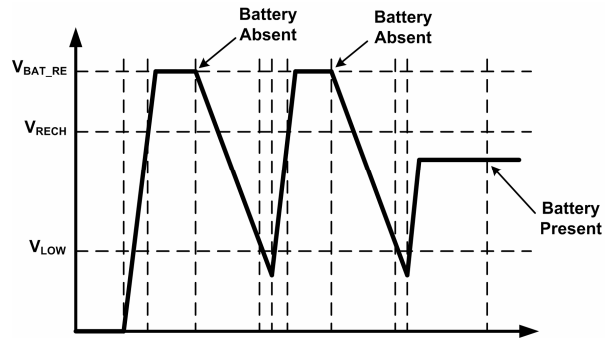

Figure 5. Battery Detect Timing Diagram

Care must be taken that the total output capacitance at the battery node is not so large that the discharge current source cannot pull the voltage below the LOWV threshold during the 1 second discharge time. The maximum output capacitances can be calculated according to the following equations:

$$C_{MAX} = \frac{I_{DISCH} \times t_{DISCH}}{4.1V - 2.9V} \qquad (6)$$

Where C_{MAX} is the maximum output capacitance, IDISCH is the discharge current, t_{DISCH} is the discharge time.

Battery Short Protection

When SRN pin voltage is lower than 2V it is considered as battery short condition during charging period. The charger will shut down immediately for 1ms, then soft start back to the charging current the same as precharge current. This prevents high current may build in output inductor and cause inductor saturation when battery terminal is shorted during charging. The converter works in non-synchronous mode during battery short.

Battery Over-Voltage Protection

The converter will not allow the high-side FET to turn-on until the battery voltage goes below 102% of the regulation voltage. This allows one-cycle response to an over-voltage condition – such as occurs when the load is removed or the battery is disconnected. A total 6mA current sink from SRP/SRN to AGND allows discharging the stored output inductor energy that is transferred to the output capacitors. If battery over-voltage condition lasts for more than 30ms, charge is disabled.

Temperature Qualification

The controller continuously monitors battery temperature by measuring the voltage between the TS pin and AGND. A negative temperature coefficient thermistor (NTC) and an external voltage divider typically develop this voltage. The controller compares this voltage against its internal thresholds to determine if charging is allowed.

To initiate a charge cycle, the battery temperature must be within the V_{LTF} to V_{HTF} thresholds. If battery temperature is outside of this range, the controller

suspends charge and waits until the battery temperature is within the V_{LTF} to V_{HTF} range. During the charge cycle the battery temperature must be within the V_{LTF} to V_{TCO} thresholds. If battery temperature is outside of this range, the controller suspends charge and waits until the battery temperature is within the V_{LTF} to V_{HTF} range. The controller suspends charge by turning off the PWM charge MOSFETss. Figure 6 summarizes the operation.
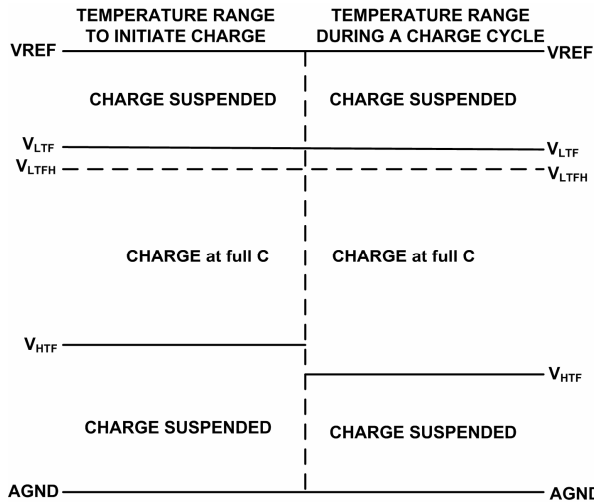

Figure 6.

Assuming a 103AT NTC thermistor on the battery pack as shown in Figure 7, the values of RT1 and RT2 can be determined by using Equation 7 and Equation 8:

$$RT2 = \frac{V_{VREF} \times RTH_{COLD} \times RTH_{HOT} \times \left(\dfrac{1}{v_{LTF}} - \dfrac{1}{v_{TCO}} \right)}{RTH_{HOT} \times \left(\dfrac{V_{VREF}}{v_{TCO}} - 1 \right) - RTH_{COLD} \times \left(\dfrac{V_{VREF}}{v_{LTF}} - 1 \right)}$$

(7)

$$RT1 = \frac{\dfrac{V_{VREF}}{V_{LTF}} - 1}{\dfrac{1}{RT2} + \dfrac{1}{RTH_{COLD}}}$$

(8)

Select 0°C to 45°C range for Li-ion or Li-polymer battery,
RTH_{COLD} = 27.28 kΩ
RTH_{HOT} = 4.911 kΩ
RT1 = 5.23 kΩ
RT2 = 30.1 kΩ

After select closest standard resistor value, by calculating the thermistor resistance at temperature threshold, the final temperature range can be gotten from thermistor datasheet temperature-resistance table.
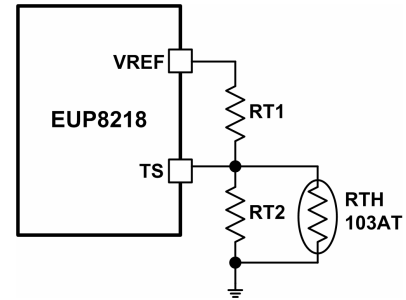

Figure 7. TS Resistor Network

MOSFET Short Circuit and Inductor Short Circuit Protection

The IC has a short circuit protection feature. Its cycle-by-cycle current monitoring feature is achieved through monitoring the voltage drop across Rdson of the MOSFETs. The charger will be latched off, but the RevFET keep on to power the system. The only way to reset the charger from latch-off status is remove adapter then plug adapter in again. Meanwhile, STAT is blinking to report the fault condition.

Thermal Regulation and Shutdown Protection

The TQFN package has low thermal impedance, which provides good thermal conduction from the silicon to the ambient, to keep junctions temperatures low. The internal thermal regulation loop will fold back the charge current to keep the junction temperature from exceeding 120°C. As added level of protection, the charger converter turns off and self-protects whenever the junction temperature exceeds the TSHUT threshold of 150°C.

The charger stays off until the junction temperature falls below 130°C.

Timer Fault Recovery

The IC provides a recovery method to deal with timer fault conditions. The following summarizes this method:

Condition 1: The battery voltage is above the recharge threshold and a timeout fault occurs.

Recovery Method: The timer fault will clear when the battery voltage falls below the recharge threshold, and battery detection will begin. A POR or taking ISET below 40mV will also clear the fault.

Condition 2: The battery voltage is below the recharge threshold and a timeout fault occurs.

Recovery Method: Under this scenario, the IC applies the fault current to the battery. This small current is used to detect a battery removal condition and remains on as long as the battery voltage stays below the recharge threshold. If the battery voltage goes above the recharge threshold, the IC disabled the fault current and executes the recovery method described in Condition 1. A POR or taking ISET below 40mV will also clear the fault.

Charge Status Outputs

The open-drain STAT outputs indicate various charger operations as listed in Table 1. These status pins can be used to drive LEDs or communicate with the host processor. Note that OFF indicates that the open-drain transistor is turned off.

Table 1. STAT Pin Definition

Charge State	STAT
Charge in progress (including recharging)	ON
Charge complete, Sleep mode, Charge disabled	OFF
Charge suspend, Input over-voltage, Battery over-voltage, timer fault, , battery absent, OTP, TS-FAULT, OCP_HSFET	BLINK

USB/Charger Detection

EUP8218 sets the FLAG1 pin to high or low to indicate whether a standard USB device or a charger is connected to the USB port. The D- line connects a 5M pull-down resistor to ground and D+ line connects a 1M push-up resistor to VREF.

When a condition exists where a charger is plugged into the USB port (D+/D- short), the voltage divider of 1M and 5M comes out a voltage of 2.75V on the D+/D- inputs. This makes FLAG1 low, indicating a charger is connected to USB port. In this condition, M0 (as shown in Figure1 at page2) is not turn on, and the input current limit set by ACSET shall not change.

In a condition where a standard USB device is plugged into the USB port, the D+ input is pull up to VREF and D- input is pull low, which makes FLAG1 high. In this condition, M0 is turn on, the voltage of ACSET changes accordingly. The input limit current is changed to a predetermined USB2 or USB3 limit current which can be set by Resistor R5B (as shown in Figure1 at Page 2).

Inductor, Capacitor, and Sense Resistor Selection Guidelines

Table 2 provides a summary of typical LC components for various charge currents.

Table 2. Typical Values as a Function of Charge Current

Charge Current	1A	2A	3A	4A
Output inductor L	6.8μH	6.8μH	3.3μH	2.2μH
Output capacitor C	10μF	20μF	20μF	30μF

APPLICATION INFORMATION

Inductor Selection

The EUP8218 has a 500-kHz switching frequency to allow the use of small inductor and capacitor values. Inductor saturation current should be higher than the charging current (I_{CHG}) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} \geq I_{CHG} + (1/2)I_{RIPPLE} \qquad (9)$$

Inductor ripple current depends on input voltage (V_{IN}), duty cycle ($D = V_{OUT}/V_{IN}$), switching frequency (fs), and inductance (L):

$$I_{RIPPLE} = \frac{V_{IN} \times D \times (1-D)}{fs \times L} \qquad (10)$$

The maximum inductor ripple current happens with D = 0.5 or close to 0.5. Usually inductor ripple is designed in the range of 20% to 40% of the maximum charging current as a trade-off between inductor size and efficiency for a practical design.

Inductor Capacitor

The input capacitor should have enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current ICIN occurs where the duty cycle is closest to 50% and can be estimated by the following equation:

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1-D)} \qquad (11)$$

A low ESR ceramic capacitor such as X7R or X5R is preferred for the input decoupling capacitor and should be placed as close as possible to the drain of the high-side MOSFET and source of the low-side MOSFET. The voltage rating of the capacitor must be higher than the normal input voltage level. A 25V rating or higher capacitor is preferred for a 15V input voltage. A 20μF capacitance is suggested for a typical 3A to 4A charging current.

Output Capacitor

The output capacitor also should have enough ripple current rating to absorb output switching ripple current. The output capacitor RMS current ICOUT is given as:

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \qquad (12)$$

The output capacitor voltage ripple can be calculated as follows:

$$\Delta V_O = \frac{V_{OUT}}{8LCfs^2}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \qquad (13)$$

At certain input/output voltages and switching frequencies, the voltage ripple can be reduced by increasing the output filter LC.

The EUP8218 has an internal loop compensator. To achieve good loop stability, the resonant frequency of the output inductor and output capacitor should be designed between 15 kHz and 25 kHz. The preferred ceramic capacitor has a 25V or higher rating, X7R or X5R.

Input Filter Design

During adapter hot plug-in, the parasitic inductance and the input capacitor from the adapter cable form a second order system. The voltage spike at the AVCC pin may be beyond the IC maximum voltage rating and damage the IC. The input filter must be carefully designed and tested to prevent an over-voltage event on the AVCC pin.

There are several methods to damping or limiting the over-voltage spike during adapter hot plug-in. An electrolytic capacitor with high ESR as an input capacitor can damp the over-voltage spike well below the IC maximum pin voltage rating. A high current capability TVS Zener diode can also limit the over-voltage level to an IC safe level. However, these two solutions may not be lowest cost or smallest size.

A cost effective and small size solution is shown in Figure 8. R1 and C1 are composed of a damping RC network to damp the hot plug-in oscillation. As a result, the over-voltage spike is limited to a safe level. D1 is used for reverse voltage protection for the AVCC pin. C2 is the AVCC pin decoupling capacitor and it should be placed as close as possible to the AVCC pin. R2 and C2 form a damping RC network to further protect the IC from high dv/dt and high voltage spike. The C2 value should be less than the C1 value so R1 can dominant the equivalent ESR value to get enough damping effect for hot plug-in. R1 and R2 must be sized enough to handle in-rush current power loss according to the resistor manufacturer's datasheet. The filter component values always need to be verified with a real application and minor adjustments may be needed to fit in the real application circuit.
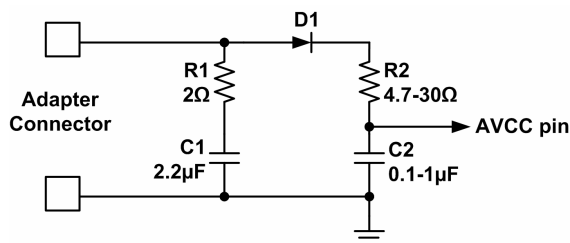
Input RevFET

N-type MOSFETs are used as input RevFET(Q1) for better cost effective and small size solution,as shown in Figure 9. There is a surge current during Q1 turn-on period when a valid adapter is inserted. Decreasing the turn-on speed of Q1 can limit this surge current in desirable range by selecting a MOSFET with relative bigger C_{GD} and/or C_{GS}. At the case Q1 turn on too fast, we need add external C_{GD} and/or C_{GS}. For example, 4.7nF C_{GD} and 47nF C_{GS} are adopted on EVM while using NexFET CSD17313 as Q1.
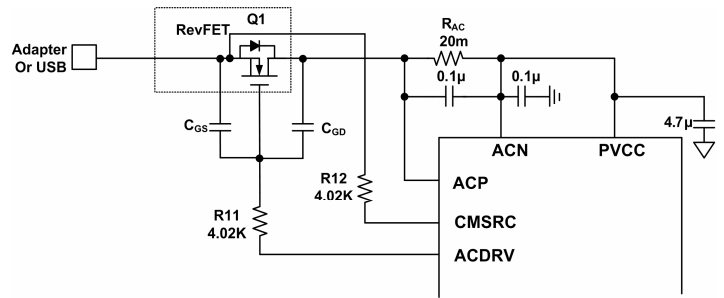
Figure 9. Input RevFET

Figure 8. Input Filter

Packaging Information

TQFN-28
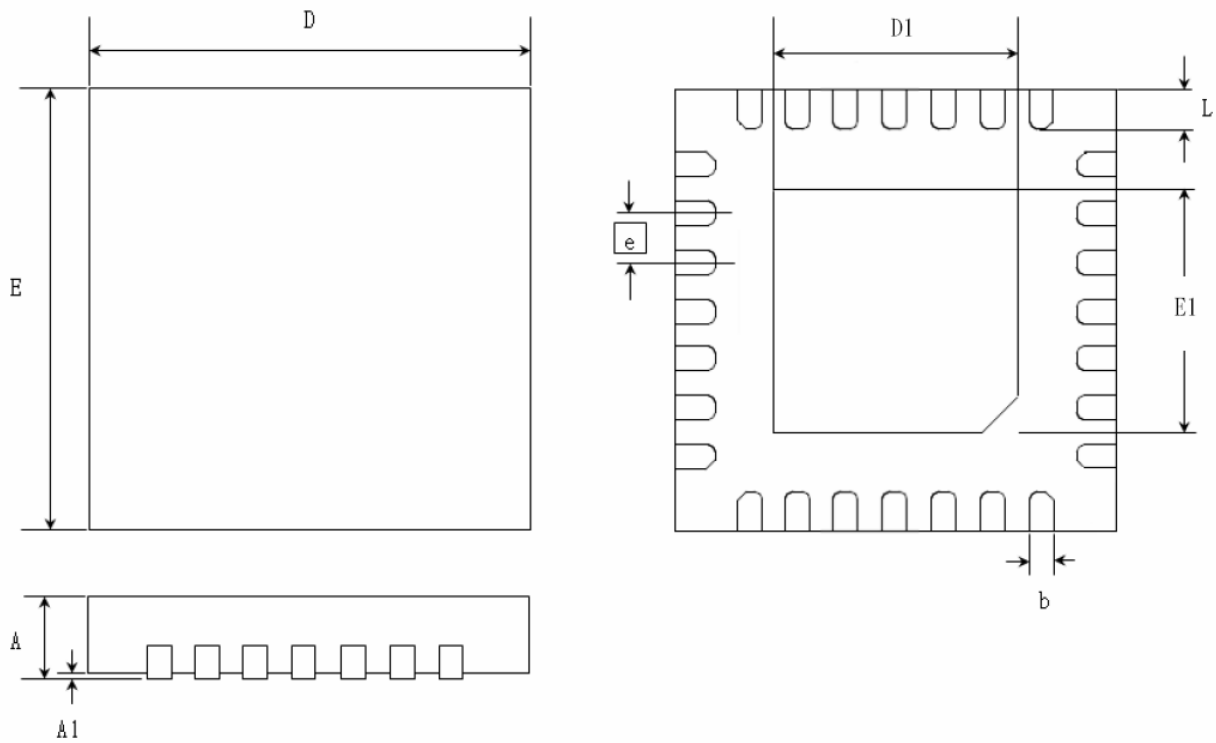
SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
b	0.15	0.25	0.006	0.010
E	3.90	4.10	0.154	0.162
D	3.90	4.10	0.154	0.162
D1	1.90	2.65	0.075	0.104
E1	1.90	2.65	0.075	0.104
e	0.40 BSC		0.016 BSC	
L	0.30	0.50	0.012	0.020