REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R338-97.	97-09-30	Monica L. Poelking
B	Changes in accordance with NOR 5962-R049-99.	99-04-05	Monica L. Poelking
C	Update boilerplate to MIL-PRF-38535 and updated appendix A. Editorial changes throughout. – tmh	00-07-17	Monica L. Poelking
D	Update boilerplate to MIL-PRF-38535 requirements and update the radiation hardness assurance boilerplate paragraphs. - LTG	08-01-23	Thomas M. Hess

REV																				
SHEET																				
REV	D	D	D	D	D	D	D	D	D	D										
SHEET	15	16	17	18	19	20	21	22	23	24										

REV STATUS	REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Thanh V. Nguyen

DEFENSE SUPPLY CENTER COLUMBUS
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Thanh V. Nguyen

APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
96-03-25

REVISION LEVEL
D

MICROCIRCUIT, DIGITAL, RADIATION HARDENED ADVANCED CMOS, DUAL D FLIP-FLOP WITH SET AND RESET, MONOLITHIC SILICON

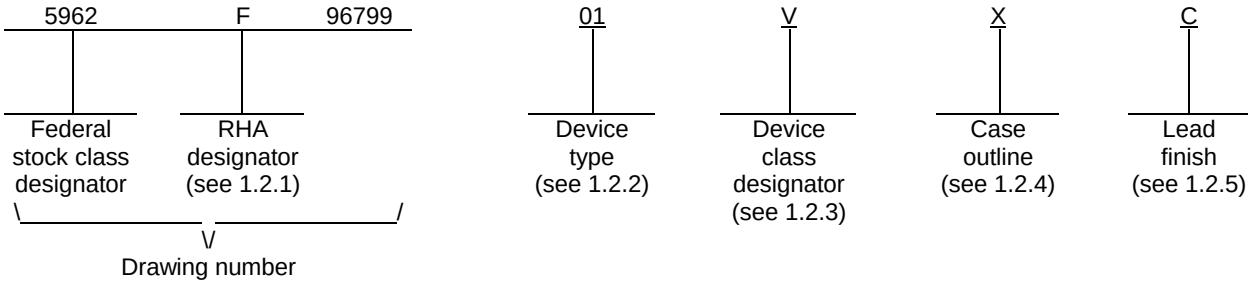
SIZE	CAGE CODE	
A	**67268**	**5962-96799**

SHEET 1 OF 24

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ACS74	Radiation hardened SOS, advanced CMOS, dual D flip-flop with set and reset
02	ACS74-02 1/	Radiation hardened SOS, advanced CMOS, dual D flip-flop with set and reset

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line
X	GDFP1-T14 or CDFP3-F14	14	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ Device type -02 is the same as device type -01 except that the device type -02 products are manufactured at an overseas wafer foundry. Device type -02 is used to positively identify, by marketing part number and by brand of the actual device, material that is supplied by an overseas foundry.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CC}) ..... -0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN}) ..... -0.5 V dc to V_{CC} + 0.5 V dc
DC output voltage range (V_{OUT}) ..... -0.5 V dc to V_{CC} + 0.5 V dc
DC input current, any one input (I_{IN}) ..... ±10 mA
DC output current, any one output (I_{OUT}) ..... ±50 mA
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Lead temperature (soldering, 10 seconds) ..... +265°C
Thermal resistance, junction-to-case (θ_{JC}):
  Case outline C ..... 24°C/W
  Case outline X ..... 30°C/W
Thermal resistance, junction-to-ambient (θ_{JA}):
  Case outline C ..... 74°C/W
  Case outline X ..... 116°C/W
Junction temperature (T_J) ..... +175°C
Maximum package power dissipation at T_A = +125°C (P_D): 4/
  Case outline C ..... 0.68 W
  Case outline X ..... 0.43 W

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V_{CC}) ..... +4.5 V dc to +5.5 V dc
Input voltage range (V_{IN}) ..... +0.0 V dc to V_{CC}
Output voltage range (V_{OUT}) ..... +0.0 V dc to V_{CC}
Maximum low level input voltage (V_{IL}) ..... 30% of V_{CC}
Minimum high level input voltage (V_{IH}) ..... 70% of V_{CC}
Case operating temperature range (T_C) ..... -55°C to +125°C
Maximum input rise or fall time at V_{CC} = 4.5 V (t_r, t_f) ..... 10 ns/V

1.5 Radiation features.

Total dose ..... > 3 x 10^5 Rads (Si)
Single event phenomenon (SEP) effective
  linear energy threshold (LET) no upsets (see 4.4.4.4) ..... > 100 MeV/(cm^2/mg) 5/
Dose rate upset (20 ns pulse) ..... > 1 x 10^{11} Rads (Si)/s 5/
Latch-up ..... None 5/
Dose rate survivability ..... > 1 x 10^{12} Rads (Si)/s 5/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise specified, all voltages are referenced to GND.
3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C unless otherwise noted.
4/ If device power exceeds package dissipation capability, provide heat sinking or derate linearly (the derating is based on θ_{JA}) at the following rate:
  Case C ..... 13.5 mW/°C
  Case X ..... 8.6 mW/°C
5/ Limits are guaranteed by design or process, but not production tested unless specified by the customer through the purchase order or contract.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation or contract.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM F1192- Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Copies of this document is available online at http://www.astm.org/ or from ASTM International, P. O. Box C700, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.1.1 Microcircuit die. For the requirements for microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.2.6 Irradiation test connections. The irradiation test connections shall be as specified in table III.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 38 (see MIL-PRF-38535, appendix A).

TABLE IA. Electrical performance characteristics.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	V_{CC}	Group A subgroups	Limits 2/		Unit
						Min	Max	
High level output voltage	V_{OH}	For all inputs affecting output under test V_{IN} = 3.15 V or 1.35 V For all other inputs V_{IN} = V_{CC} or GND I_{OH} = -50 µA	All	4.5 V	1, 2, 3	4.40		V
		M, D, P, L, R, F 3/	All		1	4.40		
		For all inputs affecting output under test V_{IN} = 3.85 V or 1.65 V For all other inputs V_{IN} = V_{CC} or GND I_{OH} = -50 µA	All	5.5 V	1, 2, 3	5.40		
		M, D, P, L, R, F 3/	All		1	5.40		
Low level output voltage	V_{OL}	For all inputs affecting output under test V_{IN} = 3.15 V or 1.35 V For all other inputs V_{IN} = V_{CC} or GND I_{OL} = 50 µA	All	4.5 V	1, 2, 3		0.1	V
		M, D, P, L, R, F 3/	All		1		0.1	
		For all inputs affecting output under test V_{IN} = 3.85 V or 1.65 V For all other inputs V_{IN} = V_{CC} or GND I_{OL} = 50 µA	All	5.5 V	1, 2, 3		0.1	
		M, D, P, L, R, F 3/	All		1		0.1	
Input current high	I_{IH}	For input under test, V_{IN} = 5.5 V For all other inputs V_{IN} = V_{CC} or GND	All	5.5 V	1		+0.5	µA
					2, 3		+1.0	
		M, D, P, L, R, F 3/	All		1		+1.0	
Input current low	I_{IL}	For input under test, V_{IN} = GND For all other inputs V_{IN} = V_{CC} or GND	All	5.5 V	1		-0.5	µA
					2, 3		-1.0	
		M, D, P, L, R, F 3/	All		1		-1.0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified		Device type	V_{CC}	Group A subgroups	Limits 2/		Unit
							Min	Max	
Output current high (Source)	I_{OH} 4/	For all inputs affecting output under test, V_{IN} = 4.5 V or 0.0 V		All	4.5 V	1	-12.0		mA
						2, 3	-8.0		
		V_{OUT} = 4.1 V	M, D, P, L, R, F 3/	All		1	-8.0		
Output current low (Sink)	I_{OL} 4/	For all inputs affecting output under test, V_{IN} = 4.5 V or 0.0 V		All	4.5 V	1	12.0		mA
						2, 3	8.0		
		V_{OUT} = 0.4 V	M, D, P, L, R, F 3/	All		1	8.0		
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		All	5.5 V	1		10.0	µA
						2, 3		200.0	
			M, D, P, L, R, F 3/	All		1		200.0	
Input capacitance	C_{IN}	V_{IH} = 5.0 V, V_{IL} = 0.0 V f = 1 MHz, see 4.4.1c		All	5.0 V	4		10	pF
Power dissipation capacitance	C_{PD} 5/			All	5.0 V	4		65	pF
						5, 6		75	
Functional test	6/	V_{IH} = 3.15 V, V_{IL} = 1.35 V		All	4.5 V	7, 8	L	H	
		See 4.4.1b	M, D, P, L, R, F 3/	All		7	L	H	
Propagation delay time, nCP to nQ or nQ	t_{PLH1} 7/	C_L = 50 pF R_L = 500Ω See figure 4		All	4.5 V	9	1.0	18.0	ns
						10, 11	1.0	20.0	
			M, D, P, L, R, F 3/	All		9	1.0	20.0	
	t_{PHL1} 7/	C_L = 50 pF R_L = 500Ω See figure 4		All	4.5 V	9	1.0	15.0	
						10, 11	1.0	18.0	
			M, D, P, L, R, F 3/	All		9	1.0	18.0	
Propagation delay time, $\overline{nS}$ to nQ	t_{PLH2} 7/	C_L = 50 pF R_L = 500Ω See figure 4		All	4.5 V	9	1.0	13.0	ns
						10, 11	1.0	16.0	
			M, D, P, L, R, F 3/	All		9	1.0	16.0	
Propagation delay time, $\overline{nS}$ to nQ	t_{PHL2} 7/	C_L = 50 pF R_L = 500Ω See figure 4		All	4.5 V	9	1.0	14.0	ns
						10, 11	1.0	17.0	
			M, D, P, L, R, F 3/	All		9	1.0	17.0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	V_{CC}	Group A subgroups	Limits 2/		Unit
						Min	Max	
Propagation delay time, nR to $\overline{nQ}$	t_{PLH3} 7/	C_L = 50 pF R_L = 500Ω See figure 4	All	4.5 V	9	1.0	12.0	ns
					10, 11	1.0	14.0	
		M, D, P, L, R, F 3/	All		9	1.0	14.0	
Propagation delay time, nR to nQ	t_{PHL3} 7/	C_L = 50 pF R_L = 500Ω See figure 4	All	4.5 V	9	1.0	14.0	ns
					10, 11	1.0	17.0	
		M, D, P, L, R, F 3/	All		9	1.0	17.0	
Output transition time	t_{THL}, t_{TLH} 7/	C_L = 50 pF R_L = 500Ω See figure 4	All	4.5 V	9	1.0	11.0	ns
					10, 11	1.0	12.0	
		M, D, P, L, R, F 3/	All		9	1.0	12.0	
Maximum clock frequency	f_{MAX} 8/	C_L = 50 pF R_L = 500Ω See figure 4	All	4.5 V	9	79.0		MHz
					10, 11	76.0		
Setup time, high or low, nD to nCP	t_s 8/		All	4.5 V	9	4.3		ns
					10, 11	4.9		
Hold time, high or low, nD to nCP	t_h 8/		All	4.5 V	9	2.0		ns
					10, 11	2.0		
$\overline{nR}$ or $\overline{nS}$ pulse width, low	t_{w1} 8/		All	4.5 V	9	5.5		ns
					10, 11	6.3		
nCP pulse width, high or low	t_{w2} 8/		All	4.5 V	9	5.5		ns
					10, 11	6.3		
Recovery time, $\overline{nR}$ or $\overline{nS}$ to nCP	t_{REC} 8/		All	4.5 V	9	3.7		ns
					10, 11	3.7		

1/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table IA herein. Output terminals not designated shall be high level logic, low level logic, or open, except for the I_{CC} test, the output terminals shall be open. When performing the I_{CC} test, the current meter shall be placed in the circuit such that all current flows through the meter.

2/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.

3/ RHA devices supplied to this drawing have been characterized through all levels M, D, P, L, R, and F of irradiation. However, this device is only tested at the 'F' level. Pre and Post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

4/ Force/Measure functions may be interchanged.

TABLE IA. Electrical performance characteristics - Continued.

5/ Power dissipation capacitance (C_{PD}) determines both the power consumption (P_D) and current consumption (I_S). Where
$P_D = (C_{PD} + C_L) (V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC})$
$I_S = (C_{PD} + C_L) V_{CC}f + I_{CC}$
f is the frequency of the input signal.

6/ The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. For V_{OUT} measurements, $L \leq 0.5$ V and $H \geq 4.0$ V.

7/ AC limits at $V_{CC} = 5.5$ V are equal to the limits at $V_{CC} = 4.5$ V. For propagation delay tests, all paths must be tested.

8/ This parameter is guaranteed but not tested. This parameter is characterized upon initial design or process changes which affect this characteristic.

TABLE IB. SEP test limits. 1/ 2/

Device Types	T_A = Temperature ±10°C	V_{CC} = 4.5 V	Bias for latch-up test V_{CC} = 5.5 V no latch-up LET = 3/ 4/
		Effective LET no upsets [MeV/(mg/cm^2)]	
01, 02	+25°C	LET ≥ 100	≥ 100

1/ For SEP test conditions, see 4.4.4.4 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Worst case temperature is $T_A \geq +125$°C.
4/ Tested to an LET of ≥ 100 MeV/(mg/cm^2), with no latch-up (SEL).

Device type	All		
Case outlines	C and X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	$\overline{1R}$	8	$\overline{2Q}$
2	1D	9	2Q
3	1CP	10	$\overline{2S}$
4	$\overline{1S}$	11	2CP
5	1Q	12	$\overline{2D}$
6	$\overline{1Q}$	13	$\overline{2R}$
7	GND	14	V_{CC}

FIGURE 1. Terminal connections.

Inputs				Outputs	
$\overline{nS}$	$\overline{nR}$	nCP	nD	nQ	$\overline{nQ}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H 1/	H 1/
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q0}$

1/ This configuration is non-stable, that is, it will not persist when set and reset inputs return to their inactive (high) level.

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-high clock transition

Q0, $\overline{Q0}$ = The level of Q, $\overline{Q}$ before the indicated input conditions were established

FIGURE 2. Truth table.

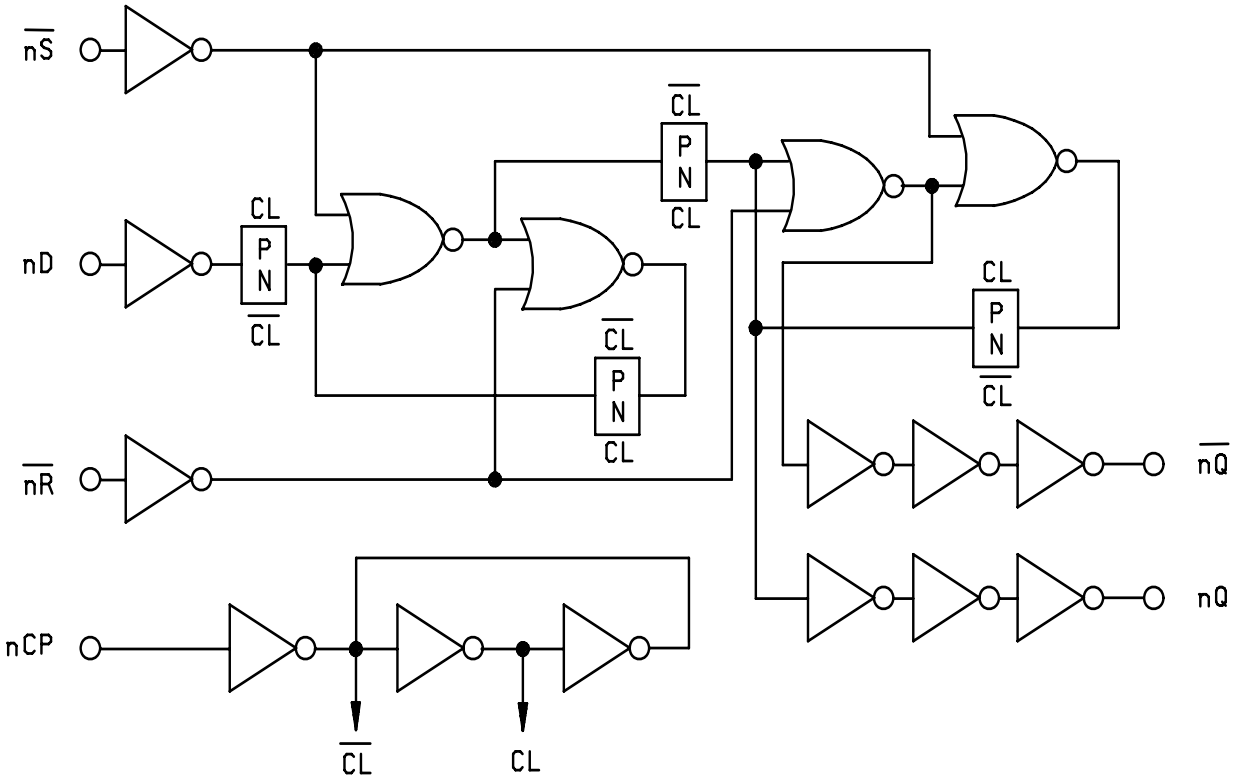


FIGURE 3. Logic diagram.

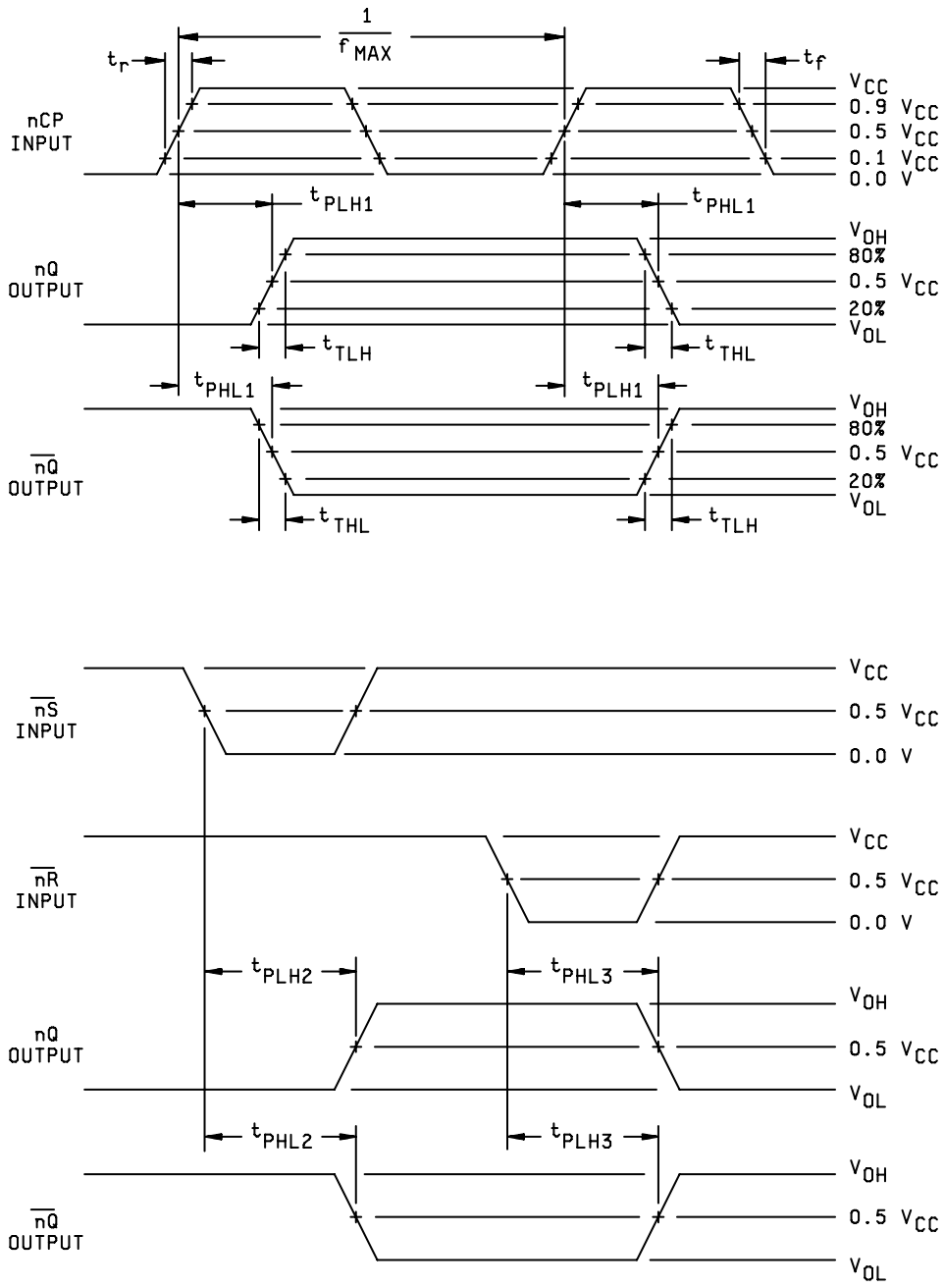
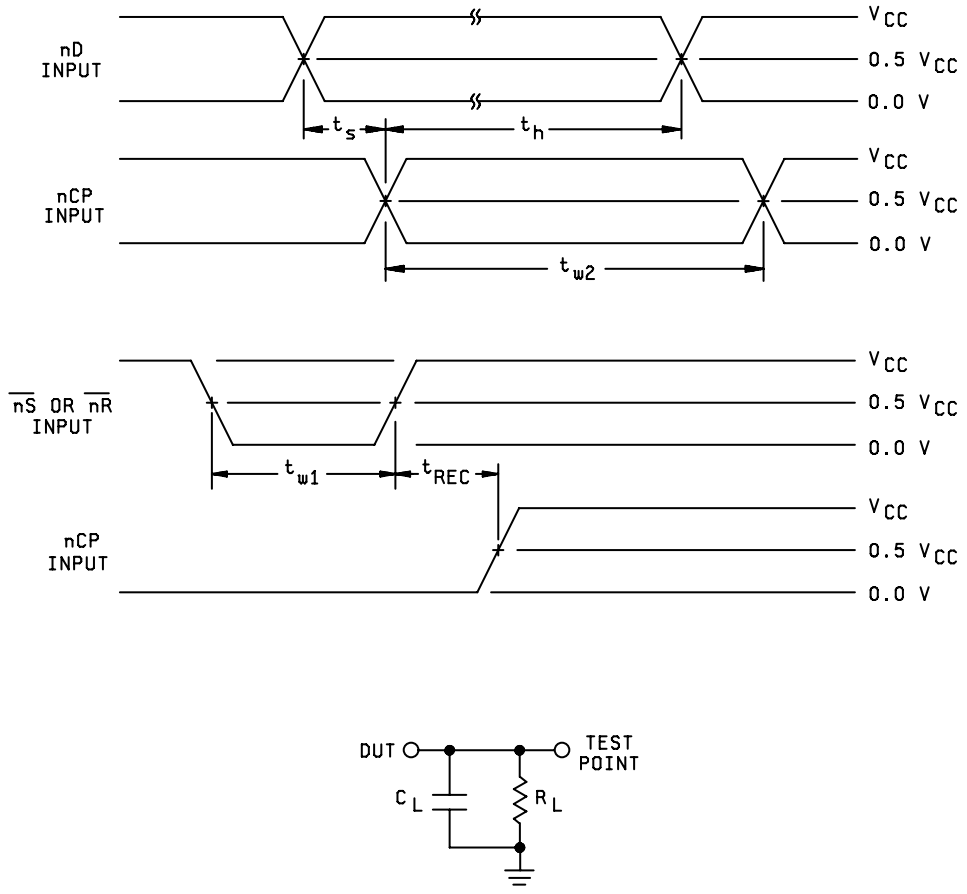


FIGURE 4. Switching waveforms and test circuit.



NOTES:
1. C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance).
2. R_L = 500Ω or equivalent.
3. Input signal from pulse generator: V_{IN} = 0.0 V to V_{CC}; PRR ≤ 10 MHz; t_r ≤ 3.0 ns; t_f ≤ 3.0 ns; t_r and t_f shall be measured from 10% V_{CC} to 90% V_{CC} and from 90% V_{CC} to 10% V_{CC}, respectively.

FIGURE 4. Switching waveforms and test circuit - Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table on figure 2 herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. Subgroups 4, 5 and 6 (C_{IN} and C_{PD} measurements) shall be measured only for the initial qualification and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and GND at a frequency of 1 MHz. For C_{IN} and C_{PD} the tests shall be sufficient to validate the limits defined in table IA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9	1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/ 3/
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11 3/
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1 and 7.
2/ PDA applies to subgroups 1, 7, 9 and deltas.
3/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be completed with reference to the zero hour electrical parameters (see table IA).

TABLE IIB. Burn-in and operating life test, delta parameters (+25°C).

Parameters 1/	Delta limits
I_{CC}	±2 μA
I_{OL}/I_{OH}	±15%

1/ These parameters shall be recorded before and after the required burn-in and life test to determine delta limits.

TABLE III. Irradiation test connections. 1/

Open	Ground	V_{CC} = 5 V ±0.5 V
5, 6, 8, 9	7	1, 2, 3, 4, 10, 11, 12, 13, 14

1/ Each pin except V_{CC} and GND will have a series resistor of 47KΩ ±5%, for irradiation testing.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and as specified herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5k rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latchup testing. When required by the customer, dose rate induced latchup testing shall be performed in accordance with method 1020 of MIL-STD-883 and as specified herein. Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. When required by the customer, dose rate upset testing shall be performed in accordance with method 1021 of MIL-STD-883 and herein.

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may effect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535. Device parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test 4 devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or $\geq 10^7$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The upset test temperature shall be +25°C. The latchup test temperature shall be at the maximum rated operating temperature ±10°C.

f. Bias conditions shall be V_{CC} = 4.5 V dc for the upset measurements and V_{CC} = 5.5 V dc for the latchup measurements.

g. For SEP test limits, see table IB herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

GND ..... Ground zero voltage potential.
I_{CC} ..... Quiescent supply current.
I_{IL} ..... Input current low.
I_{IH} ..... Input current high.
T_C ..... Case temperature.
T_A ..... Ambient temperature.
V_{CC} ..... Positive supply voltage.
C_{IN} ..... Input terminal-to-GND capacitance.
C_{OUT} ..... Output terminal-to-GND capacitance.
C_{PD} ..... Power dissipation capacitance.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

6.7 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied.

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

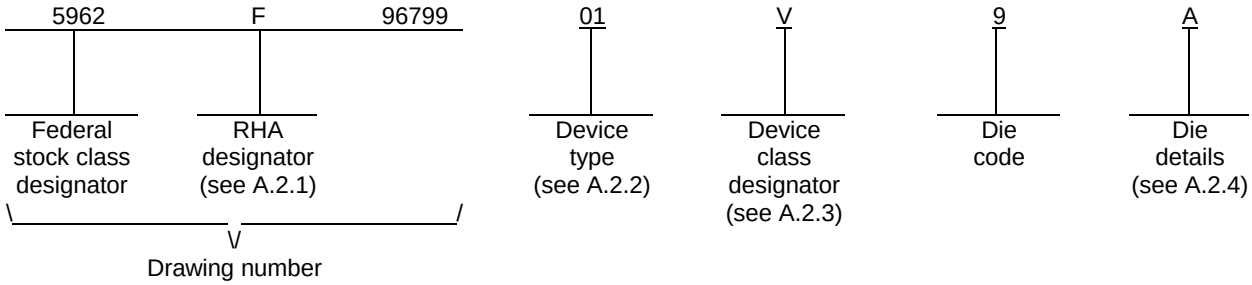
d. Number of transients (SEP).

e. Occurrence of latchup (SEP).

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device Class V) are reflected in the Part or Identification Number (PIN). When available a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die shall meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ACS74	Radiation Hardened, SOS, advanced CMOS, dual D flip-flop with set and reset.
02	ACS74-02	Radiation Hardened, SOS, advanced CMOS, dual D flip-flop with set and reset.

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535.

A.1.2.4 Die Details. The die details designation shall be a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die types	Figure number
01, 02	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die types	Figure number
01, 02	A-1

A.1.2.4.3 Interface materials.

Die types	Figure number
01, 02	A-1

A.1.2.4.4 Assembly related information.

Die types	Figure number
01, 02	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2. APPLICABLE DOCUMENTS

A.2.1 Government specification, standard, and handbooks. The following specification, standard, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan, for device classes Q and V and herein.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and figure A-1.

A.3.2.5 Truth table. The truth table shall be as defined in paragraph 3.2.3 herein.

A.3.2.6 Irradiation test connections. The irradiation test connections shall be as defined within paragraph 3.2.6 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4. VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer Lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4 herein.

A.5. DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be in accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6. NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DSCC-VA, P.O. Box 3990, Columbus, Ohio 43218-3990 or telephone (614) 692-0547.

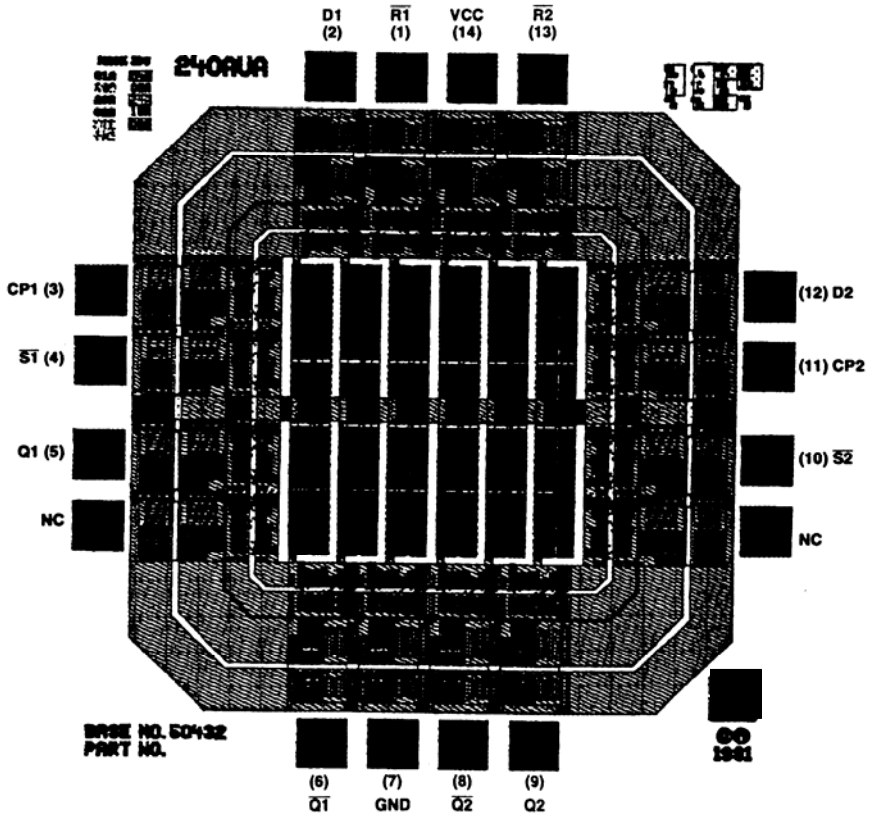
A.6.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DSCC-VA and have agreed to this drawing.

Die bonding pad locations and electrical functions.

Die physical dimensions.

Die size:	2240 x 2240 microns
Die thickness:	21 ±2 mils



Note: Pad numbers reflect terminal numbers when placed in case outlines C and X (see figure 1).

FIGURE A-1. Die bonding pad locations and electrical functions.

Interface materials.

Device type 01		
Metal 1:	AlSiCu	7.5kA ±0.75kA
Metal 2 (Top):	AlSiCu	10.0kA ±1.0kA
Device type 02		
Metal 1:	AlSi	7.0kA ±1.0kA
Metal 2 (Top):	AlSi	10.0kA ±1.0kA
Backside metallization:	None	

Glassivation.

Device type 01	
Type:	PSG
Thickness:	8.0kA ±1.0kA
Device type 02	
Type:	PSG
Thickness:	13.0kA ±1.5kA
Substrate:	Silicon on Sapphire (SOS)

Assembly related information.

Substrate potential:	Insulator
Special assembly instructions:	Bond pad #14 (V_{CC}) first

FIGURE A-1. Die bonding pad locations and electrical functions – Continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 08-01-23

Approved sources of supply for SMD 5962-96799 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962F9679901VCC	34371	ACS74DMSR
5962F9679901VXC	34371	ACS74KMSR
5962F9679901V9A	34371	ACS74HMSR
5962F9679902VCC	3/	ACS74DMSR-02
5962F9679902VXC	3/	ACS74KMSR-02
5962F9679902V9A	3/	ACS74HMSR-02

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
34371	Intersil Corporation 1650 Robert J. Conlan Blvd Palm Bay, FL 32905