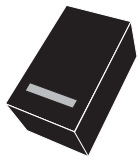
ESDAXLC6-1MY2

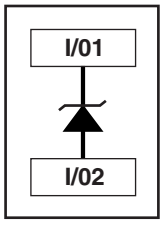
Extra low capacitance single line transient voltage surge suppressor (TVS)

Datasheet - production data



µQFN-2L

Figure 1. Functional diagram



Features

- Extra low capacitance 0.6 pF max on a wide frequency spectrum (200 MHz - 3000 MHz)
- Unidirectional device
- Low clamping factor V_{CL}/V_{BR}
- Fast response time
- Very thin package: 0.50 mm max
- Low leakage current
- High ESD protection level
- High integration
- Suitable for high density boards

Complies with the following standards

- IEC 61000-4-2 level 4
- MIL STD 883G-Method 3015-7: class 3B

Applications

Where transient over voltage protection and electrical overstress protection in sensitive equipment is required, such as:

- Computers
- Printers
- Communication systems
- Cellular phone handsets and accessories
- Video equipment Portable equipment

Description

The ESDAXLC6-1MY2 is a single line Transil™ diode designed specifically for the protection of integrated circuits in portable equipment and miniaturized electronics devices subject to ESD transient over voltages. Packaged in µQFN-2L, it minimizes PCB consumption.

TM: Transil is a trademark of STMicroelectronics

1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
V_{PP}	Peak pulse voltage: IEC 61000-4-2, level 4: contact discharge		8	kV
P_{PP}	Peak pulse power dissipation (8/20 µs) (1)	$T_{j\ initial} = T_{amb}$	12	W
I_{PP}	Peak pulse current typical value (8/20 µs)		2.8	A
T_{op}	Operating junction temperature range		- 40 to + 125	°C
T_{stg}	Storage temperature range		- 55 to +150	°C

1. For a surge greater than the maximum values, the diode will fail in short-circuit

Figure 2. Electrical characteristics (definitions)

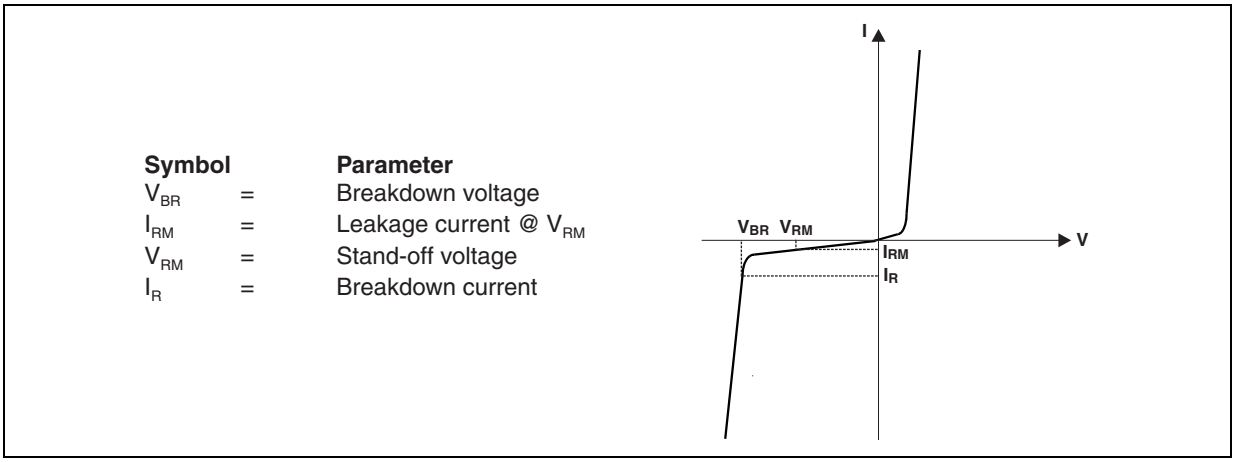


Table 2. Electrical characteristics (values, T_{amb} = 25 °C)

Symbol	Test condition	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	6	-	-	V
I_{RM}	V_{RM} = 3 V	-	-	100	nA
C_{line}	V_R = 0 V, F = (200 MHz - 3000 MHz), V_{osc} = 30 mV	-	-	0.6	pF

Figure 3. Junction capacitance versus reverse voltage applied (typical values)

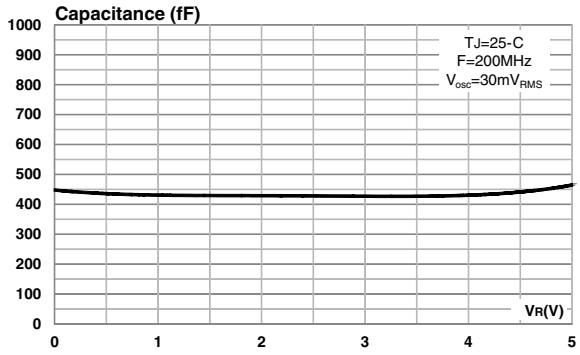


Figure 4. Junction capacitance versus frequency (typical values)

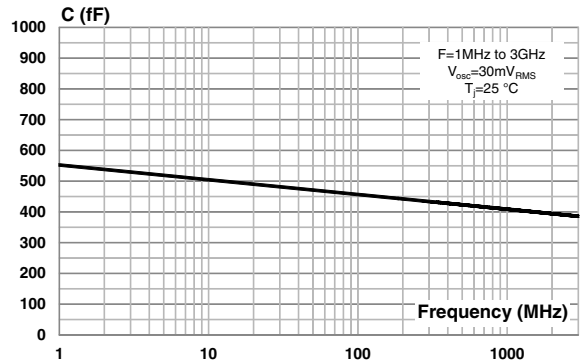


Figure 5. S21 (dB) attenuation

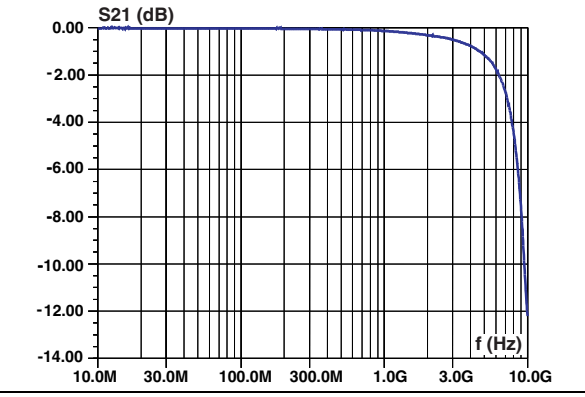


Figure 6. Leakage current versus junction temperature (typical values)

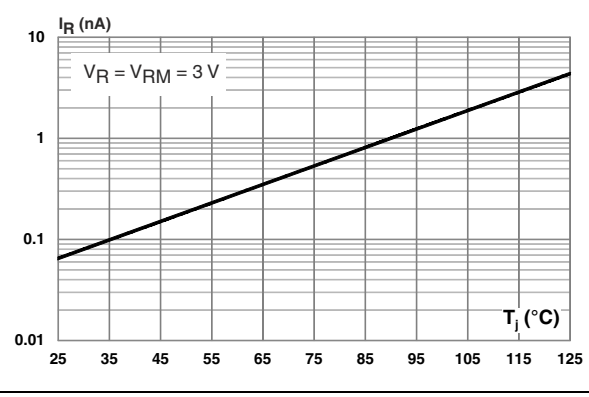


Figure 7. ESD response to IEC 61000-4-2 (+ 8 kV contact discharge)

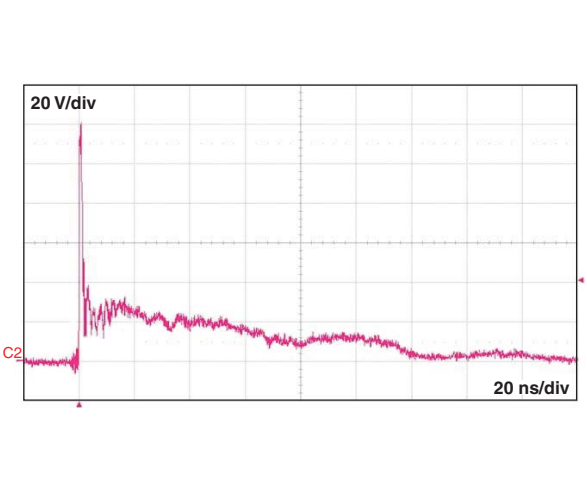
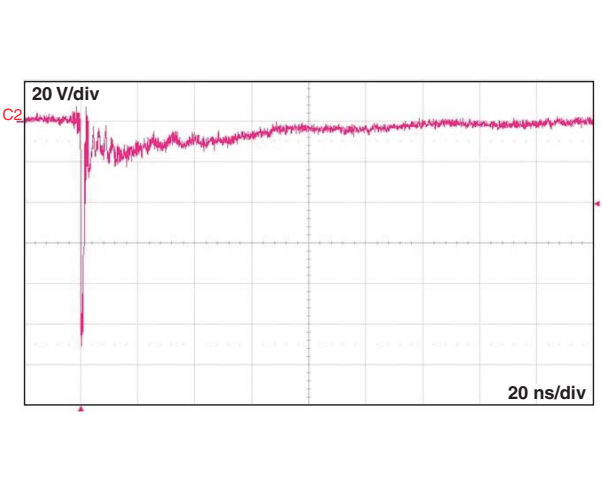
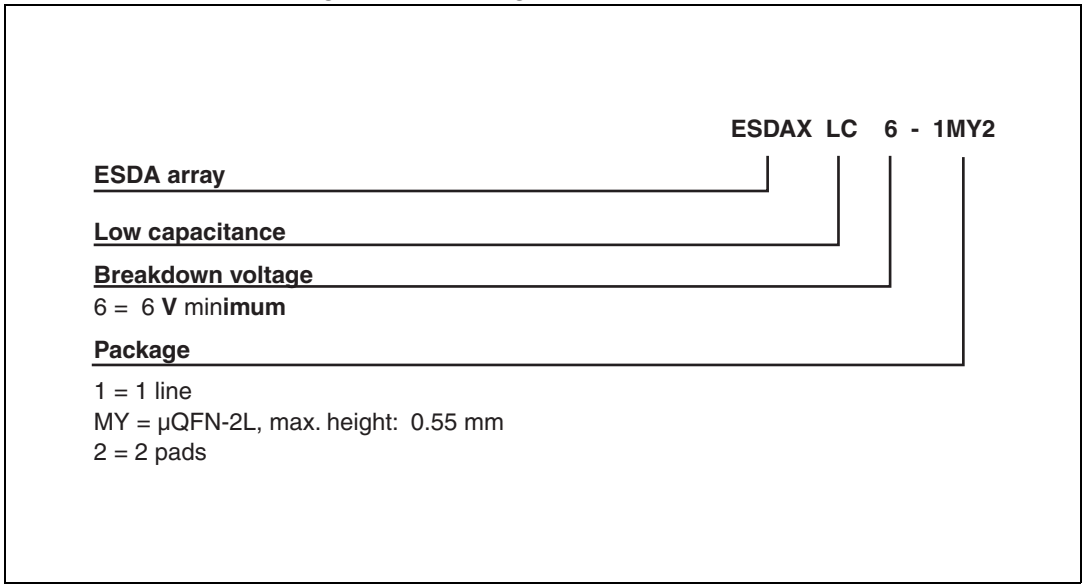


Figure 8. ESD response to IEC 61000-4-2 (-8 kV contact discharge)



2 Ordering information scheme

Figure 9. Ordering information scheme

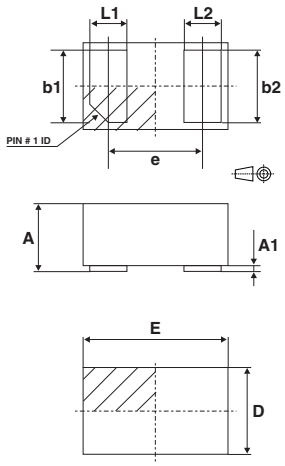


3 Package information

- Epoxy meets UL 94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 3. µQFN-2L dimensions



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.40	0.47	0.50	0.016	0.019	0.020
A1	0.00		0.05	0.000		0.002
b1	0.45	0.50	0.55	0.018	0.020	0.022
b2	0.45	0.50	0.55	0.018	0.020	0.022
D	0.55	0.60	0.65	0.022	0.024	0.026
E	0.95	1.00	1.05	0.037	0.039	0.041
e	0.60	0.65	0.70	0.024	0.026	0.028
L1	0.20	0.25	0.30	0.008	0.010	0.012
L2	0.20	0.25	0.30	0.008	0.010	0.012

Figure 10. Footprint (dimensions in mm)

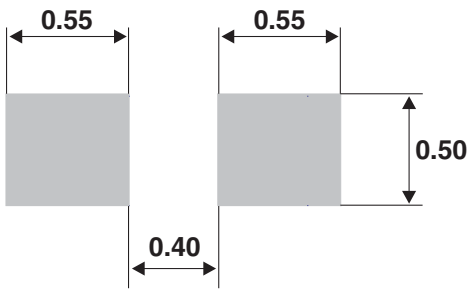
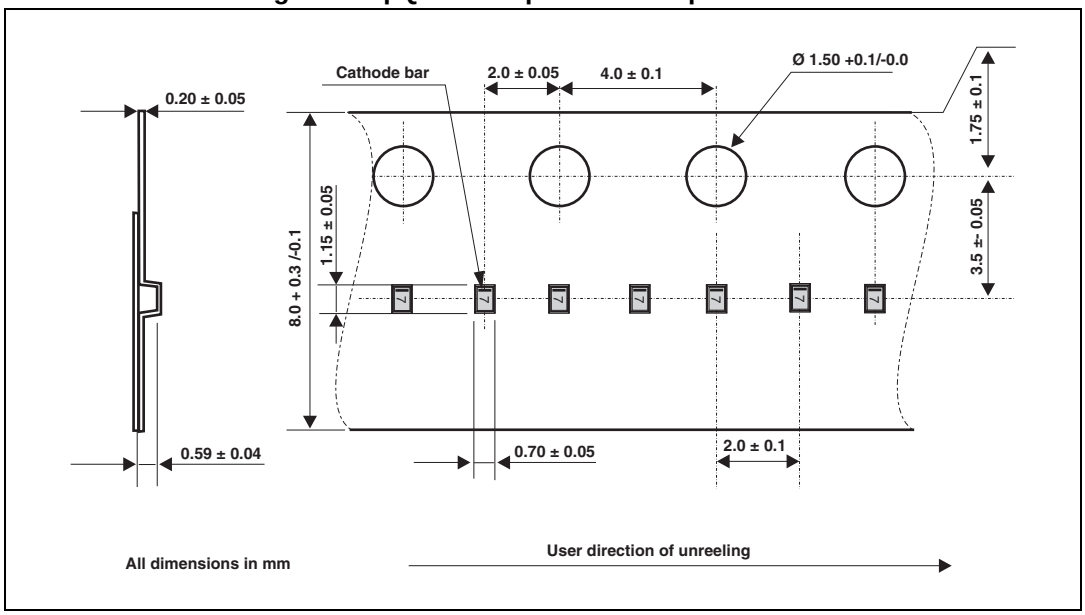


Figure 11. Marking

Note: Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

Figure 12. µQFN-2L tape and reel specification

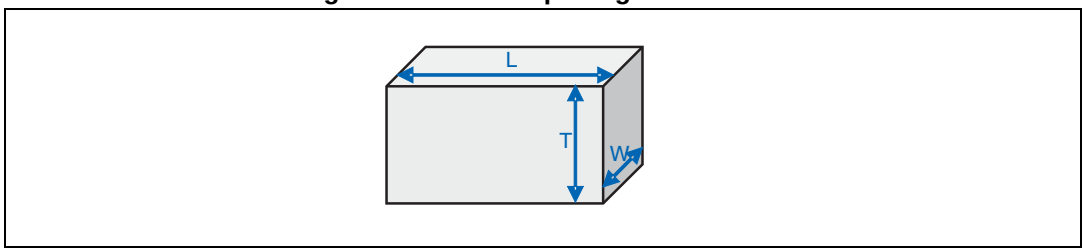


4 Recommendation on PCB assembly

4.1 Stencil opening design

1. General recommendation on stencil opening design
   a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

Figure 13. Stencil opening dimensions



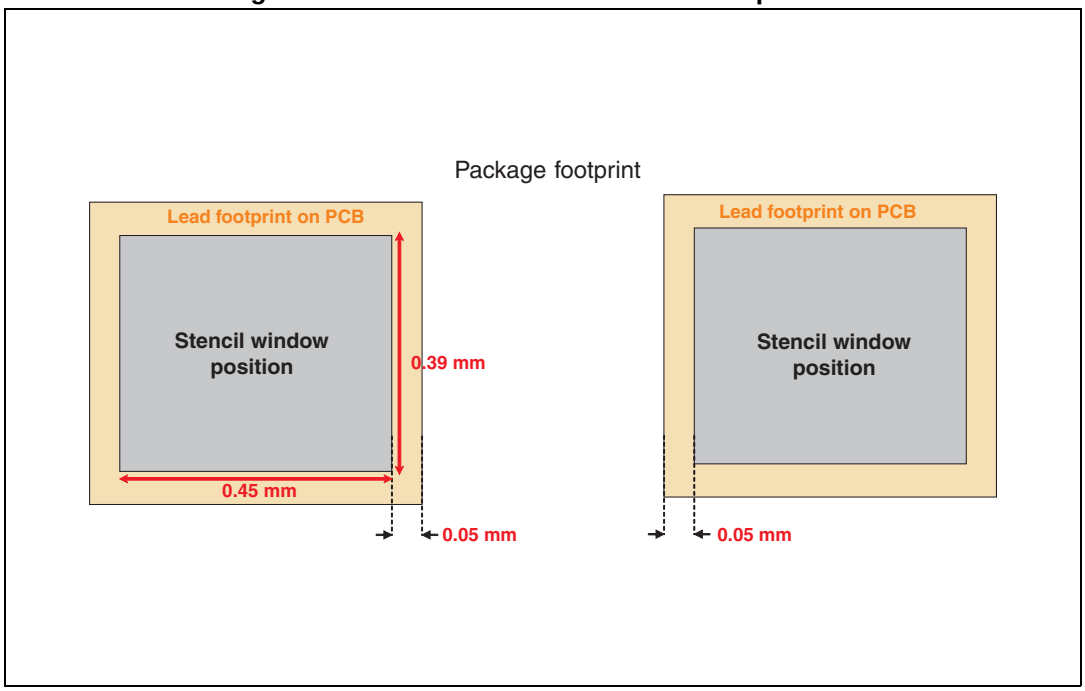
   b) General design rule
   Stencil thickness (T) = 75 ~ 125 µm

$$\text{Aspect Ratio} = \frac{W}{T} \geq 1.5$$

$$\text{Aspect Area} = \frac{L \times W}{2T(L + W)} \geq 0.66$$

2. Reference design
   a) Stencil opening thickness: 100 µm
   b) Stencil opening for central exposed pad: Opening to footprint ratio is 50%.
   c) Stencil opening for leads: Opening to footprint ratio is 90%.

Figure 14. Recommended stencil window position



4.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Solder paste with fine particles: powder particle size is 20-45 µm.

4.3 Placement

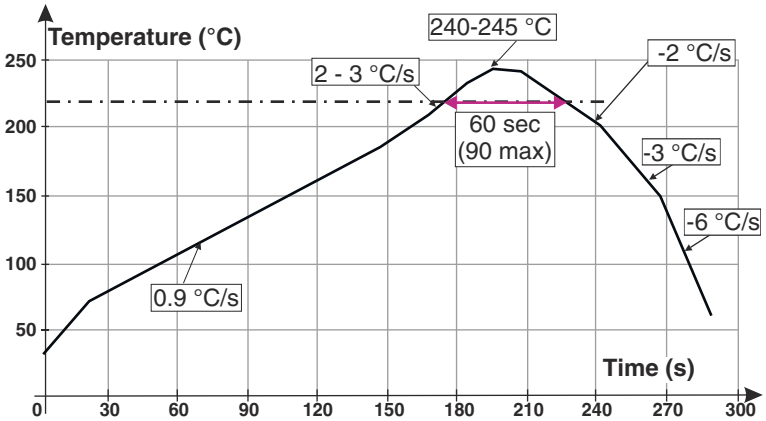
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

4.5 Reflow profile

Figure 15. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.
Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020

5 Ordering information

Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
ESDAXLC6-1MY2	7	µQFN-2L	0.942 mg	12000	Tape and reel

6 Revision history

Table 5. Document revision history

Date	Revision	Changes
18-Jan-2010	1	Initial release.
23-Sep-2011	2	Updated package name.
31-Mar-2014	3	Updated operating junction temperature range in *Table 2*. Updated *Figure 3*, *Figure 4*, and *Figure 6*. Updated graphic and dimension names in *Table 3*, Updated *Figure 15*.

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