



Product Specification

B121EW08 V0

Preliminary Specifications

Final Specifications

Module	12.1" WXGA Color TFT-LCD
Model Name	B121EW08 V0

Customer	Date
_____	_____
Checked & Approved by	
_____	_____
Note: This Specification is subject to change without notice.	

Approved by	Date
_____	_____
Prepared by	
_____	_____
NBBU Marketing Division / AU Optronics corporation	



Contents

1. Handling Precautions	4
2. General Description	5
2.1 General Specification	5
2.2 Optical Characteristics	6
3. Functional Block Diagram	11
4. Absolute Maximum Ratings	12
4.1 Absolute Ratings of TFT LCD Module	12
4.2 Absolute Ratings of Backlight Unit	12
4.3 Absolute Ratings of Environment	12
5. Electrical characteristics	13
5.1 TFT LCD Module	13
5.2 Backlight Unit	15
6. Signal Characteristic	17
6.1 Pixel Format Image	17
6.2 The input data format	18
6.3 Signal Description/Pin Assignment	19
6.4 Interface Timing	21
6.5 Power ON/OFF Sequence	22
7. Connector Description	23
7.1 TFT LCD Module	23
7.2 Backlight Unit	23
8. Vibration and Shock Test	24
8.1 Vibration Test	24
8.2 Shock Test Spec:	24
9. Reliability	25
10. Mechanical Characteristics	26
11. Shipping and Package	28
11.1 Shipping Label Format	28
11.2. Carton package	28
11.3 Shipping package of palletizing	28
12. Appendix: EDID description	30



Product Specification

B121EW08 V0

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2007/08/13	All	First Edition for Customer		



1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CCFL Reflector edge. Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be damaged.
- 10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Cold cathode fluorescent lamp in LCD contains a small amount of mercury. Please follow local ordinances or regulations for disposal.
- 13) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source(, IEC60950 or UL1950), or be applied exemption.
- 14) The LCD module is designed so that the CCFL in it is supplied by Limited Current Circuit(IEC60950 or UL1950). Do not connect the CCFL in Hazardous Voltage Circuit.



Product Specification

B121EW08 V0

2. General Description

B121EW08 V0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and 2-CCFL backlight system. The screen format is intended to support the WXGA (1280(H) x 800(V)) screen and 262k colors (RGB 6-bits data driver). All input signals are LVDS interface compatible.

2.1 General Specification

The following items are characteristics summary on the table at 25 °C condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	307.9 (12.1 W")			
Active Area	[mm]	261.12 (H) x 163.2 (V)			
Pixels H x V		1280x3(RGB) x 800			
Pixel Pitch	[mm]	0.204			
Pixel Arrangement		R.G.B. Vertical Stripe			
Display Mode		Normally White			
White Luminance (ICCFL=6.0mA) Note: ICCFL is lamp current	[cd/m ²]	500 Typ. (5 points average) 425 Min. (5 points average) (Note1)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		600:1 Typ., 500:1 Min.			
Optical Rise Time/Fall Time	[msec]	25 Typ., 35 Max.			
Nominal Input Voltage VDD	[Volt]	+3.3 Typ.			
Power Consumption	[Watt]	10.0 Typ. (Without inverter loss)			
Weight	[Grams]	430g Max.			
Physical Size (w/o Inverter)	[mm]		L	W	T
		Max	276.3	180.9	7.0
		Typ	275.8	180.4	-
		min	275.3	179.9	-
Electrical Interface		1 Channel LVDS			
Surface Treatment		Anti-glare, 3H Max.			
Support Color		262K colors (RGB 6-bit)			
Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	0 to +50 -20 to +60			
RoHS Compliance		RoHS Compliance			



Product Specification

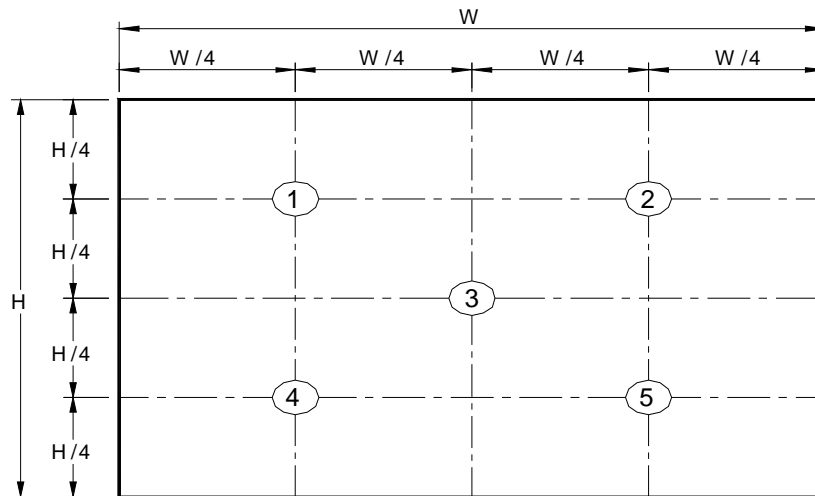
B121EW08 V0

2.2 Optical Characteristics

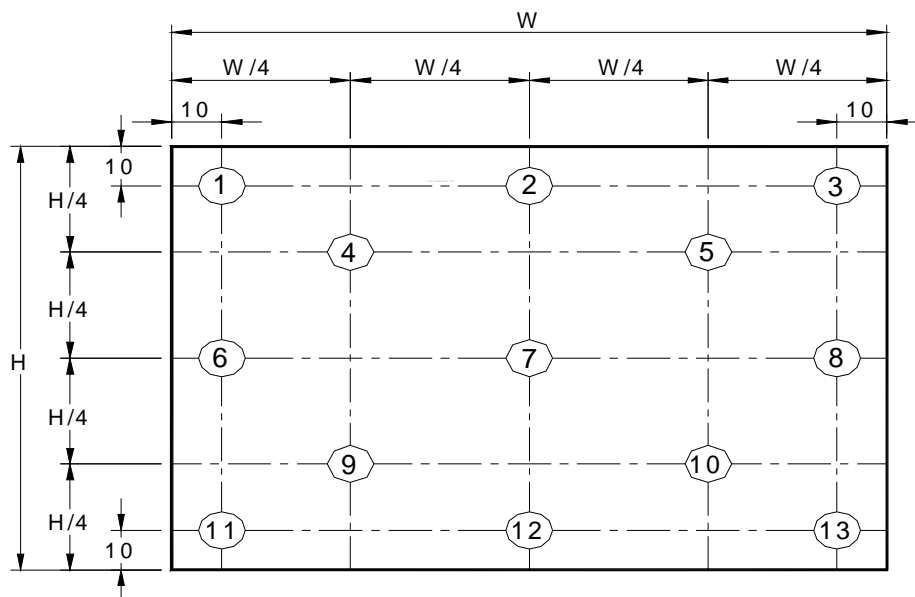
The optical characteristics are measured under stable conditions at 25°C (Room Temperature):

Item	Unit	Conditions	Min.	Typ.	Max.	Note
White Luminance	[cd/m ²]	5 points average	425	500	-	1, 4, 5.
Viewing Angle	[degree]	Horizontal (Right) CR = 10 (Left)	70	80	-	8
	[degree]		70	80	-	
	[degree]	Vertical (Upper) CR = 10 (Lower)	70	80	-	
	[degree]		70	80	-	
Luminance Uniformity		5 Points			1.25	1
Luminance Uniformity		13 Points			2.00	2
CR: Contrast Ratio			500	600	-	6
Cross talk	%				1.4	7
Response Time	[msec]	Rising	-	15	20	8
	[msec]	Falling	-	10	15	
	[msec]	Rising + Falling		25	35	
Color / Chromaticity Coordinates (CIE 1931)		Red x	0.550	0.580	0.610	2,8
		Red y	0.310	0.340	0.370	
		Green x	0.300	0.330	0.360	
		Green y	0.545	0.575	0.605	
		Blue x	0.125	0.155	0.185	
		Blue y	0.125	0.155	0.185	
		White x	0.283	0.313	0.343	
		White y	0.299	0.329	0.359	
NTSC	%	CIE 1931	-	45	-	

Note 1: 5 points position (Display area: 261.12 (H) x 163.2 (V) mm)



Note 2: 13 points position



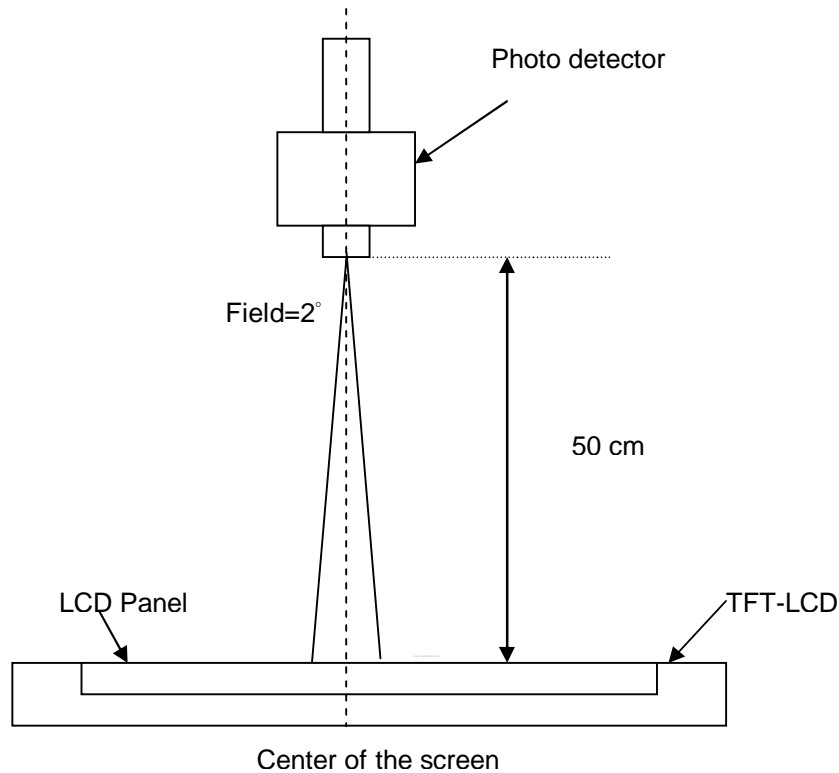
Note 3: The luminance uniformity of 5 and 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room.



Note 5 : Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points , $Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5$

$L (x)$ is corresponding to the luminance of the point X at Figure in Note (1).

Note 6 : Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

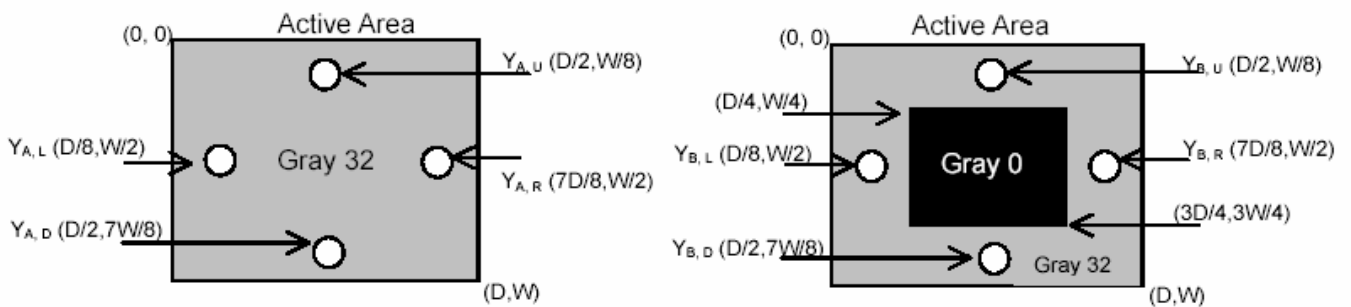
Note 7 : Definition of Cross Talk (CT)

$$CT = | Y_B - Y_A | / Y_A \times 100 (\%)$$

Where

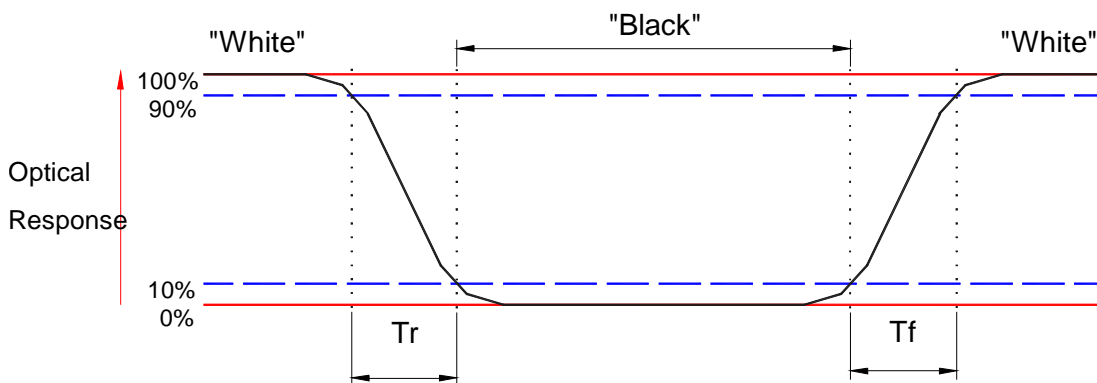
Y_A = Luminance of measured location without gray level 0 pattern (cd/m²)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m²)



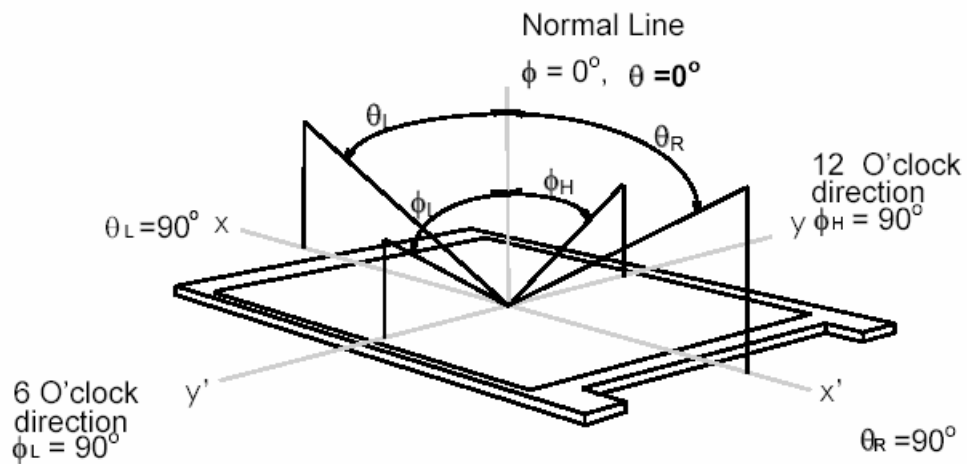
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



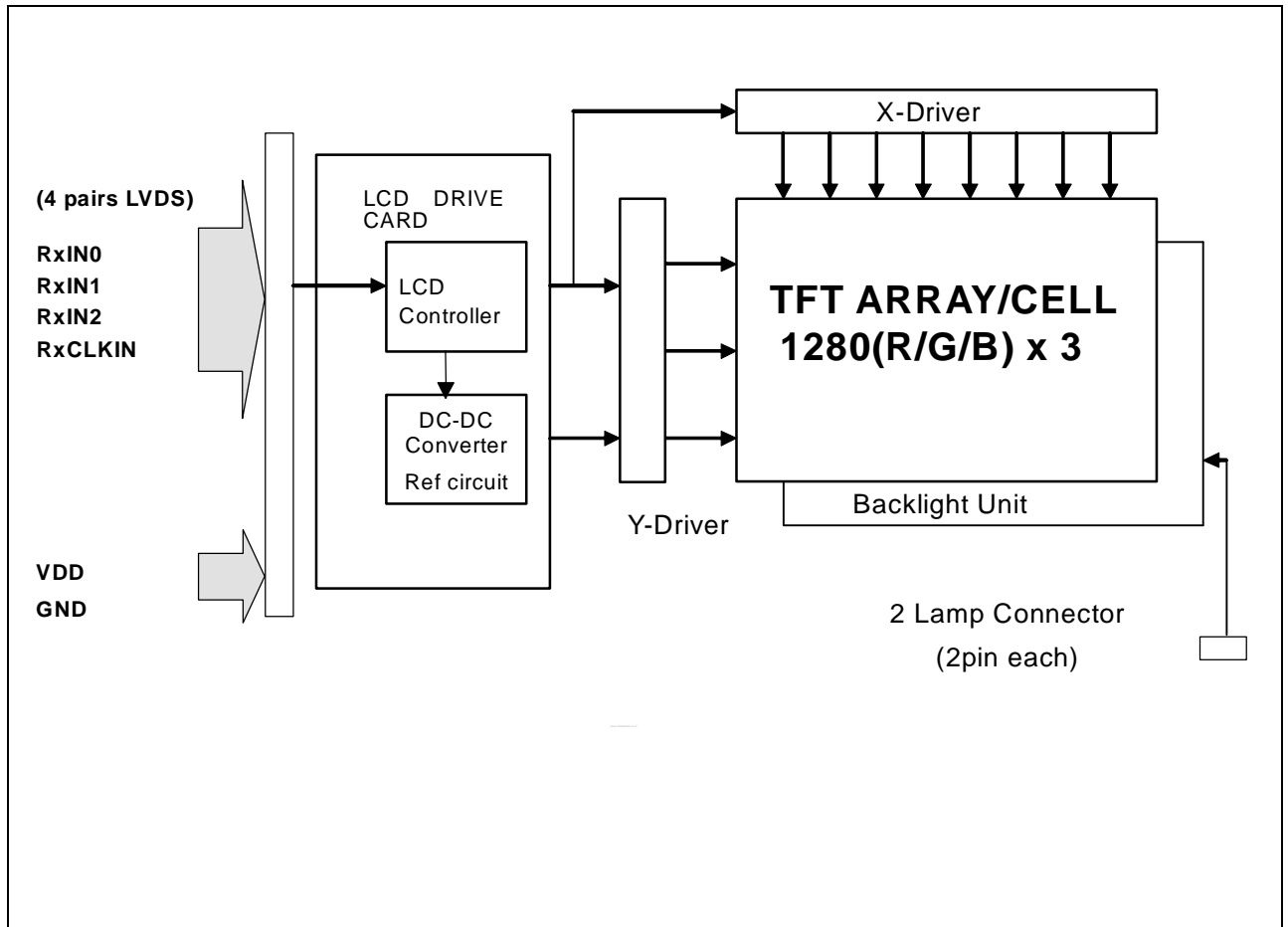
Note 9: Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≥ 10 , at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 12.1 inches wide Color TFT/LCD Module.



4. Absolute Maximum Ratings

Absolute maximum ratings of the module are as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/ LCD Drive	VDD	2.8	3.8	[Volt]	Note 1,2

4.2 Absolute Ratings of Backlight Unit

Item	Symbol	Min	Max	Unit	Conditions
CCFL Current	ICCFL	5.0	6.0	[mA] rms	Note 1,2

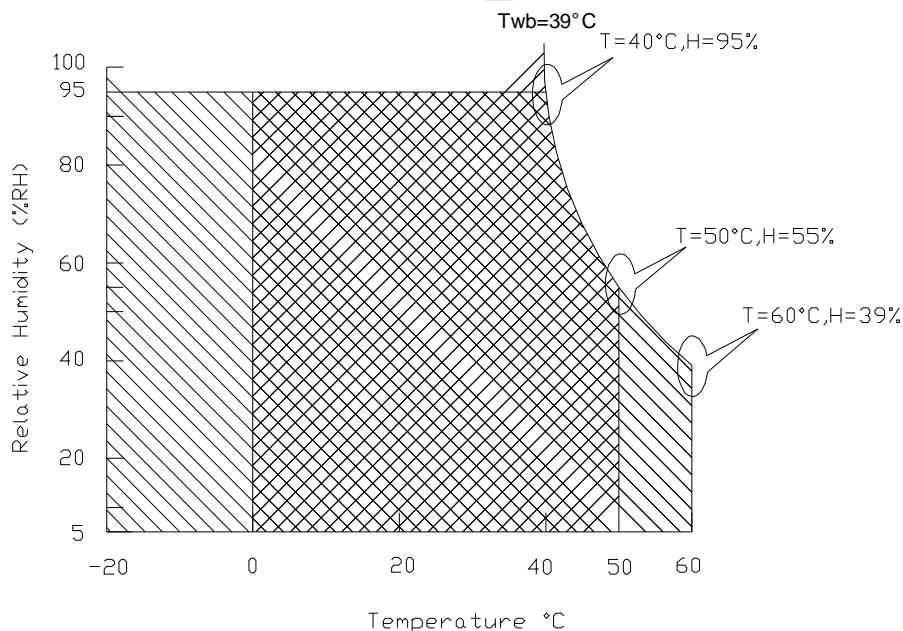
4.3 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 3
Operation Humidity	HOP	5	95	[%RH]	Note 3
Storage Temperature	TST	-20	+60	[°C]	Note 3
Storage Humidity	HST	5	95	[%RH]	Note 3

Note 1: At Ta (25°C)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality performance, please refer to AUO IIS(Incoming Inspection Standard).



Operating Range  Storage Range  + 

5. Electrical characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

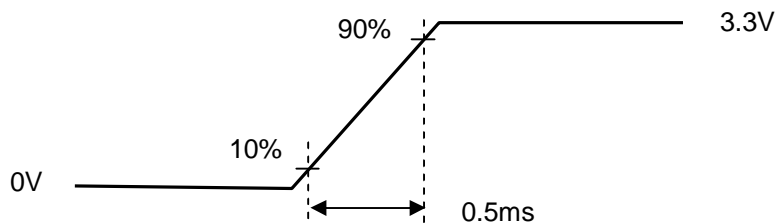
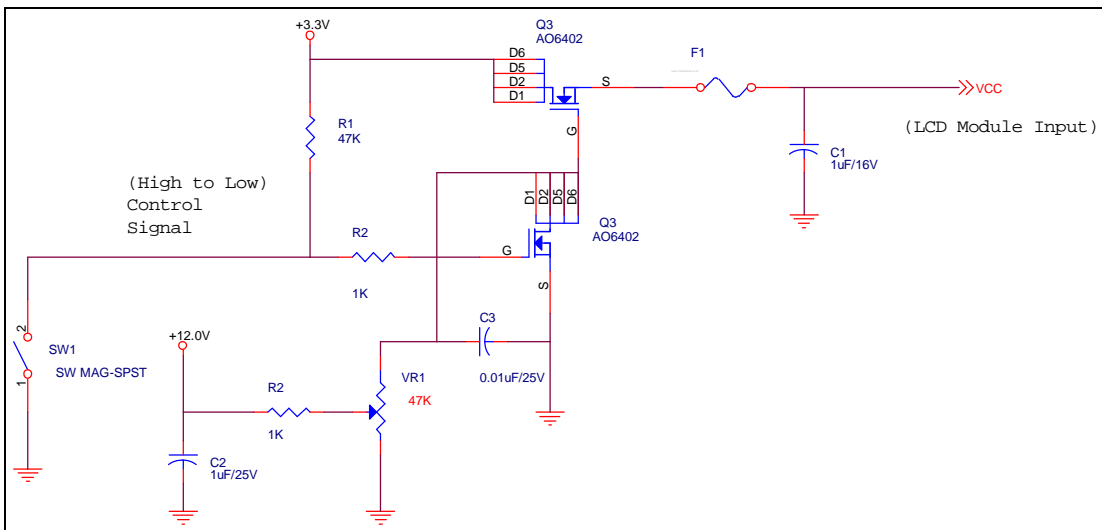
Input power specifications are as follows;

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power		0.9	1.1	[Watt]	Note 1, 2
IDD	IDD Current		270	370	[mA]	Note 1, 2
IRush	Inrush Current			1000	[mA]	Note 3
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	[mV] p-p	

Note 1 : Maximum Measurement Condition : Black Pattern

Note 2 : Typical Measurement Condition: Mosaic Pattern

Note 3 : Measure Condition



Vin rising time

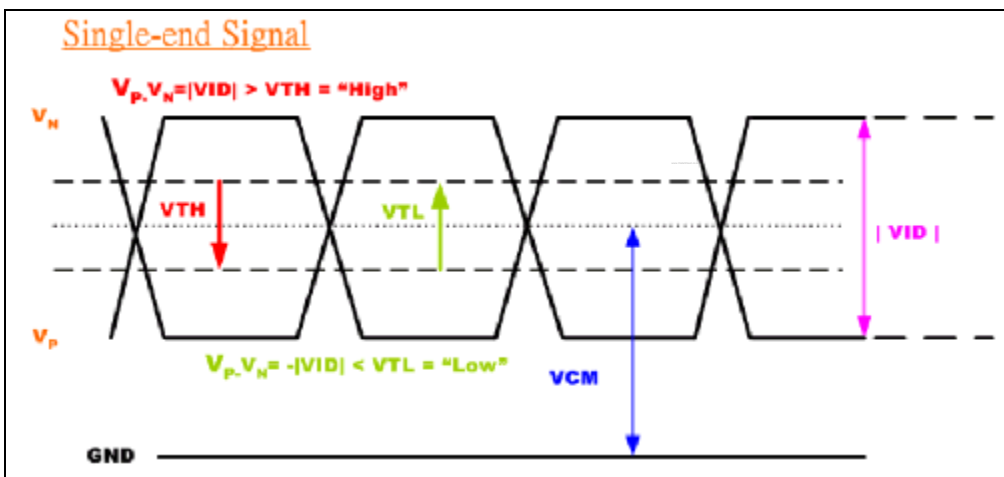
5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
Vth	Differential Input High Threshold (Vcm=+1.2V)		100	[mV]
Vtl	Differential Input Low Threshold (Vcm=+1.2V)	-100		[mV]
Vcm	Differential Input Common Mode Voltage	1.125	1.375	[V]

Note: LVDS Differential Voltage



5.2 Backlight Unit

Parameter guideline for CCFL Inverter

Parameter	Min	Typ	Max	Units	Condition
CCFL current each Lamp (I_{CCFL})	5.0	5.5	6.0	[mA] rms	(Ta=25°C) Note 2
CCFL Frequency(F_{CCFL})	45	55	65	[KHz]	(Ta=25°C) Note 3,4
CCFL Startup Voltage(V_s)		1150	1400	[Volt] rms	(Ta= 0°C) Note 5
CCFL Startup Voltage(V_s)		920	1110	[Volt] rms	(Ta= 25°C) Note 5
CCFL Voltage (Reference) (V_{CCFL})		550		[Volt] rms	(Ta=25°C) Note 6
CCFL Power consumption for 2 Lamp (P_{CCFL})	-	-	7.8	[Watt]	(Ta=25°C) Note 6

Note 1: Typ are AUO recommended Design Points.

*1 All of characteristics listed are measured under the condition using the AUO Test inverter.

*2 In case of using an inverter other than listed, it is recommended to check the inverter carefully.

Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.

*3 In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CCFL, for instance, becomes more than 1 [M ohm] when CFL is damaged.

*4 Generally, CCFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.

*5 CCFL discharge frequency must be carefully chosen so as not to produce interfering noise stripes on the screen.

*6 Reducing CCFL current increases CCFL discharge voltage and generally increases CCFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

Note 2: It should be employed the inverter which has “Duty Dimming”, if ICCFL is less than 4mA.

Note 3: CCFL discharge frequency should be carefully determined to avoid interference between inverter and TFT LCD.

Note 4: The frequency range will not affect to lamp life and reliability characteristics.

Note 5: CCFL inverter voltage should be able to give out a power that has a generating capacity larger than the lamp startup voltage, otherwise backlight may has blinking for a moment after turns on or can not be turned on.

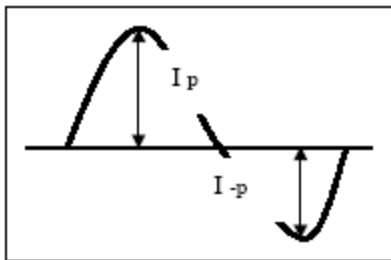
Note 6: Calculator value for reference ($ICCFL \times VCCFL = PCCFL$)

Note 7: Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp, are following.

It shall help increase the lamp lifetime and reduce leakage current.

- a. The asymmetry rate of the inverter waveform should be less than 10%.
- b. The distortion rate of the waveform should be within $\sqrt{2} \pm 10\%$.

* Inverter output waveform had better be more similar to ideal sine wave.



* Asymmetry rate:

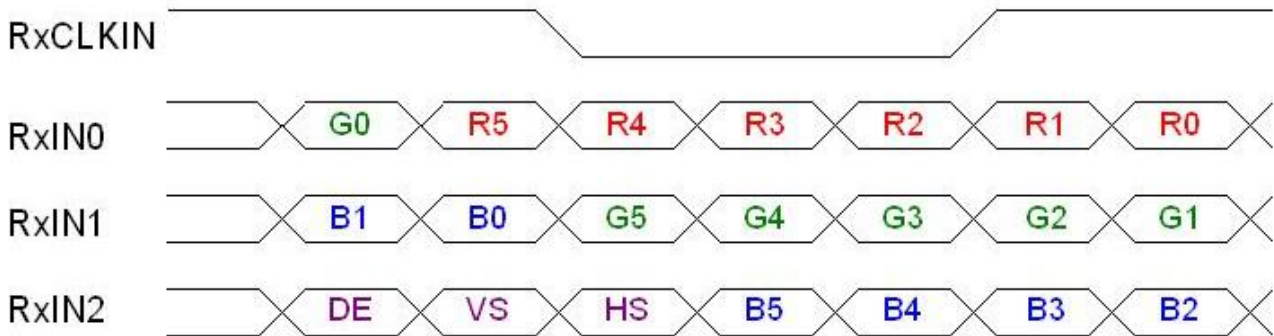
$$\frac{|I_p - I_{-p}|}{I_{rms}} * 100\%$$

* Distortion rate

$$I_p \text{ (or } I_{-p}) / I_{rms}$$

Note 8: It is an edge-type BLU with dual CCFL, the life-time define as the brightness decay to 50% of original value and under normal operation.

6.2 The input data format



Signal Name	Description	
+RED5 (R5) +RED4 (R4) +RED3 (R3) +RED2 (R2) +RED1 (R1) +RED0 (R0)	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) (Red-pixel Data)	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
+GREEN 5 (G5) +GREEN 4 (G4) +GREEN 3 (G3) +GREEN 2 (G2) +GREEN 1 (G1) +GREEN 0 (G0)	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) (Green-pixel Data)	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
+BLUE 5 (B5) +BLUE 4 (B4) +BLUE 3 (B3) +BLUE 2 (B2) +BLUE 1 (B1) +BLUE 0 (B0)	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) (Blue-pixel Data)	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
-DTCLK	Data Clock	The typical frequency is 71.1 MHz. The signal is used to strobe the pixel data and DSPTMG signals. All pixel data shall be valid at the falling edge when the DSPTMG signal is high.
DSPTMG (DE)	Display Timing	This signal is stored at the falling edge of -DTCLK. When the signal is high, the pixel data shall be valid to be displayed.
VSUNC (VS)	Vertical Sync	The signal is synchronized to -DTCLK .
HSUNC (HS)	Horizontal Sync	The signal is synchronized to -DTCLK .

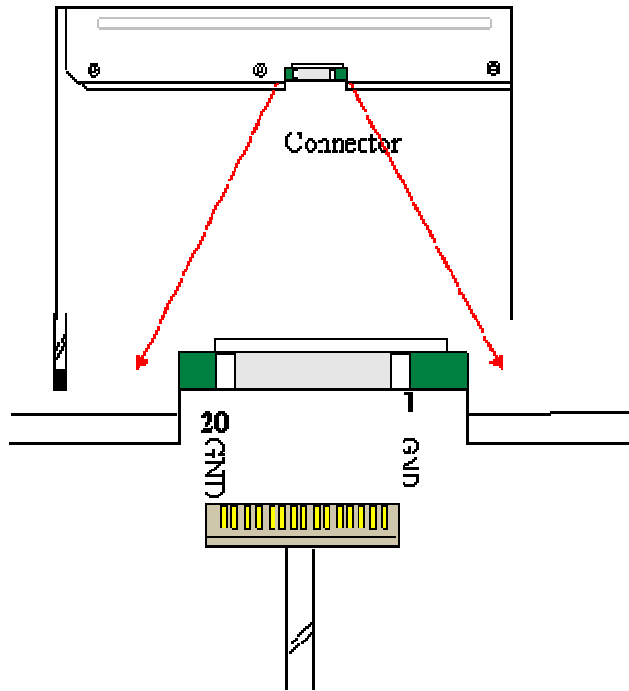
Note: Output signals from any system shall be low or High-impedance state when VDD is off.

6.3 Signal Description/Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

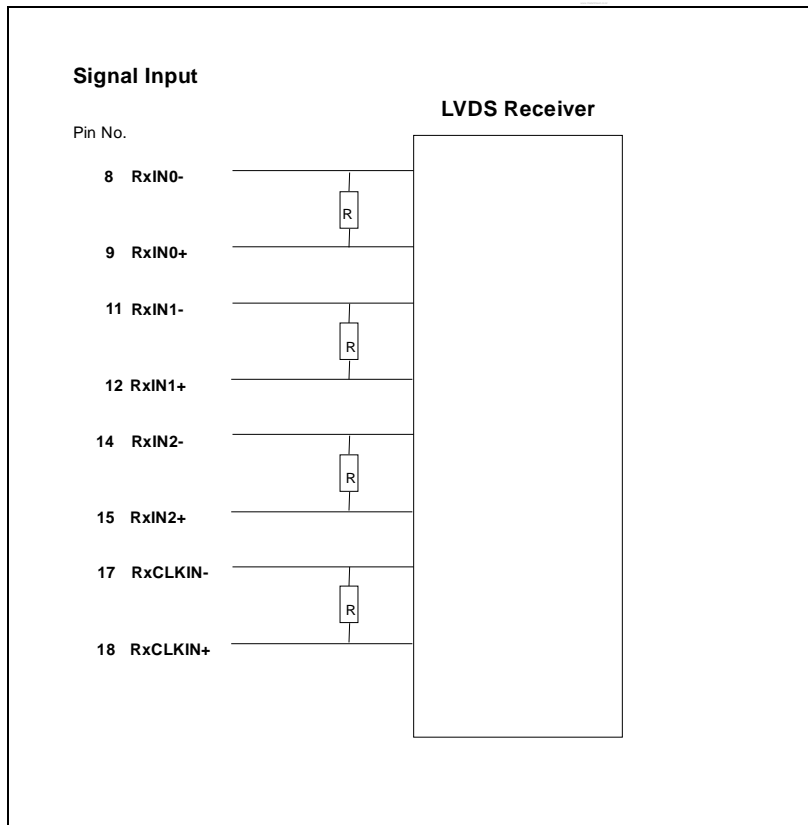
Pin	Signal Name	Description
1	GND	Ground
2	VDD	+3.3V Power Supply
3	VDD	+3.3V Power Supply
4	V _{EDID}	+3.3V EDID Power
5	NC	No Connection (Bist Enable)
6	CLK _{EDID}	EDID Clock Input
7	DATA _{EDID}	EDID Data Input
8	RxIN0-	LVDS differential data input(R0-R5, G0)
9	RxIN0+	LVDS differential data input(R0-R5, G0)
10	GND	Ground
11	RxIN1-	LVDS differential data input(G1-G5, B0-B1)
12	RxIN1+	LVDS differential data input(G1-G5, B0-B1)
13	GND	Ground
14	RxIN2-	LVDS differential data input(B2-B5, HS, VS, DE)
15	RxIN2+	LVDS differential data input(B2-B5, HS, VS, DE)
16	GND	Ground
17	RxCLKIN-	LVDS differential clock input
18	RxCLKIN+	LVDS differential clock input
19	GND	Ground
20	NC	No connection

Note1: Start from right side



Note2: Input signals shall be low or High-impedance state when VDD is off.
internal circuit of LVDS inputs are as following.

The module uses a 100ohm resistor between positive and negative data lines of each receiver input



6.4 Interface Timing

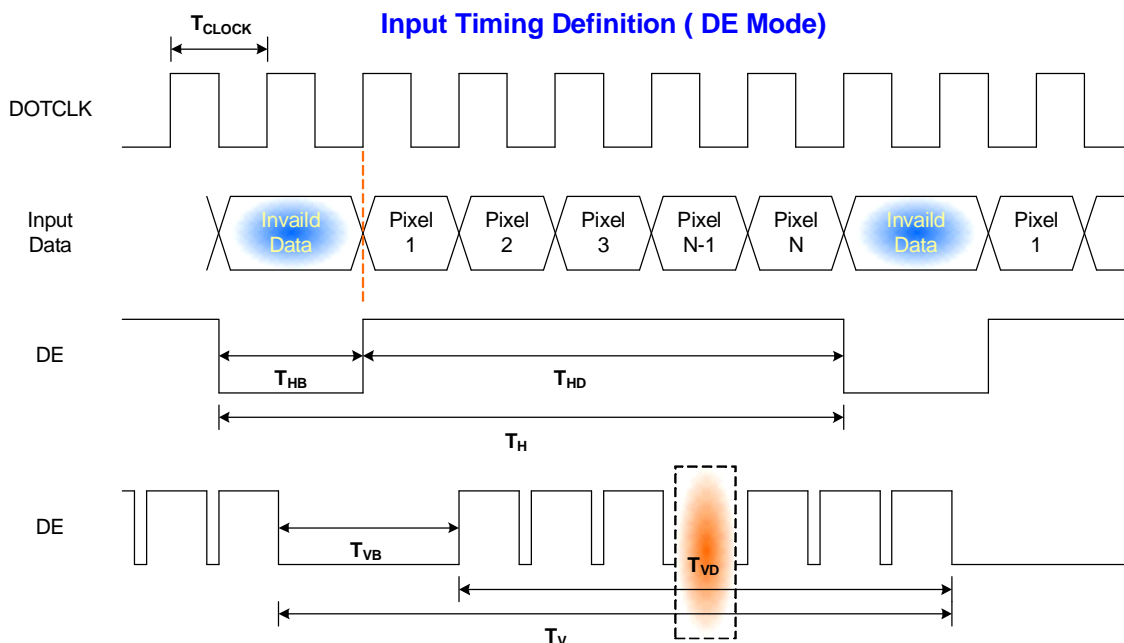
6.4.1 Timing Characteristics

Basically, interface timings should match the 1280x800 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	50	60	-	Hz
Clock frequency		$1/T_{\text{Clock}}$	62	68	72	MHz
Vertical Section	Period	T_V	803	816	832	T_{Line}
	Active	T_{VD}	800	800	800	
	Blanking	T_{VB}	3	16	32	
Horizontal Section	Period	T_H	1302	1408	1700	T_{Clock}
	Active	T_{HD}	1280	1280	1280	
	Blanking	T_{HB}	22	2	420	
End-frame checking period		tEF	2			T_{Line}
DE checking period		tDE	6400			T_{Line}

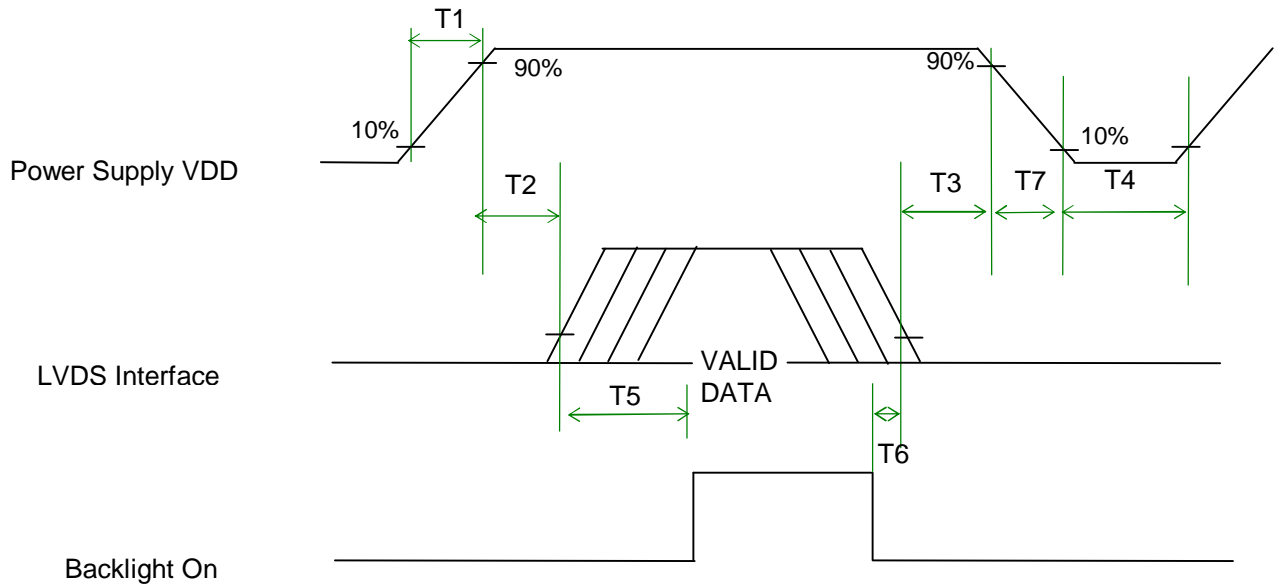
Note : DE mode only

6.4.2 Timing diagram



6.5 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



Power Sequence Timing

Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	(ms)
T2	0	-	50	(ms)
T3	0	-	50	(ms)
T4	400	-	-	(ms)
T5	200	-	-	(ms)
T6	200	-	-	(ms)
T7	0	-	10	(ms)



7. Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

Connector Name / Designation	For Signal Connector (LVDS)
Manufacturer	Hirose
Type / Part Number	DF19LA-20P-1H
Mating Housing/Part Number	DF19G-20S-1C or compatible

7.2 Backlight Unit

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Type / Part Number	SM02B-BHSS-1-TB

Since B121EW08 is a dual-CCFL model, there will be 2 connectors for CCFL, each a high voltage end and a low voltage end.

Pin #	Cable color	Signal Name
1	Red/ Blue	Lamp High Voltage
2	White	Lamp Low Voltage



8. Vibration and Shock Test

8.1 Vibration Test

Test Spec:

- I Test method: Non-Operation
- I Acceleration: 1.5G , sine wave
- I Frequency: 10 - 500Hz Random
- I Sweep: 0.5 octave/minute in each of three mutually perpendicular axes.

8.2 Shock Test Spec:

Test Spec:

- I Test method: Non-Operation
- I Acceleration: 220 G , Half sine wave
- I Active time: 2 ms
- I Pulse: Half sine wave



9. Reliability

Subject	Description
Operating High Temperature	+50°C ,Dynamic ,250hr ,Humidity 20%
Operating Low Temperature	0°C ,Dynamic ,250hr ,Humidity 20%
Storage High Temperature	+65°C ,Non_Operating ,250hr ,Humidity 20%
Storage Low Temperature	-20°C ,Non_Operating ,250hr
High Temp &High Humidity	+40°C ,Dynamic ,Humidity 95% ,250hr
Temperature Cycling Non-Operating	-40°C to +65°C ,Ramp< 20°C /min, Duration at Temp. = 30 min, Test Cycles =50
Altitude	Op(0~14000 ft) Non-op (0~40000ft)
MTBF	200K hrs
Storage Shock	180g's, 2.0 ms, Half Sine Wave \pm 3 Axis (+X, -X, +Y, -Y, +Z, -Z) 1Shocks per Direction
Storage Vibration	1.5 Grms, 30 min/side, PSD Spectrum Break Points, 26 Hz G2/Hz=0.316, 50 Hz G2/Hz=0.007, 222 Hz G2/Hz=0.0018, 500Hz G2/Hz=0.0001
ESD	Contact : \pm 8 KV Air : \pm 15 KV

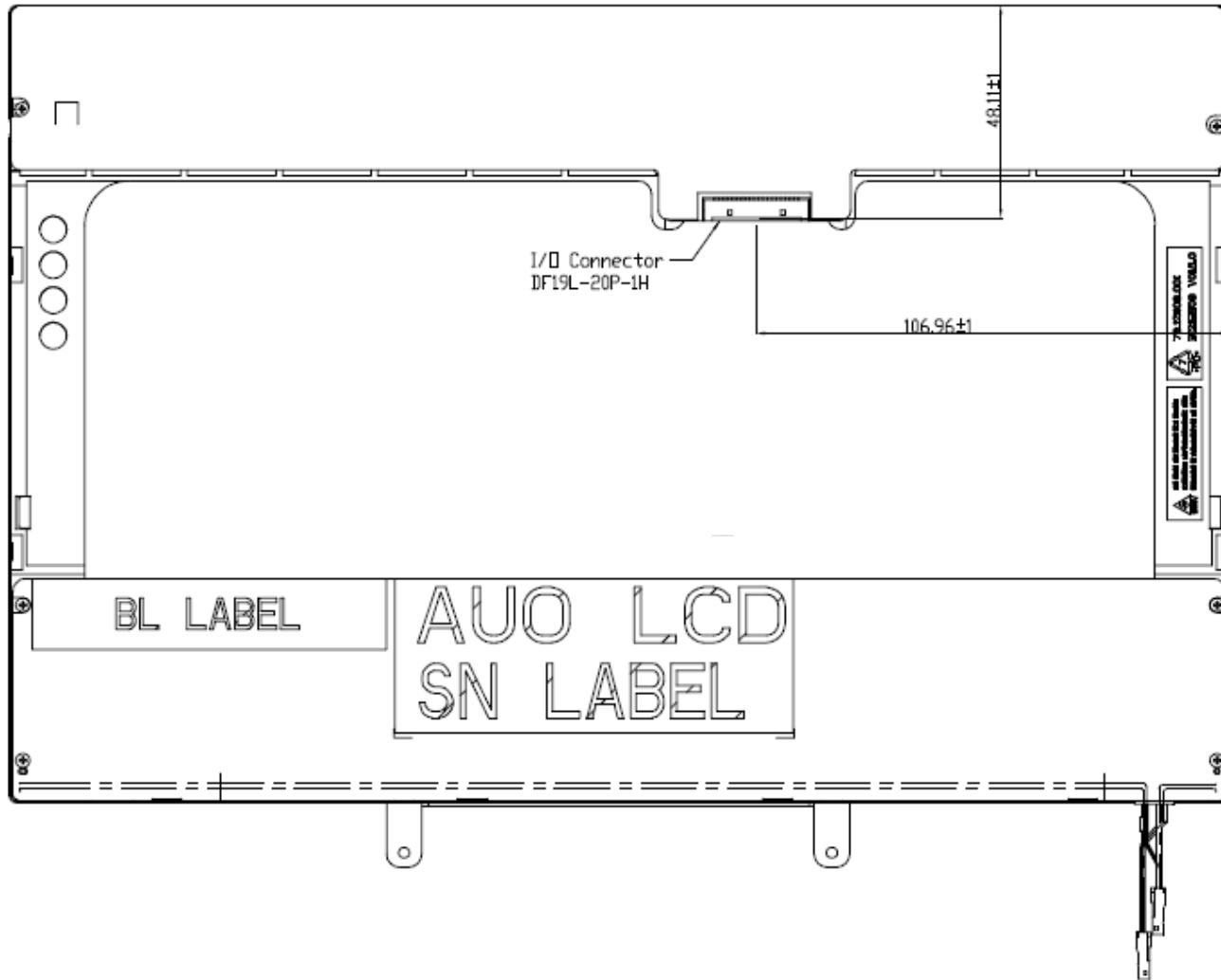
Note1: According to EN61000-4-2 , ESD class B: Some performance degradation allowed. No data lost.
Self-recoverable. No hardware failures.

Note2: MTBF (Excluding the CCFL): 30,000 hours with a confidence level 90%.

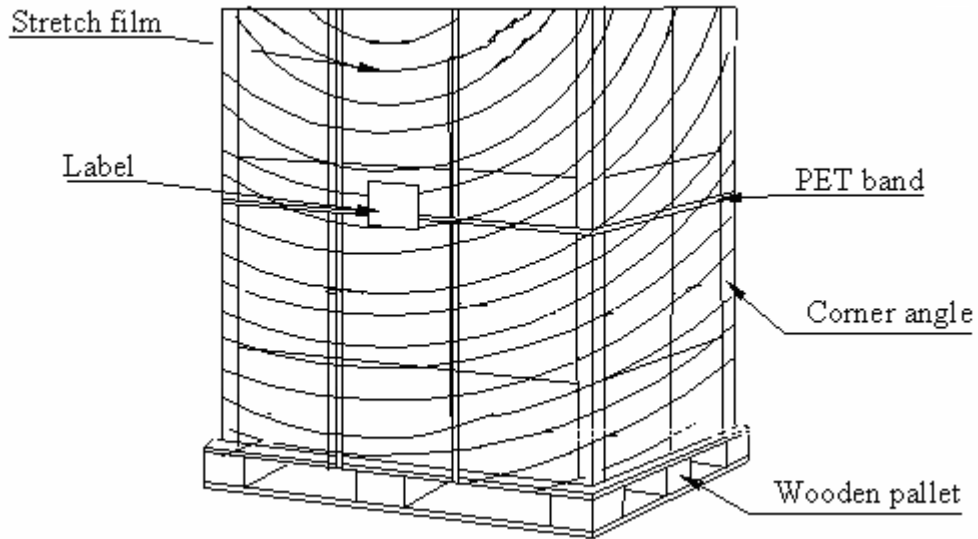


Product Specification

B121EW08 V0



11.3 Shipping package of palletizing





12. Appendix: EDID description

TBD