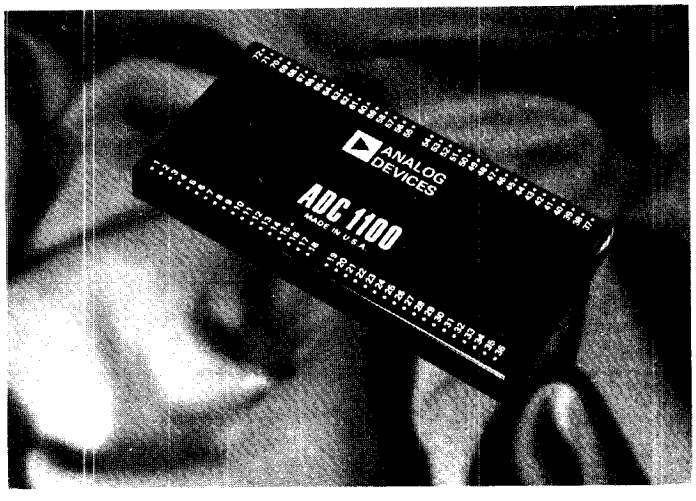
ANALOG DEVICES

Low Cost Dual Slope A/D Converter

FEATURES

- 3½ BCD Digits or 11 Bits Plus Sign
- Accepts Bipolar or Unipolar Input Signals
- Requires Only +5V Power
- 40dB Normal Mode Noise Rejection
- Analog Input Overvoltage Protected
- Automatic Zero Correction
- Can Drive Display and/or Feed Computer
- User Choice of Three Triggering Methods
- Capable of Ratiometric Operation



GENERAL DESCRIPTION

The ADC1100 is a dual slope integrating analog-to-digital converter with 3½ BCD digit or 11 binary bit resolution. It accepts an analog input signal within the nominal range of ±200mV, and converts the average value during the input integration time period to parallel output sign-magnitude BCD or sign-magnitude binary data. The unit is packaged in a small 2″ x 4″ x 0.4″ module, and requires only +5V power.

EXCELLENT NOISE REJECTION

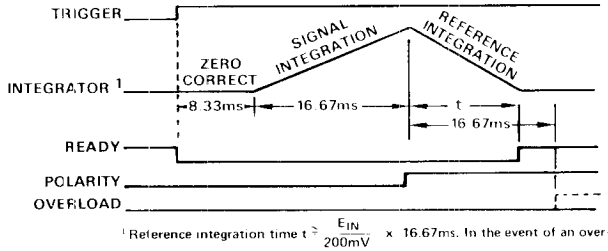
Because the ADC1100's output is based on the average value of the input signal during the input integration time period, inaccuracies due to noise spikes are greatly suppressed. In addition, with the input integration time period set equal to one cycle of the power line, the integral of any power line noise is equal to zero. This results in a normal mode power line noise rejection ratio of at least 40dB. By locking the input integration time precisely to one period of the power line using an external phase locked loop, this ratio can be increased to over 80dB. Since the excellent noise rejection is achieved without any input filtering, the analog input settling time required prior to the commencement of a conversion is zero.

APPLICATIONS

With the only power required being +5V, and with its excellent noise rejection, the ADC1100 is an ideal choice for installation at transducer locations. The BCD coded version is also well suited for many behind-the-panel applications because it allows the instrument designer complete freedom in choosing a display. For example, it may be desirable to share a single display with more than one digital output device, or to display a digital output scaled quite differently from the ADC1100/BCD's ±199.9mV input range.

TIMING INFORMATION

As shown in Figure 1, each conversion begins with an automatic zero correction cycle. Polarity data is valid anytime after the completion of the input signal integration time period, and it remains latched in one polarity until such time as a conversion is performed with an input signal of the opposite polarity. The digital output data is valid no later than 50ns prior to the READY output's "0" to "1" transition. This "set up" time is sufficient to allow the output data to be strobed into a following register or latch on the READY output's "0" to "1" edge. In the event of an overrange input signal, the OVERLOAD output will go from "0" to "1" at the end of the conversion. It will remain latched in the "1" state until a normal conversion has been performed.



[1] Reference integration time $t \geq \frac{E_{IN}}{200mV} \times 16.67ms$. In the event of an overloaded input, $t_{max} = 50ms$. (The times shown are those obtained when the unit is set for 60Hz noise rejection.)

Figure 1. Timing Diagram

SPECIFICATIONS (typical @ +25°C and +5.0V dc unless otherwise noted)

MODEL	ADC1100/BCD	ADC1100/BIN
RESOLUTION	3½ BCD digits plus sign	11 Bits Plus Sign
ACCURACY		
Relative to Full Scale	±0.05%	*
Absolute	±0.1%	*
TEMPERATURE COEFFICIENTS		
Gain TC	±50ppm/°C max	*
Offset TC	±2ppm/°C max	*
INPUT CHARACTERISTICS		
Input Range	±199.9mV	±204.7mV
Input Resolution	0.1mV/LSB	*
Input Impedance	10^9 ohms min	*
Input Bias Current	1.5nA max	*
Overvoltage Protection	±20V[1]	*
Normal Mode Rejection	40dB min @ 60Hz[2]	*
CONVERSION TIME		
Normal Conversion	42ms max[3]	*
Overload Conversion	70ms max	*
CONVERSION RATE		
Internal Trigger	4/sec	*
External Trigger	0 to 20/sec	*
Automatic	20 to 40/sec	*
DIGITAL OUTPUTS[4]		
Data Output	Positive True Logic	*
Polarity	Logic "0" = Positive Signal	*
	Logic "1" = Negative Signal	*
Ready	Logic "0" = Busy	*
	Logic "1" = Ready	*
Overload	Logic "0" = Normal	*
	Logic "1" = Overload	*
LOGIC INPUTS[5]		
Trigger Input	2 TTL Unit Loads	*
Hold Input	2 TTL Unit Loads	*
POWER SUPPLY REQUIREMENTS	+5.00V dc ±5% @ 200mA typ, 250mA max	*
POWER SUPPLY SENSITIVITY	0.01%/%ΔV_S	*
TEMPERATURE RANGE		
Operating	0 to +70°C	*
Storage	-25°C to +85°C	*

[1] Maximum voltage that can be applied to the input continuously without risking damage to the unit. Up to ±50V can be applied momentarily.

[2] Normal mode rejection at 50Hz is also 40dB minimum when unit is calibrated for 50Hz normal mode noise rejection.

[3] A normal conversion will take 42ms max when the unit is calibrated for 60Hz noise rejection. When set for 50Hz noise rejection, a normal conversion will take 50ms max.

[4] All digital outputs are rated at 6 TTL unit loads each, with a Logic "1" ≥ +2.4V @ 240μA max, and a Logic "0" ≤ +0.4V @ -9.6mA max.

[5] The trigger and hold inputs are internally tied to pull-up resistors. It is thus assured that these inputs are maintained in the high state with no connections to them. For both inputs, a Logic "1" ≥ +2.0V, and a Logic "0" ≤ +0.8V @ -3.2mA max.

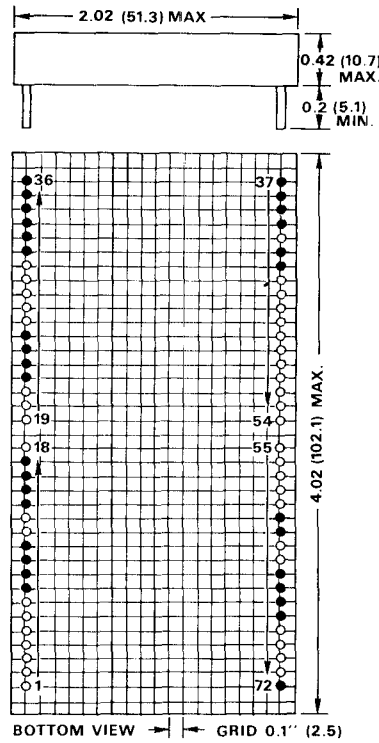
Specifications subject to change without notice.

DATA OUTPUT PIN DESIGNATIONS

PIN	14	15	16	17	22	23	24	25	31	32	33	34	35
ADC1100/BCD	1	2	4	8	10	20	40	80	100	200	400	800	1000
ADC1100/BIN	LSB	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	—	—	MSB

OUTLINE DIMENSIONS AND PIN DESIGNATIONS

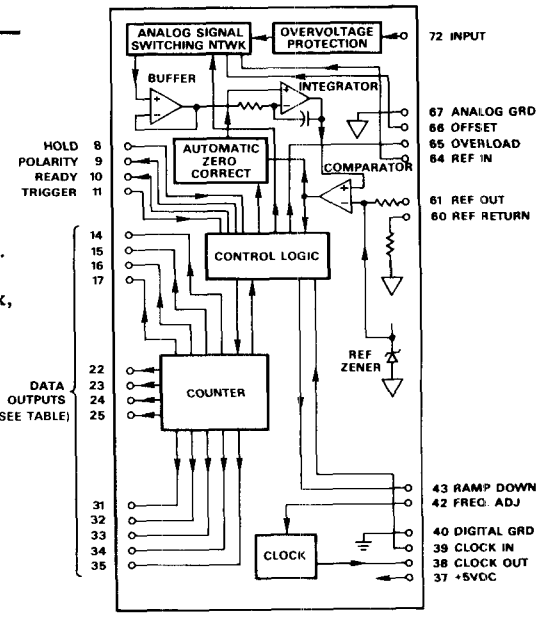
Dimensions shown in inches and (mm).



NOTE:
Terminal pins installed only in shaded hole locations. Pins 33 and 34 installed in ADC1100/BCD only. All pins are gold plated half-hard brass, (MIL-G-45 204), 0.019 (0.48) dia 0.2 (5.1) min. length.

For plug-in mounting card order Board No. AC1550

BLOCK DIAGRAM AND PIN DESIGNATIONS



CLOCK CONNECTIONS

The ADC1100 is normally connected to its own internal clock. This is accomplished by jumpering CLOCK OUT (pin 38) to CLOCK IN (pin 39). The internal clock is factory set to operate at a nominal frequency of 120kHz, which results in an input signal integration time period of 16 2/3ms. Since 16 2/3ms is equal to one cycle of a 60Hz power line, any 60Hz noise appearing on the input will have an integral of zero, and thus will not affect the digital output.

Under certain circumstances, it may be desirable to be able to adjust the internal clock's frequency. Figure 2 shows how this may be accomplished with suitable connections to pin 42 (which otherwise would have nothing connected to it).

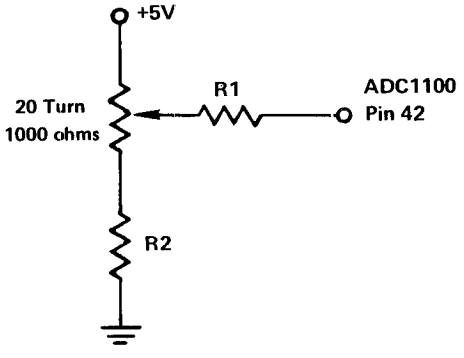


Figure 2. Clock Frequency Adjustment

With R1 = 2200 ohms and R2 = 470 ohms, this circuit can be used to optimize the rejection of 60Hz normal mode noise. The potentiometer is used to adjust the input integration time period to be exactly equal to one cycle of a power line that has a nominal frequency of 60Hz. With R1 = 470 ohms and R2 = 2700 ohms, the clock will operate at a nominal frequency of 100kHz. This gives an input integration time of 20ms, which is equal to one cycle of a 50Hz power line. The potentiometer is then used to optimize the rejection of 50Hz noise.

GAIN ADJUSTMENT

The gain of the ADC1100 is set with a 50 ohm, 20 turn potentiometer whose wiper is connected to pin 64. One end of the potentiometer is connected to pin 60, and the other end to pin 61. BCD coded units are calibrated by applying an input signal of 199.85mV and then adjusting the gain adjustment potentiometer until the converter's output is just on the verge of switching between output codes 1998 and 1999. Binary coded units are calibrated by applying a 204.65mV input and adjusting the gain potentiometer until the converter's output is just on the verge of switching from 11111111110 to 11111111111. If exact gain calibration is not required, the gain adjustment potentiometer can be deleted, and pins 60, 61, and 64 are then jumpered together.

OFFSET ADJUSTMENT

The ADC1100 goes into an automatic zero correction cycle at the beginning of each conversion. It does not, therefore, require any external zero or offset adjustment. However, in the event the input signal contains an externally generated offset of up to ±1mV, it could be cancelled out with the circuit shown in Figure 3 (pin 66 normally has nothing connected to it).

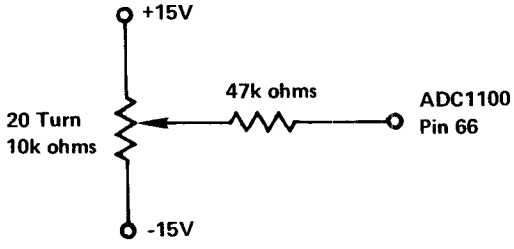


Figure 3. Offset Adjustment

TRIGGERING CONVERSIONS

The ADC1100 may be triggered in any of three ways. The first is the easiest to implement. With no connections to TRIGGER (pin 11) or HOLD (pin 8), the unit will continuously perform conversions at the rate of about 4 conversions/second. With no connections to TRIGGER (pin 11), and with HOLD (pin 8) jumpered to READY (pin 10), the ADC1100 will perform continuous conversions, with a new conversion beginning as soon as the conversion in progress is completed. The READY output (pin 10) remains at a Logical "1" for approximately 100ns between conversions. The conversion rate depends upon the magnitude of the input signal. With the clock operating at 120kHz (for optimum rejection of 60Hz noise), and with a nonoverloaded input, that rate will vary from about 23/sec. to about 40/sec.

Finally, the ADC1100 can be commanded to make a conversion upon receipt of an externally generated pulse. Figure 4A shows how the unit is triggered with a positive-going pulse, and Figure 4B describes triggering with a negative-going pulse.

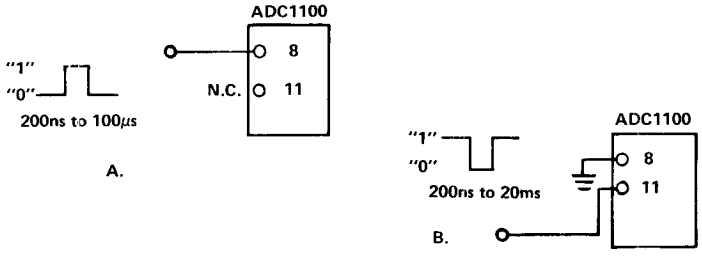


Figure 4. External Triggering

When using a positive-going trigger pulse the conversion commences (and the READY output goes from "1" to "0") approximately 100ns after the leading edge ("0" to "1" transition) of the trigger pulse. When using a negative-going pulse, the conversion begins about 100ns following the pulse's trailing edge ("0" to "1" transition). Should a trigger pulse be received while a conversion is in progress, it will be ignored, and the conversion in progress will continue to completion.

POWER AND GROUND CONNECTIONS

Digital ground (pin 40) and analog ground (pin 67) should be tied together externally with a good ground bus connection. Care should be taken to ensure that no digital ground return signals are carried in the analog input's ground return lead. The +5V power input is internally bypassed with a 10μF capacitor, but additional bypass capacitance can be added externally if desired. Analog Devices' model 906 modular power supply is an ideal power source for the ADC1100. It supplies +5V at up to 250mA.

LATCHED DATA OUTPUTS

When the digital outputs of the ADC1100/BCD are used to drive a display, it may be desirable to have the data latched to keep the display from blinking. This can be easily accomplished using only two external digital ICs, as shown in Figure 5. Note that no latching circuitry is shown for the overload, sign, and "1000" outputs. None is required. These outputs are latched, and, therefore, do not require external latching. The latched data is updated on the "0" to "1" transition of the READY output (pin 10), which occurs at the completion of each conversion.

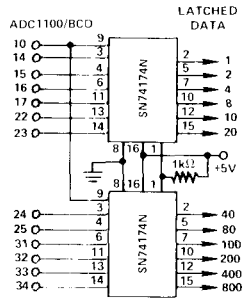


Figure 5. External Data Latches

MAXIMUM POWER LINE NOISE REJECTION

When maximum rejection of power line originated noise is needed, the circuitry shown in Figure 6 may be used to give the ADC1100 a power line noise rejection ratio of over 80dB. This circuit is a phase locked loop that locks the input signal integration time period to be exactly equal to one cycle of the line voltage applied to the primary of the 115V ac to 6.3V ac transformer.

It can be used with either 50Hz or 60Hz power lines. Because of the long time constant in the phase locked loop, it may take as long as three minutes for the loop to lock onto the power line frequency following initial power turn-on.

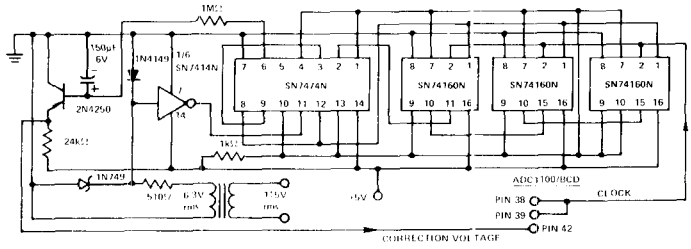


Figure 6a. Phase Locked Clock Circuitry For ADC1100/BCD

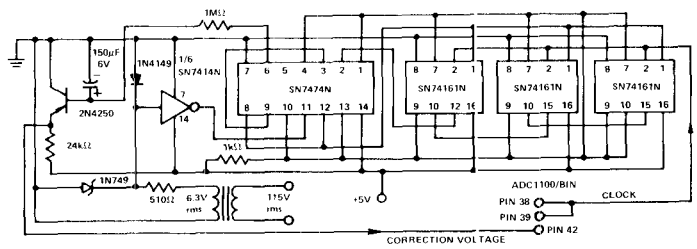


Figure 6b. Phase Locked Clock Circuitry For ADC1100/BIN

USING EXTERNAL COUNTERS

The ADC1100 can be used to produce an output pulse train, the number of pulses in which is proportional to the analog input voltage. This pulse train output can be applied to external counters to implement nearly any counting scheme desired. For example, Figure 7 shows a circuit using the ADC1100/BCD which gives a full scale count of 9995, where the least significant digit has only two possible values, 0 or 5. The counter would count in the following sequence: 1890, 1895, 1900, 1905, etc.

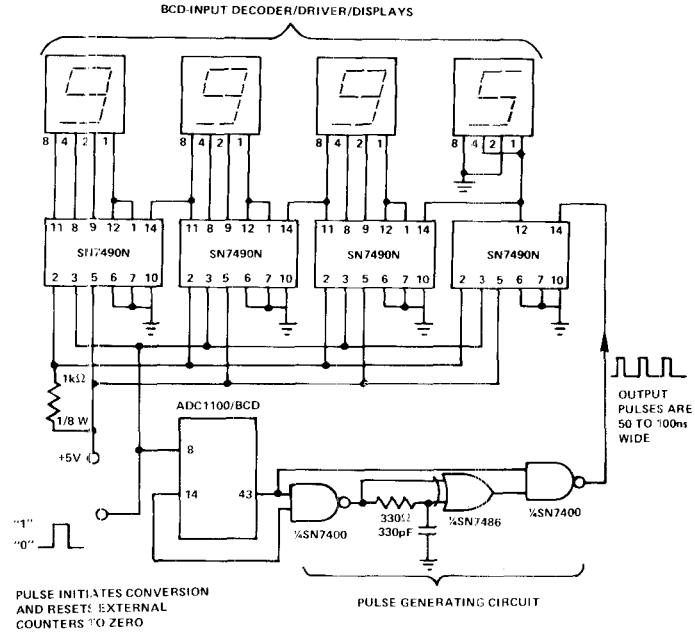


Figure 7. External Count-by-5 Counter

When designing external counter systems, it is only necessary to remember that BCD coded units produce exactly 1999 pulses and binary coded units produce exactly 2047 pulses for plus or minus full scale inputs. Smaller inputs yield proportionately smaller numbers of pulses. The "Pulse Generating Circuit" of Figure 7 can be used with either binary or BCD coded units.

RATIOMETRIC OPERATION

There may be instances where it would be desirable to measure the ratio of two voltages, rather than the specific value of one voltage. For example, the ratio of a strain gauge load cell's output to its excitation voltage may be highly accurate **and** repeatable, but the excitation voltage itself may vary somewhat. If the excitation voltage is applied to the reference input (pin 64) and the cell's output is applied to the analog input (pin 72), then the ADC1100's digital output will be the ratio of the two: digital output = V_{IN}/V_{REF} x (Full Scale Digital Output). Thus, variations in the excitation voltage will not affect the digital output. The voltage source driving the reference input should have a source impedance of 1000ohms or less. For best operation, the reference input voltage should be kept within the range of +100mV to +300mV, but in any case cannot exceed ±1V without risking damage to the unit. Care should be taken to ensure that the reference voltage is accurately referred to analog ground (pin 67). The ADC1100 will exhibit a gain TC of ±15ppm/°C or better in this mode of operation.