ACT8840

Rev 1, 07-Feb-14

Advanced PMU for Single-core Application Processors

FEATURES

INTEGRATED POWER SUPPLIES

- **Four DC/DC Step-Down (Buck) Regulators**
  - **2 x 1.8A, 2 x 1.3A**
- **Five Low-Noise LDOs**
  - **2 x 150mA, 3 x 350mA**
- **Three Low-Input Voltage LDOs**
  - **1 x 150mA, 2 x 350mA**
- **One Low IQ Keep-Alive LDO**
- **Backup Battery Charger**

SYSTEM CONTROL AND INTERFACE

- **Six General Purpose I/O with PWM Drivers**
- **I²C Serial Interface**
- **Interrupt Controller**

e and Sequencing Controller

- **Power on Reset**
- **Soft / Hard Reset**
- **Watchdog Supervision**
- **Multiple Sleep Modes**

- **Thermal Management Subsystem**

APPLICATIONS

- **Tablet PC**
- **Mobile Internet Devices (MID)**
- **Ebooks**
- **Personal Navigation Devices**

GENERAL DESCRIPTION

The ACT8840 is a complete, cost effective, and highly-efficient *ActivePMU™* power management solution optimized for the power, voltage sequencing and control requirements of general Single-core application processor.

The ACT8840 features four fixed-frequency,

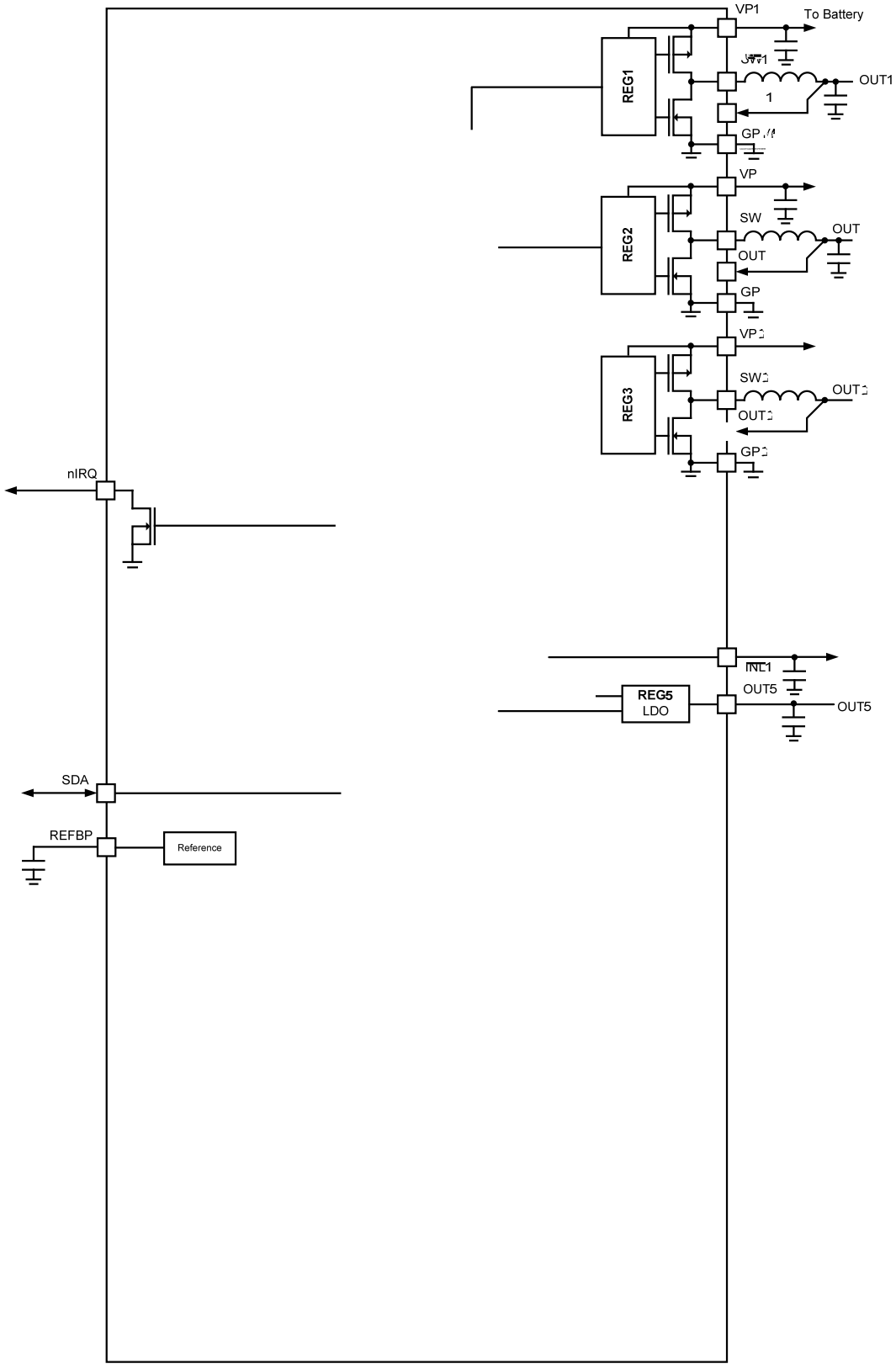
converters that achieve peak efficiencies of up to 97%. These regulators operate with a fixed frequency of 2.25MHz, minimizing noise in sensitive applications and allowing the use of small external components. These buck regulators supply up to 1.8A of output current and can fully satisfy the power and control requirements of the single-core application processor. Dynamic Voltage Scaling (DVS) is supported either by dedicated control pins, or through I²C interface to optimize the energy-per-task performance for the processor. This device also include eight low-noise LDOs (up to 350mA per LDO), one always-ON LDO and an integrated backup battery charger to provide a complete power system for the processor.

The power sequence and reset controller provides power-on reset, SW-initiated reset, and power cycle reset for the processor. It also features the watchdog supervisory function. Multiple sleep modes with autonomous sleep and wake-up sequence control are supported.

The thermal management and protection subsystem allows the host processor to manage the power dissipation of the PMU and the overall system dynamically. The PMU provides a thermal warning to the host processor when the temperature reaches a certain threshold such that the system can turn off some of the non-essential functions, reduce the clock frequency and etc to manage the system temperature.

The ACT8840 is available in a compact, Pb-Free and RoHS-compliant TQFN66-48 package.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1, 2		

ABSOLUTE MAXIMUM RATINGS [i]

PARAMETER	VALUE	UNIT
INL1, INL2, INL3 to GA; VP1, SW1, OUT1 to GP14; VP2, SW2, OUT2 to GP2; VP3, SW3, OUT3 to GP3; VP4, SW4, OUT4 to GP14	-0.3 to 6	V
GP14, GP2, GP3 to GA	-0.3 to + 0.3	V
OUT5, OUT6, OUT7, OUT13 to GA	-0.3 to INL1 + 0.3	V
OUT8, OUT9, GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, VSELR2, nPBIN, nRSTO, nIRQ, nPBSTAT, PWREN, PWRHLD, REFBP, SCL, SDA to GA	-0.3 to INL2 + 0.3	V
OUT10, OUT11, OUT12 to GA	-0.3 to INL3 + 0.3	V
Junction to Ambient Thermal Resistance	21	°C/W
Operating Ambient Temperature Range	-40 to 85	°C
Operating Junction Temperature	-40 to 125	°C
Storage Temperature	-55 to 150	°C
Lead Temperature (Soldering, 10 sec)	300	°C

¡ : Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

I²C INTERFACE ELECTRICAL CHARACTERISTICS

(V_{INL2} = 3.6V, T_A = 25°C, unless otherwise specified.)

Figure 1:
I²C Compatible Serial Bus Timing

GLOBAL REGISTER MAP CONT'D

BLOCK	ADDRESS		BITS							
			D7	D6	D5	D4	D3	D2	D1	D0
REG9	0x70	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT [i]	0	1	1	1	0	1	0	0
REG9	0x71	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	DIS	nFLTMSK	OK
		DEFAULT [i]	1	1	0	0	0	1	0	R
REG10	0x80	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT [i]	0	1	1	1	1	0	0	1
REG10	0x81	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	DIS	nFLTMSK	OK
		DEFAULT [i]	1	1	0	1	0	1	0	R
REG11	0x90	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT [i]	0	1	1	0	0	1	0	0
REG11	0x91	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	DIS	nFLTMSK	OK
		DEFAULT [i]	1	1	0	1	0	1	0	R
REG12	0xA0	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT [i]	0	1	1	1	1	0	0	1
REG12	0xA1	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	DIS	nFLTMSK	OK
		DEFAULT [i]	1	1	0	1	0	1	0	R
REG13	0xB1	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*
		DEFAULT [i]	1	0	0	0	0	0	0	0
PB	0xC0	NAME	PBAMSK	PBDMSK	*Reserved*	*Reserved*	*Reserved*	*Reserved*	WDSREN	WDPCEN
		DEFAULT [i]	0	0	0	0	0	0	0	0
PB	0xC1	NAME	INTADR [7]	INTADR [6]	INTADR [5]	INTADR [4]	INTADR [3]	INTADR [2]	INTADR [1]	INTADR [0]
		DEFAULT [i]	R	R	R	R	R	R	R	R
PB	0xC2	NAME	PBASTAT	PBDSTAT	PBDAT	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*
		DEFAULT [i]	R	R	R	R	R	R	R	R
PB	0xC3	NAME	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	SIPC
		DEFAULT [i]	0	0	0	0	0	0	0	0
PB	0xC5	NAME	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	PCSTAT	SRSTAT
		DEFAULT [i]	0	0	0	0	0	0	R	R
GPIO6	0xE3	NAME	PWM6EN	FRE6[2]	FRE6[1]	FRE6[0]	DUTY6[3]	DUTY6[2]	DUTY6[1]	DUTY6[0]
		DEFAULT [i]	0	0	0	0	0	0	0	0
GPIO5	0xE4	NAME	PWM5EN	FRE5[2]	FRE5[1]	FRE5[0]	DUTY5[3]	DUTY5[2]	DUTY5[1]	DUTY5[0]
		DEFAULT [i]	0	0	0	0	0	0	0	0
GPIO3	0xF4	NAME	PWM3EN	FRE3[2]	FRE3[1]	FRE3[0]	DUTY3[3]	DUTY3[2]	DUTY3[1]	DUTY3[0]
		DEFAULT [i]	0	0	0	0	0	0	0	0
GPIO4	0xF5	NAME	PWM4EN	FRE4[2]	FRE4[1]	FRE4[0]	DUTY4[3]	DUTY4[2]	DUTY4[1]	DUTY4[0]
		DEFAULT [i]	0	0	0	0	0	0	0	0
GPIO1	0xE5	NAME	PWM1EN	FRE1[2]	FRE1[1]	FRE1[0]	DUTY1[3]	DUTY1[2]	DUTY1[1]	DUTY1[0]
		DEFAULT [i]	0	0	0	0	0	0	0	0
GPIO2	0xF3	NAME	PWM2EN	FRE2[2]	FRE2[1]	FRE2[0]	DUTY2[3]	DUTY2[2]	DUTY2[1]	DUTY2[0]
		DEFAULT [i]	0	0	0	0	0	0	0	0

¡ : Default values of ACT8840QM188-T.

REGISTER AND BIT DESCRIPTIONS

BLOCK	ADDRESS	BIT	NAME	ACCESS	DESCRIPTION
SYS	0x00	[7]	nBATLEVMSK	R/W	Battery Voltage Level Interrupt Mask. Set this bit to 1 to unmask the interrupt. See the *Programmable Battery Voltage Monitor* section for more information
SYS	0x00	[6]	nBATSTAT	R	Battery Voltage Status. Value is 1 when BATLEV interrupt is generated, value is 0 otherwise.
SYS	0x00	[5]	VBATDAT	R	Battery Voltage Monitor real time status. Value is 1 when VBAT < BATLEV, value is 0 otherwise.
SYS	0x00	[4]	-	R/W	Reserved.
SYS	0x00	[3:0]	BATLEV	R/W	Battery Voltage Detect Threshold. Defines the BATLEV voltage threshold. See the *Programmable Battary Voltage Monitor* section for more information.
SYS	0x01	[7]	nTMSK	R/W	Thermal Interrupt Mask. Set this bit to 1 to unmask the interrupt.
SYS	0x01	[6]	TSTAT	R	Thermal Interrupt Status. Value is 1 when a thermal interrupt is generated, value is 0 otherwise.
SYS	0x01	[5:0]	-	R/W	Reserved.
REG1	0x10	[7:6]	-	R	Reserved.
REG1	0x10	[5:0]	VSET0	R/W	Primary Output Voltage Selection. See the *Output Voltage Programming* section for more information
REG1	0x12	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG1	0x12	[6:3]	-	R	Reserved.
REG1	0x12	[2]	PHASE	R/W	Regulator Phase Control. Set bit to 1 for the regulator to operate 180° out of phase with the oscillator, clear bit to 0 for the regulator to operate in phase with the oscillator.
REG1	0x12	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG1	0x12	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG2	0x20	[7:6]	-	R	Reserved.
REG2	0x20	[5:0]	VSET0	R/W	Primary Output Voltage Selection. Valid when VSEL is driven low. See the *Output Voltage Programming* section for more information
REG2	0x21	[7:6]	-	R	Reserved.
REG2	0x21	[5:0]	VSET1	R/W	Secondary Output Voltage Selection. Valid when VSEL is driven high. See the *Output Voltage Programming* section for more information

REGISTER AND BIT DESCRIPTIONS CONT'D

BLOCK	ADDRESS	BIT	NAME	ACCESS	DESCRIPTION
REG6	0x59	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG6	0x59	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG7	0x60	[7:6]	-	R	Reserved.
REG7	0x60	[5:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG7	0x61	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG7	0x61	[6:3]	-	R	Reserved.
REG7	0x61	[2]	DIS	R/W	Output Discharge Control. When activated, LDO output is discharged to Pks4j[gh.6 5ge

REGISTER AND BIT DESCRIPTIONS CONT'D

BLOCK	ADDRESS	BIT	NAME	ACCESS	DESCRIPTION
REG10	0x81	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG10	0x81	[6:3]	-	R	Reserved.
REG10	0x81	[2]	DIS	R/W	Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG10	0x81	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG10	0x81	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG11	0x90	[7:6]	-	R	Reserved.
REG11	0x90	[5:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG11	0x91	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG11	0x91	[6:3]	-	R	Reserved.
REG11	0x91	[2]	DIS	R/W	Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG11	0x91	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG11	0x91	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG12	0xA0	[7:6]	-	R	Reserved.
REG12	0xA0	[5:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG12	0xA1	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG12	0xA1	[6:3]	-	R	Reserved.
REG12	0xA1	[2]	DIS	R/W	Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG12	0xA1	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG12	0xA1	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG13	0xB1	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG13	0xB1	[6:0]	-	R	Reserved.
PB	0xC0	7	nPBAMSK	R/W	nPBIN Assertion Interrupt Control. Set this bit to 1 to generate an interrupt when nPBIN is asserted.
PB	0xC0	6	nPBDMSK	R/W	nPBIN De-assertion Interrupt Control. Set this bit to 1 to generate an interrupt when nPBIN is de-asserted.

REGISTER AND BIT DESCRIPTIONS CONT'D

BLOCK	ADDRESS	BIT	NAME	ACCESS	DESCRIPTION
PB	0xC0	[5:2]	-	R	Reserved.
PB	0xC0	1	WDSREN	R/W	Watchdog Soft-Reset Enable. Set this bit to 1 to enable watchdog function. When the watchdog timer expires, the PMU commences a soft-reset routine. This bit is automatically reset to 0 when entering sleep mode.
PB	0xC0	0	WDPCEN	R/W	Watchdog Power-Cycle Enable. Set this bit to 1 to enable watchdog function. When watchdog timer expires, the PMU commence a power cycle. This bit is automatically reset to 0 when entering sleep mode.
PB	0xC1	[7:0]	INTADR	R	Interrupt Address. It holds the address of the block that triggers the interrupt. This byte defaults to 0xFF and is automatically set to 0xFF after being read. Bit 7 is the MSB while Bit 0 is the LSB.
PB	0xC2	7	PBASTAT	R	nPBIN Assertion Interrupt Status. The value of this bit is 1 if the nPBIN Assertion Interrupt is triggered.
PB	0xC2	6	PBDSTAT	R	nPBIN De-assertion Interrupt Status. The value of this bit is 1 if the nPBIN De-assertion Interrupt is triggered.
PB	0xC2	5	PBASTAT	R	nPBIN Status bit. This bit contains the real-time status of the nPBIN pin. The value of this bit is 1 if nPBIN is asserted, and is 0 if nPBIN is de-asserted.
PB	0xC2	[4:0]	-	R	Reserved.
PB	0xC3	[7:1]	-	R	Reserved.
PB	0xC3	0	SIPC	R/W	Software Initiated Power Cycle. When this bit is set, the PMU commences a power cycle after 8ms delay.
PB	0xC5	[7:2]	-	R	Reserved.
PB	0xC5	1	PCSTAT	R/W	Power-cycle Flag. The value of this bit is 1 after a power cycle. This bit is automatically cleared to 0 after read.
PB	0xC5	0	SRSTAT	R/W	Soft-reset Flag. The value of this bit is 1 after a soft-reset. This bit is automatically cleared to 0 after read.
GPIO6	0xE3	[7]	PWM6EN	R/W	PWM Function Enable. Set 1 to enable PWM function of GPIO6.
GPIO6	0xE3	[6:4]	FRE6	R/W	PWM Frequency Selection Bits for GPIO6. See the Table 6 for code to frequency cross.
GPIO6	0xE3	[3:0]	DUTY6	R/W	Duty Cycle Selection Bits for GPIO6. See the Table 7 for code to duty cross.
GPIO5	0xE4	[7]	PWM5EN	R/W	PWM Function Enable. Set 1 to enable PWM function of GPIO5.
GPIO5	0xE4	[6:4]	FRE5	R/W	PWM Frequency Selection Bits for GPIO5. See the Table 6 for code to frequency cross.
GPIO5	0xE4	[3:0]	DUTY5	R/W	Duty Cycle Selection Bits for GPIO5. See the Table 7 for code to duty cross.
GPIO3	0xF4	[7]	PWM3EN	R/W	PWM Function Enable. Set 1 to enable PWM function of GPIO3.
GPIO3	0xF4	[6:4]	FRE3	R/W	PWM Frequency Selection Bits for GPIO3. See the Table 6 for code to frequency cross.
GPIO3	0xF4	[3:0]	DUTY3	R/W	Duty Cycle Selection Bits for GPIO3. See the Table 7 for code to duty cross.
GPIO4	0xF5	[7]	PWM4EN	R/W	PWM Function Enable. Set 1 to enable PWM function of GPIO4.
					PWM Frequency Selectio Pts for GPIO3. See the4Table56 for [illegible]
GPIO3	0xF4	43:0]	DUTY3	R/W	

SYSTEM CONTROL ELECTRICAL CHARACTERISTICS

(V_{INL2} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Range		3.0		5.5	V
UVLO Threshold Voltage	V_{INL2} Rising	2.6	2.8	3.0	V
UVLO Hysteresis	V_{INL2} Hysteresis		200		mV
Operating Supply Current	All Regulators Enabled but no load		0.6	1.2	mA
Shutdown Supply Current	All Regulators Disabled except REG13		10	20	µA
Oscillator Frequency		2.0	2.25	2.5	MHz
Logic High Input Voltage		1.4			V
Logic Low Input Voltage				0.4	V
Leakage Current	V[nIRQ] = V[nRSTO] = 4.2V			1	µA
Low Level Output Voltage	nIRQ, nRSTO, ISINK = 5mA			0.3	V
Thermal Shutdown Temperature	Temperature rising		160		°C
Thermal Shutdown Hysteresis			20		°C

STEP-DOWN DC/DC ELECTRICAL CHARACTERISTICS

(V_{VP1} = V_{VP2} = V_{VP3} = V_{VP4} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		2.7		5.5	V
UVLO Threshold	Input Voltage Rising	2.5	2.6	2.7	V
UVLO Hysteresis	Input Voltage Falling		100		mV
Standby Supply Current	V_{OUT} = 103%, Regulator Enabled		72	100	µA
Shutdown Current	V_{VP} = 5.5V, Regulator Disabled		0	2	µA
Output Voltage Accuracy	V_{OUT} ≥ 1.0V, I_{OUT} = 10mA	-1%	V_{NOM} ¡	1%	V
	V_{OUT} < 1.0V, I_{OUT} = 10mA	-10		10	mV
Line Regulation	V_{VP} = Max (V_{NOM}① +1V, 3.2V) to 5.5V		0.15		%/V
Load Regulation REG1/4	I_{OUT} = 10mA to IMAX②		1.70		%/A
Load Regulation REG2/3	I_{OUT} = 10mA to IMAX②		1.00		%/A
Power Good Threshold	V_{OUT} Rising		93		%V_{NOM}
Power Good Hysteresis	V_{OUT} Falling		2		%V_{NOM}
Switching Frequency	V_{OUT} ≥ 20% of V_{NOM}	2	2.25	2.5	MHz
	V_{OUT} = 0V		550		kHz
Soft-Start Period			400		µs
Minimum On-Time			75		ns
REG1 AND REG4					
Maximum Output Current		1.3			A
Current Limit		1.6	2.1	2.6	A
PMOS On-Resistance	I_{SW} = -100mA		0.14		Ω
NMOS On-Resistance	I_{SW} = 100mA		0.08		Ω
SW Leakage Current	V_{VP} = 5.5V, V_{SW} = 0 or 5.5V		0	2	µA
Input Capacitor			4.7		µF
Output Capacitor			33		µF
Power Inductor		1.0	2.2	3.3	µH
REG2 AND REG3					
Maximum Output Current		1.8			A
Current Limit		2.3	2.8	3.4	A
PMOS On-Resistance	I_{SW} = -100mA		0.095		Ω
NMOS On-Resistance	I_{SW} = 100mA		0.08		Ω
SW Leakage Current	V_{VP} = 5.5V, V_{SW} = 0 or 5.5V		0	2	µA
Input Capacitor			10		µF
Output Capacitor			44		µF
Power Inductor		0.5	1	2.2	µH

¡ : V_{NOM} refers to the nominal output voltage level for V_{OUT} as defined by the *Ordering Information* section.

②: IMAX Maximum Output Current.

LOW-NOISE LDO ELECTRICAL CHARACTERISTICS

(V_{INL1} = V_{INL2} = 3.6V, C_{OUT5} = C_{OUT6} = C_{OUT7} = C_{OUT8} = C_{OUT9} = 2.2µF, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		2.5		5.5	V
	V_{OUT} ≥ 1.0V, I_{OUT} = 10mA	-1	V_{NOM} ¡	1	%
	V_{OUT} < 1.0V, I_{OUT} = 10mA	-10	n	mV	
Line Regulation	V_{INL} = Max (V + 0.5V, 3.6V) to 5.5V	0.5		mV	
Load Regulation	I_{OUT} = 1mA to IMAX②		0.1		V/A
Power Supply Rejection Ratio	f = 1kHz, I_{OUT} = 20mA, V_{OUT} = 1.2V		75	n	
	f = 10kHz, I_{OUT} = 20mA, V_{OUT} =		65	0( )]TJ-29.6067 -2.3333 TD-.0007 Tc.002 Regulator Enabled Regulator Disabled	dB
	Soft-Start Period			V	
	$_{OUT}$ = 3.0V	140		µs	
Power Good Threshold V	$_{OUT}$ Rising	92	n	Power Good Hysteresis	V
	$_{OUT}$ Falling	3.5		%	
Output Noise	I_{OUT} = 20mA, f = 10Hz to 100kHz, V_{OUT} = 1.2V		30	µV	$_{RMS}$
Discharge Resistance	LDO Disabled, DIS[ ] = 1	1.5	k		Ω
LDO rated at 150mA (REG5 & REG6)					
Dropout Voltage £	I_{OUT} = 80mA, V_{OUT} > 3.1V		140	280	

¡ : V_{NOM} refers to the nominal output voltage level for V_{OUT} as defined by the *Ordering Information* section.

②: IMAX Maximum Output Current.

③: Dropout Voltage is defined as the differential voltage between input and output when the output voltage drops 100mV below the regulation voltage (for 3.1V output voltage or higher).

¤: LDO current limit is defined as the output current at which the output voltage drops to 95% of the respective regulation voltage. Under heavy overload conditions the output current limit folds back by 50% (typ.).

LOW-INPUT VOLTAGE LDO ELECTRICAL CHARACTERISTICS

(V_{INL3} = 3.6V, C_{OUT10} = C_{OUT11} = C_{OUT12} = 2.2µF, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		1.7		5.5	V
Output Voltage Accuracy	V_{OUT} ≥ 1.0V, I_{OUT} = 10mA	-1	V_{NOM} ¡	1	%
	V_{OUT} < 1.0V, I_{OUT} = 10mA	-10		10	mV
Line Regulation	V_{INL} = Max (V_{OUT} + 0.5V, 3.6V) to 5.5V		0.5		mV
Load Regulation	I_{OUT} = 1mA to IMAX②		0.1		V/A
Power Supply Rejection Ratio	f = 1kHz, I_{OUT} = 20mA, V_{OUT} = 1.2V		50		dB
	f = 10kHz, I_{OUT} = 20mA, V_{OUT} = 1.2V		40		
Supply Current per Output	Regulator Enabled		22		µA
	Regulator Disabled		0	2	
Soft-Start Period	V_{OUT} = 3.0V		100		µs
Power Good Threshold	V_{OUT} Rising		92		%
Power Good Hysteresis	V_{OUT} Falling		3.5		%
Output Noise	I_{OUT} = 20mA, f = 10Hz to 100kHz, V_{OUT} = 1.2V		30		μV_{RMS}
Discharge Resistance	LDO Disabled, DIS[ ] = 1		1.5		kΩ
LDO rated at 150mA (REG10)					
Dropout Voltage£	I_{OUT} = 80mA, V_{OUT} > 3.1V		100	200	mV
Maximum Output Current		150			mA
Current Limit¤	V_{OUT} = 95% of regulation voltage	180			mA
Recommend Output Capacitor			2.2		µF
LDO rated at 350mA (REG11 & REG12)					
Dropout Voltage£	I_{OUT} = 160mA, V_{OUT} > 3.1V		100	200	mV
Maximum Output Current		350			mA
Current Limit¤	V_{OUT} = 95% of regulation voltage	400			mA
Recommend Output Capacitor			2.2		µF

¡ : V_{NOM} refers to the nominal output voltage level for V_{OUT} as defined by the *Ordering Information* section.

②: IMAX Maximum Output Current.

③: Dropout Voltage is defined as the differential voltage between input and output when the output voltage drops 100mV below the regulation voltage (for 3.1V output voltage or higher).

¤: LDO current limit is defined as the output current at which the output voltage drops to 95% of the respective regulation voltage. Under heavy overload conditions the output current limit folds back by 50% (typ.).

LOW-POWER(ALWAYS-ON) LDO ELECTRICAL CHARACTERISTICS

(V_{INL1} = 3.6V, C_{OUT13} = 1µF, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
REG13					
Operating Voltage Range		2.5		5.5	V
Output Voltage Accuracy		-3	V_{NOM} [i]	3	%
Line Regulation	V_{INL1} = Max (V_{OUT} + 0.2V, 2.5V) to 5.5V		13		mV
Supply Current from V_{INL1}			5		µA
Maximum Output current		50			mA
Recommend Output Capacitor		0.47			µF

PWM LED DRIVER ELECTRICAL CHARACTERISTICS

(V_{INL2} = 3.6V, T_A = 25°C, unless otherwise specified.)

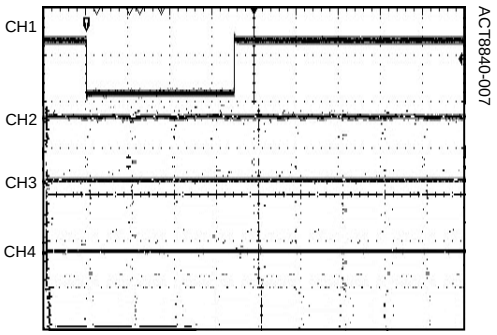
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Current	100% Duty Cycle	6	10	16	mA
Output Low Voltage	Feed in with 6mA			0.35	V
Leakage Current	Sinking from 5.5V source			1	µA
PWM Frequency	FRE[2:0] = 000		0.25		Hz
PWM Duty Adjustment	DUTY[3:0] = 0000 to 1111	6.25		100	%

¡ : V_{NOM} refers to the nominal output voltage level for V_{OUT} as defined by the *Ordering Information* section.

TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(T_A = 25°C, unless otherwise specified.)

Sleep of PWREN, OUT1/3/9

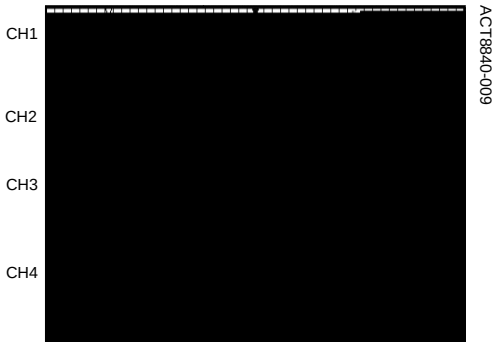


CH1: V_{PWREN}, 3V/div
CH2: V_{OUT1}, 2V/div
CH3: V_{OUT3}, 1V/div
CH4: V_{OUT9}, 2V/div
TIME: 4ms/div

Sleep of PWREN, OUT2/4/6

CH1: V_{PWREN}, 3V/div
CH2: V_{OUT2}, 1V/div
CH3: V_{OUT4}, 1V/div
CH4: V_{OUT6}, 1V/div
TIME: 4ms/div

Sleep of PWREN, OUT5/7/8



CH1: V_{PWREN}, 3V/div
CH2: V_{OUT5}, 1V/div
CH3: V_{OUT7}, 2V/div
CH4: V_{OUT8}, 10V/div
TIME: 4ms/div

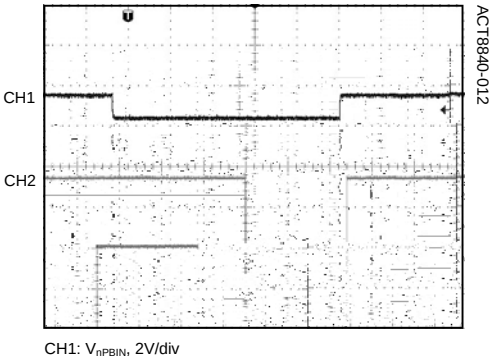
Sleep of PWREN, OUT10/11/12

CH1: V_{PWREN}, 3V/div
CH2: V_{OUT10}, 2V/div
CH3: V_{OUT11}, 2V/div
CH4: V_{OUT12}, 3V/div
TIME: 4ms/div

Shutdown of PWRHLD, OUT1/3/5

CH1: V_{PWRHLD}, 2V/div
CH2: V_{OUT1}, 2V/div
CH3: V_{OUT3}, 2V/div
CH4: V_{OUT5}, 1V/div
TIME: 1ms/div

nPBIN and nPBSTAT

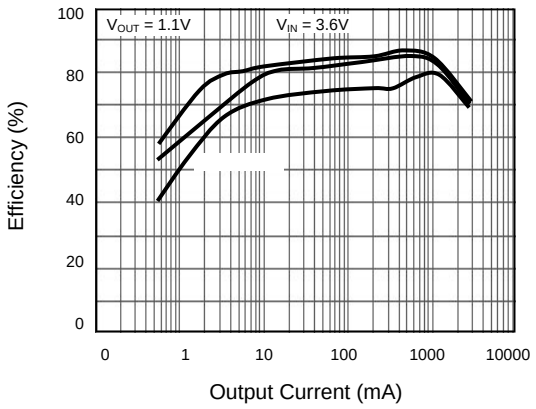


CH1: V_{nPBIN}, 2V/div
CH2: $V_{nPBSTAT}$, 2V/div
TIME: 10ms/div

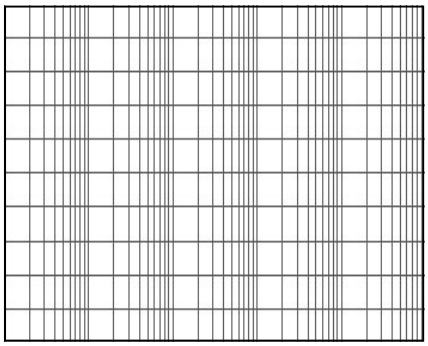
TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(T_A = 25°C, unless otherwise specified.)

REG3 Efficiency vs. Output Current



REG4 Efficiency vs. Output Current



REG10 @ 10mA vs. Temperature

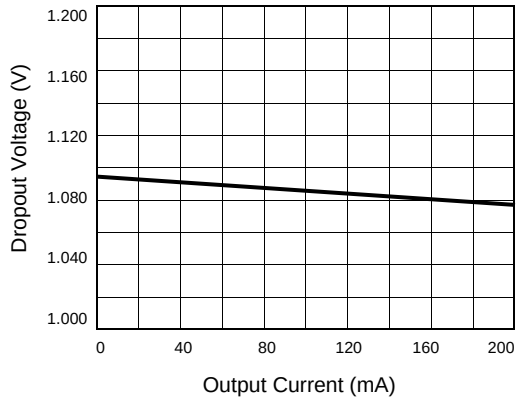
V_{OUT10} @ 150mA vs. Temperature

REG5/6 Dropout Voltage vs. I_{OUT}

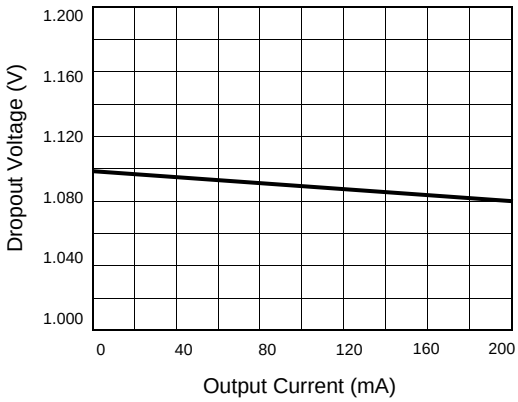
TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(T_A = 25°C, unless otherwise specified.)

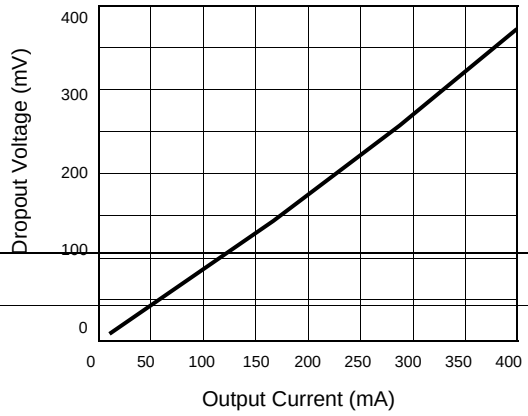
REG5 V_{OUT} vs. I_{OUT}



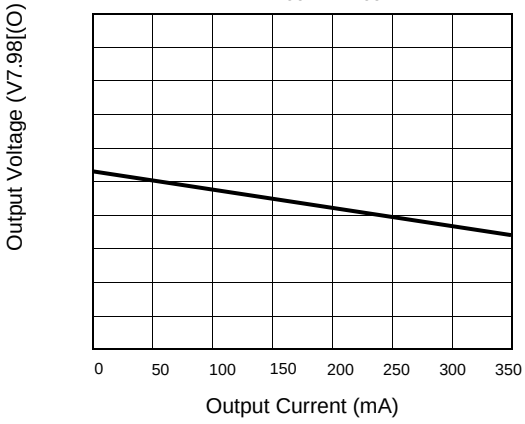
REG6 V_{OUT} vs. I_{OUT}



REG7/8/9 Dropout Voltage vs. I_{OUT}



REG7 V_{OUT} vs. I_{OUT}



REG8 V_{OUT} vs. I_{OUT}

REG9 V_{OUT} vs. I_{OUT}

1.36 9.6(0)9.5( )]TJ0 -3.74 TD[(.36)9.6(0)9.5( )]TJ0 -3.793TD[(.3289.6(0)9.5( )]TJ0 -3.7

A C T

SYSTEM CONTROL INFORMATION

Interfacing with the Telechips TCC88xx Processors

The ACT8840 is optimized for the general Single-core processors, supporting both the power domains as well as the signal interface. The following paragraphs describe how to design ACT8840 with the general Single-core processors.

While the ACT8840 supports many possible configurations for powering these processors, one of the most common configurations is detailed in this datasheet.

Table 1:

ACT8840 Power Domains

ACT8840 REGULATOR	POWER DOMAIN	DEFAULT VOLTAGE	MAX CURRENT	POWER UP ORDER	ON/OFF @ SLEEP	POWER OFF ORDER	TYPE
REG1	VDD_M0 PVDD_MEM VDD_EXT0~2 VDD_LCD VDD_AUD VDD_SYS0~1 VDD_CKO VDD_KEY VDD_MODEM VDD_IO	3.3V	1.3A	3	ON	1	DC/DC Step Down
REG2	VDD_ARM	1.25V	1.8A	2	OFF	2	DC/DC Step Down
REG3	VDD_M1~2 VDD_MEM1~2	1.8V	1.8A	3	ON	1	DC/DC Step Down
REG4	VDD_INT	1.1V	1.3A	2	OFF	2	DC/DC Step Down
REG5	VDD_UOTG_D VDD_UHOST_D	1.1V	150mA	3	OFF	1	Low-Noise LDO
REG6	VDD_ALIVE	1.1V	150mA	1	ON	3	Low-Noise LDO
REG7	VDD_UOTG_A VDD_UHOST_A	3.3V	350mA	3	OFF	1	Low-Noise LDO
REG8	VDD_APLL VDD_MPLL VDD_VPLL VDD_EPLL VDD_HDMI VDD_HDMI_PLL VDD_MIPI_D VDD_MIPI_PLL	1.1V	350mA	2	OFF	2	Low-Noise LDO
REG9	VDD_CAM	2.8V	350mA	3	ON	1	Low-Noise LDO
REG10	VDD_ADC	3.3V	150mA	3	OFF	1	Low Input-Voltage LDO
REG11	VDD_MIPI_A	1.8V	350mA	3	OFF	1	Low Input-Voltage LDO
REG12	VDD_DAC VDD_DAC_A VDD_HDMI_OSC	3.3V	350mA	3	OFF	1	Low Input-Voltage LDO
REG13	VDD_RTC	3.0V	50mA	0	ON	0	Always-ON LDO

Control Signals

Enable Inputs

The ACT8840 features a variety of control inputs, which are used to enable and disable outputs depending upon the desired mode of operation. PWREN, PWRHLD are logic inputs, while nPBIN is a unique, multi-function input.

nPBIN Multi-Function Input

The ACT8840 features the nPBIN multi-function pin, which combines system enable/disable control with a hardware reset function. Select either of the two pin functions by asserting this pin, either through a direct connection to GA, or through a 50kΩ resistor to GA, as shown in Figure 2.

Manual Reset Function

The second major function of the nPBIN input is to provide a manual-reset input for the processor. To manually-reset the processor, drive nPBIN directly to GA through a low impedance (less than 2.5kΩ). An internal timer detects the duration of the MR event:

Short Press / Soft-Reset:

If the MR is asserted for less than 4s, ACT8840 commences a soft-reset operation where nRSTO immediately asserts low, then remains asserted low until the nPBIN input is de-asserted and the reset time-out period expires. A status bit, SRSTAT[ ] , is set after a soft-reset event. The SRSTAT[ ] bit is automatically cleared to 0 after read. After Short Press, set WDSREN[ ] to 1 about 1s after nRSTO de-assert then clear WDSREN[ ] for properly shutdown sequence.

Long Press / Power-cycle:

If the MR is asserted for more than 4s, ACT8840 commences a power cycle routine in which case all regulators are turned off and then turned back on. A status bit, PCSTAT[ ], is set after the power cycle. The PCSTAT[ ] bit is automatically cleared to 0 after read.

nPBSTAT Output

nPBSTAT is an open-drain output that reflects the state of the nPBIN input; nPBSTAT is asserted low whenever nPBIN is asserted, and is high-Z otherwise. This output is typically used as an interrupt signal to the processor, to initiate a software-programmable routine such as operating mode selection or to open a menu. Connect nPBSTAT to an appropriate supply voltage through a 10kΩ or greater resistor.

Figure 2:
nPBIN Input

nRSTO Output

nRSTO is an open-drain output which asserts low upon startup or when manual reset is asserted via the nPBIN input. When asserted on startup, nRSTO remains low until reset time-out period expires. When asserted due to manual-reset, nRSTO immediately asserts low, then remains asserted low until the nPBIN input is de-asserted and the reset time-out period expires.

Connect a 10kΩ o o o-r npull-oe1(s)ist oe

Push-Button Control

The ACT8840 is designed to initiate a system enable sequence when the nPBIN multi-function input is asserted. Once this occurs, a power-on sequence commences, as described below. The power-on sequence must complete and the microprocessor must take control (by asserting PWRHLD) before nPBIN is de-asserted. If the microprocessor is unable to complete its power-up routine successfully before the user releases the push-button, the ACT8840 automatically shuts the system down. This provides protection against accidental or momentary93 771.tal or 99uassertions of the push-button. If desired, longer “push-and-hold” times can be implemented by simply adding an additional time delay before asserting PWREN or PWRHLD.

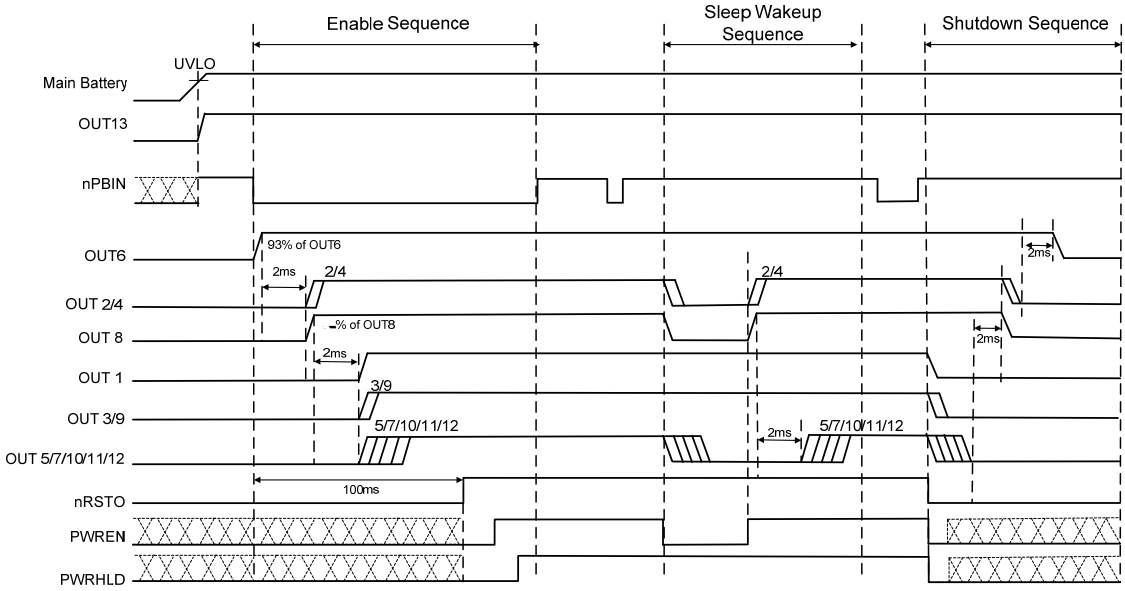
Control Sequences

The ACT8840 features a variety of control sequences that are optimiz3 771.tal06 99ued for supporting system enable and disable.

Enabling/Disabling Sequence

A typical enable sequence is initiated whenever the nPBIN is asserted low via 50KΩ r e s i s power control diagram is s3 771.1.8982 99uhown in Figure 3. During the boot sequence, the microprocessor must assert PWRHLD, and PWREN, to ensure that the system remains powered after nPBIN is released. Once the

Figure 3:
Power Control Sequence



FUNCTIONAL DESCRIPTION

I²C Interface

The ACT8840 features an I²C interface that allows advanced programming capability to enhance overall system performance. To ensure compatibility with a wide range of system processors, the I²C interface supports clock speeds of up to 400kHz ("Fast-Mode" operation) and uses standard I²C commands. I²C write-byte commands are used to program the ACT8840, and I²C read-byte commands are used to read the ACT8840's internal registers. The ACT8840 always operates as a slave device, and is addressed using a 7-bit slave address followed by an eighth bit, which indicates whether the transaction is a read-operation or a write-operation, [1011010x].

SDA is a bi-directional data line and SCL is a clock input. The master device initiates a transaction by issuing a START condition, defined by SDA transitioning from high to low while SCL is high. Data is transferred in 8-bit packets, beginning with the MSB, and is clocked-in on the rising edge of SCL. Each packet of data is followed by an "Acknowledge" (ACK) bit, used to confirm that the data was transmitted successfully.

For more information regarding the I²C 2-wire serial interface, go to the NXP website: http://www.nxp.com.

Housekeeping Functions

Programmable battery Voltage Monitor

The ACT8840 features a programmable battery-voltage monitor, which monitors the voltage at INL2 (which should be connected directly to the battery) and compares it to a programmable threshold voltage. The VBATMON comparator is designed to be immune to noise resulting from switching, load transients, etc. The BATMON comparator is disable by default; to enable it, set the BATLEV[3:0] register to one of the value in Table 2. Note that there is a 200mV hysteresis between the rising and falling threshold for the comparator. The VBATDAT [ ] bit reflects the output of the BATMON comparator. The value of VBATDAT[ ] is 1 when V_{INL2} < BATLEV; value is 0 otherwise.

The VBATMON comparator can generate an interrupt when V_{INL2} is lower than BATLEV[ ] voltage. The interrupt is masked by default by can be unmasked by setting VBATMSK[ ] = 1.

Table 2:

BATLEV Falling Threshold

BATLEV[3:0]	BATLEV Falling Threshold
0000	2.5
0001	2.6
0010	2.7
0011	2.8
0100	2.9
0101	3.0
0110	3.1
0111	3.2
1000	3.3
1001	3.4
1010	

Thermal Protection

The ACT8840 integrates thermal shutdown protection circuitry to prevent damage resulting from excessive thermal stress, as may be encountered under fault conditions.

Thermal Interrupt

If the thermal interrupt is unmasked (by setting nTMSK[ ] to 1), ACT8840 can generate an interrupt when the die temperature reaches 120°C (typ.).

Thermal Protection

If the ACT8840 die temperature exceeds 160°C, the thermal protection circuitry disables all regulators and prevents the regulators from being enabled until the IC temperature drops by 20°C (typ.).

General Description

REG1, REG2, REG3, and REG4 are fixed-frequency, current-mode, synchronous PWM step-down converters that achieves peak efficiencies of up to 97%. These regulators operate with a fixed frequency of 2.25MHz, minimizing noise in sensitive applications and allowing the use of small external components. Additionally, REG1, REG2, REG3, and REG4 are available with a variety of standard and custom output voltages, and may be software-controlled via the I^2C interface for systems that require advanced power management functions.

100% Duty Cycle Operation

REG1, REG2, REG3, and REG4 are capable of operating at up to 100% duty cycle. During 100%

Enable / Disable Control

During normal operation, each buck may be enabled or disabled via the I^{2}C interface by writing to that regulator's ON[ ] bit.

OK[ ] and Output Fault Interrupt

Each DC/DC features a power-OK status bit that can be read by the system microprocessor via the I^{2}C interface. If an output voltage is lower than the power-OK threshold, typically 7% below the programmed regulation voltage, that regulator's OK[ ] bit will be 0.

If a DC/DC's nFLTMSK[

PCB Layo.ratps2( )]TJ/TT6 1 Tf10.02 0 0 10.02 57.548

LOW-NOISE, LOW-DROPOUT LINEAR REGULATORS

General Description

ACT8840 features eight low-noise, low-dropout linear regulators (LDOs) that supply up to 350mA. Three of these LDOs (REG10, REG11, and REG12) supports extended input voltage range down to 1.7V. Each LDO has been optimized to achieve low noise and high-PSRR.

Output Current Limit

Each LDO contains current-limit circuitry featuring a current-limit fold-back function. During normal and moderate overload conditions, the regulators can support more than their rated output currents. During extreme overload conditions, however, the current limit is reduced by approximately 30%, reducing power dissipation within the IC.

Compensation

The LDOs are internally compensated and require very little design effort, simply select input and output capacitors according to the guidelines below.

Input Capacitor Selection

Each LDO requires a small ceramic input capacitor to supply current to support fast transients at the input of the LDO. Bypassing each INL pin to GA with 1µF. High quality ceramic capacitors such as X7R and X5R dielectric types are strongly recommended.

ALWAYS-ON LDO (REG13)

General Description

REG13 is an always-on, low-dropout linear regulator (LDO) that is optimized for RTC and backup-battery applications. REG13 features low-quiescent supply current, current-limit protection, and reverse-current protection, and is ideally suited for always-on power supply applications, such as for a real-time clock, or as a backup-battery or super-cap charger.

Reverse-Current Protection

REG13 features internal circuitry that limits the reverse supply current to less than 1µA when the input voltage falls below the output voltage, as can be encountered in backup-battery charging applications. REG13's internal circuitry monitors the input and the output, and disconnects internal circuitry and parasitic diodes when the input voltage falls below the output voltage, greatly minimizing backup battery discharge.

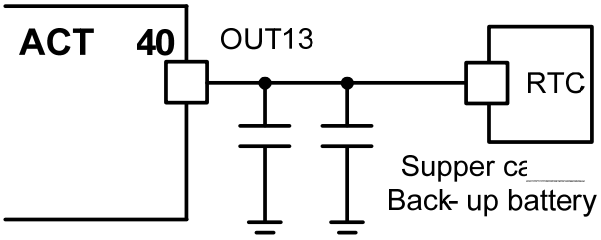
Typical Application

Voltage Regulators

REG13 is ideally suited for always-on voltage-regulation applications, such as for real-time clock and memory keep-alive applications. This regulator requires only a small ceramic capacitor with a minimum capacitance of 0.47µF for stability. For best performance, the output capacitor should be connected directly between the output and GA, with a short and direct connection.

Figure 4:

Typical Application of RTC LDO



Backup Battery Charging

REG13 features a constant current-limit, which protects the IC under output short-circuit conditions as well as provides a constant charge current, when operating as a backup battery charger.

PWM LED DRIVERS

The GPIO1, the GPIO2, the GPIO3, the GPIO4, the GPIO5, and the GPIO6 are configured as PWM LED drivers, which could support up to 6mA current with programmable frequency and duty cycle. Set PWMxEN[ ] bit to "1" to enable PWM function of GPIOx.

PWM Frequence Selection

Each LED driver may be independently programmed to a different frequency by writing to the GPIO's FRE[2:0] register via the I^2C serial interface as shown in Table 4.

Table 4:

GPIOx/FRE[ ] PWM Frequency Setting

PWM Duty Cycle Selection

Each LED driver may be independently programmed to a different duty cycle by writing to the GPIO's DUTY[3:0] register via the I^2C serial interface as shown in Table 5.

Table 5: