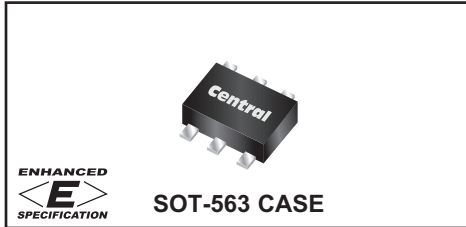


CMLT3904E CMLT3904EG* NPN
 CMLT3906E CMLT3906EG* PNP
 CMLT3946E CMLT3946EG* NPN/PNP

**ENHANCED SPECIFICATION
 SURFACE MOUNT SILICON
 COMPLEMENTARY TRANSISTORS**



* Device is *Halogen Free* by design

ENHANCED SPECIFICATIONS:

- ◆ BV_{CBO} from 40V MIN to 60V MIN (PNP)
- ◆ BV_{EBO} from 5.0V MIN to 6.0V MIN (PNP)

MAXIMUM RATINGS: ($T_A=25^\circ\text{C}$)

- ◆ **Collector-Base Voltage**
Collector-Emitter Voltage
- ◆ **Emitter-Base Voltage**
Continuous Collector Current
Power Dissipation (Note 1)
Power Dissipation (Note 2)
Power Dissipation (Note 3)
Operating and Storage Junction Temperature
Thermal Resistance

ELECTRICAL CHARACTERISTICS: ($T_A=25^\circ\text{C}$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	NPN		PNP		UNITS
		MIN	TYP	TYP	MAX	
I_{CEV}	$V_{CE}=30V, V_{EB}=3.0V$	-	-	-	50	nA
◆ BV_{CBO}	$I_C=10\mu A$	60	115	90	-	V
BV_{CEO}	$I_C=1.0mA$	40	60	55	-	V
◆ BV_{EBO}	$I_E=10\mu A$	6.0	7.5	7.9	-	V
◆ $V_{CE(SAT)}$	$I_C=10mA, I_B=1.0mA$	-	0.057	0.050	0.100	V
◆ $V_{CE(SAT)}$	$I_C=50mA, I_B=5.0mA$	-	0.100	0.100	0.200	V
$V_{BE(SAT)}$	$I_C=10mA, I_B=1.0mA$	0.65	0.75	0.75	0.85	V
$V_{BE(SAT)}$	$I_C=50mA, I_B=5.0mA$	-	0.85	0.85	0.95	V
◆ h_{FE}	$V_{CE}=1.0V, I_C=0.1mA$	90	240	130	-	
◆ h_{FE}	$V_{CE}=1.0V, I_C=1.0mA$	100	235	150	-	
h_{FE}	$V_{CE}=1.0V, I_C=10mA$	100	215	150	300	
◆ h_{FE}	$V_{CE}=1.0V, I_C=50mA$	70	110	120	-	
h_{FE}	$V_{CE}=1.0V, I_C=100mA$	30	50	55	-	

◆ Enhanced Specification

- Notes: (1) Ceramic or aluminum core PC Board with copper mounting pad area of 4.0mm²
 (2) FR-4 Epoxy PC Board with copper mounting pad area of 4.0mm²
 (3) FR-4 Epoxy PC Board with copper mounting pad area of 1.4mm²



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DESCRIPTION:

These CENTRAL SEMICONDUCTOR devices are combinations of dual, enhanced specification transistors in a space saving SOT-563 package, designed for small signal general purpose amplifier and switching applications.

MARKING CODES:

CMLT3904E:	L04
CMLT3906E:	L06
CMLT3946E:	L46
CMLT3904EG*:	C4G
CMLT3906EG*:	C6G
CMLT3946EG*:	46G

- ◆ h_{FE} from 60 MIN to 70 MIN (NPN/PNP)
- ◆ $V_{CE(SAT)}$ from 0.3V MAX to 0.2V MAX (NPN)
from 0.4V MAX to 0.2V MAX (PNP)

SYMBOL		UNITS
V_{CBO}	60	V
V_{CEO}	40	V
V_{EBO}	6.0	V
I_C	200	mA
P_D	350	mW
P_D	300	mW
P_D	150	mW
T_J, T_{stg}	-65 to +150	$^\circ\text{C}$
θ_{JA}	357	$^\circ\text{C/W}$

R6 (29-June 2015)

CMLT3904E CMLT3904EG* NPN
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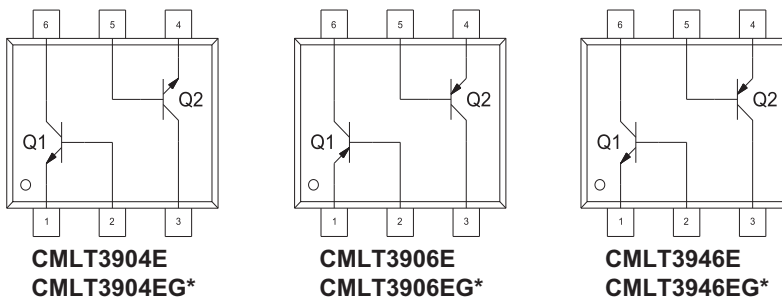
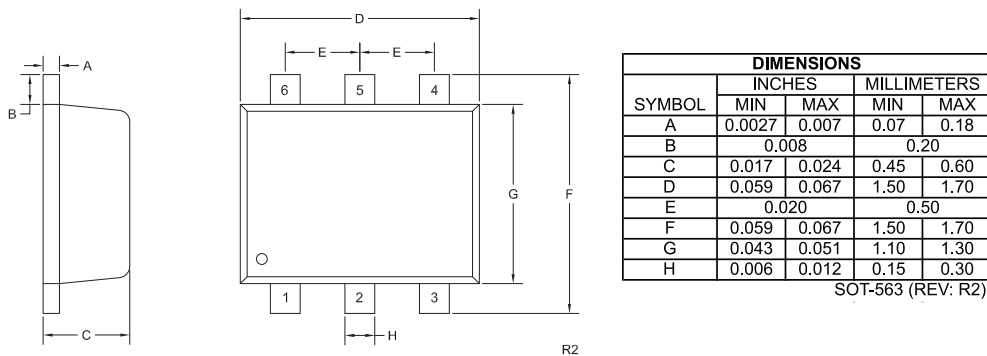


**ENHANCED SPECIFICATION
 SURFACE MOUNT SILICON
 COMPLEMENTARY TRANSISTORS**

ELECTRICAL CHARACTERISTICS PER TRANSISTOR - Continued: ($T_A=25^\circ\text{C}$)

SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
f_T	$V_{CE}=20\text{V}$, $I_C=10\text{mA}$, $f=100\text{MHz}$	300		MHz
C_{ob}	$V_{CB}=5.0\text{V}$, $I_E=0$, $f=1.0\text{MHz}$		4.0	pF
C_{ib}	$V_{BE}=0.5\text{V}$, $I_C=0$, $f=1.0\text{MHz}$		8.0	pF
h_{ie}	$V_{CE}=10\text{V}$, $I_C=1.0\text{mA}$, $f=1.0\text{kHz}$	1.0	12	$k\Omega$
h_{re}	$V_{CE}=10\text{V}$, $I_C=1.0\text{mA}$, $f=1.0\text{kHz}$	0.1	10	$\times 10^{-4}$
h_{fe}	$V_{CE}=10\text{V}$, $I_C=1.0\text{mA}$, $f=1.0\text{kHz}$	100	400	
h_{oe}	$V_{CE}=10\text{V}$, $I_C=1.0\text{mA}$, $f=1.0\text{kHz}$	1.0	60	μS
NF	$V_{CE}=5.0\text{V}$, $I_C=100\mu\text{A}$, $R_S=1.0k\Omega$ $f=10\text{Hz}$ to 15.7kHz		4.0	dB
t_d	$V_{CC}=3.0\text{V}$, $V_{BE}=0.5\text{V}$, $I_C=10\text{mA}$, $I_{B1}=1.0\text{mA}$		35	ns
t_r	$V_{CC}=3.0\text{V}$, $V_{BE}=0.5\text{V}$, $I_C=10\text{mA}$, $I_{B1}=1.0\text{mA}$		35	ns
t_s	$V_{CC}=3.0\text{V}$, $I_C=10\text{mA}$, $I_{B1}=I_{B2}=1.0\text{mA}$		200	ns
t_f	$V_{CC}=3.0\text{V}$, $I_C=10\text{mA}$, $I_{B1}=I_{B2}=1.0\text{mA}$		50	ns

SOT-563 CASE - MECHANICAL OUTLINE



LEAD CODE:

- 1) Emitter Q1
- 2) Base Q1
- 3) Collector Q2
- 4) Emitter Q2
- 5) Base Q2
- 6) Collector Q1

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**ENHANCED SPECIFICATION
SURFACE MOUNT SILICON
COMPLEMENTARY TRANSISTORS**



SERVICES

- Bonded Inventory
- Custom Electrical Screening
- Custom Electrical Characteristic Curves
- SPICE Models
- Custom Packaging
- Package Base Options
- Custom Device Development/ Multi Discrete Modules (MDM™)
- Bare Die Available for Hybrid Applications

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R6 (29-June 2015)