LCD Segment Drivers

Multi-function LCD Segment Drivers

BU97600xxx Series MAX 148 Segment(37SEG x 4COM)

General Description

The BU97600FV-M and BU97600FUV-M are 1/4, 1/3, 1/2 or 1/1 duty general-purpose LCD driver. The BU97600FV-M and BU97600FUV-M can also control up to 16 general-purpose output ports. These products also incorporate a key scan circuit that accepts input from up to 20 keys to reduce printed circuit board wiring.

Features

- AEC-Q100 Qualified (Note1)
- Key input function for up to 20 keys (A key scan is performed only when a key is pressed.)
- Either 1/4, 1/3, 1/2 or 1/1 duty (static) can be selected with the serial control data.
- Serial data control of frame frequency for common and segment output waveforms.
- Serial data control of switching between the segment output ports, PWM output port and general-purpose output port functions. (Max 6ch internal PWM, max 16ch external PWM and max16ch GPO.)
- Built-in OSC circuit
- Support External PWM input
- Integrated Power-on Reset circuit
- No external component
- Low power consumption design
- Supports Line and Frame Inversion

(Note1) Grade 2

Key Specifications

- Supply Voltage Range: +2.7V to +6.0V
- Operating Temperature Range: -40°C to +105°C
- Max Segments:
  - BU97600FV-M 116 Segments
  - BU97600FUV-M 148 Segments
- Display Duty: 1/1,1/2,1/3,1/4 selectable
- Bias: 1/2, 1/3 selectable
- Interface: 3wire serial interface

Packages

W(Typ.)×D(Typ.)×H(Max.)

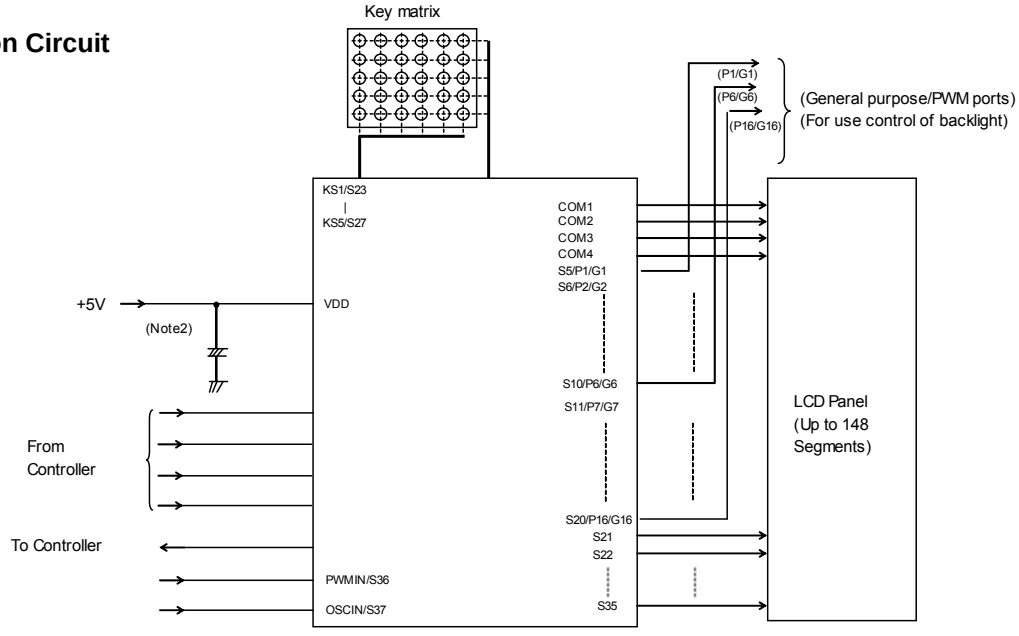
SSOP-B40
13.60mm x 7.80mm x 1.80mm

TSSOP-C48V
12.50mm x 8.10mm x 1.00mm

Applications

- Car HVAC control panel, Car audio, Home electrical appliance, Meter equipment etc.

Typical Application Circuit



(Note2) Insert capacitors between VDD and VSS C > 0.1uF.

Figure 1. Typical Application Circuit

Block Diagram

BU97600FV-M

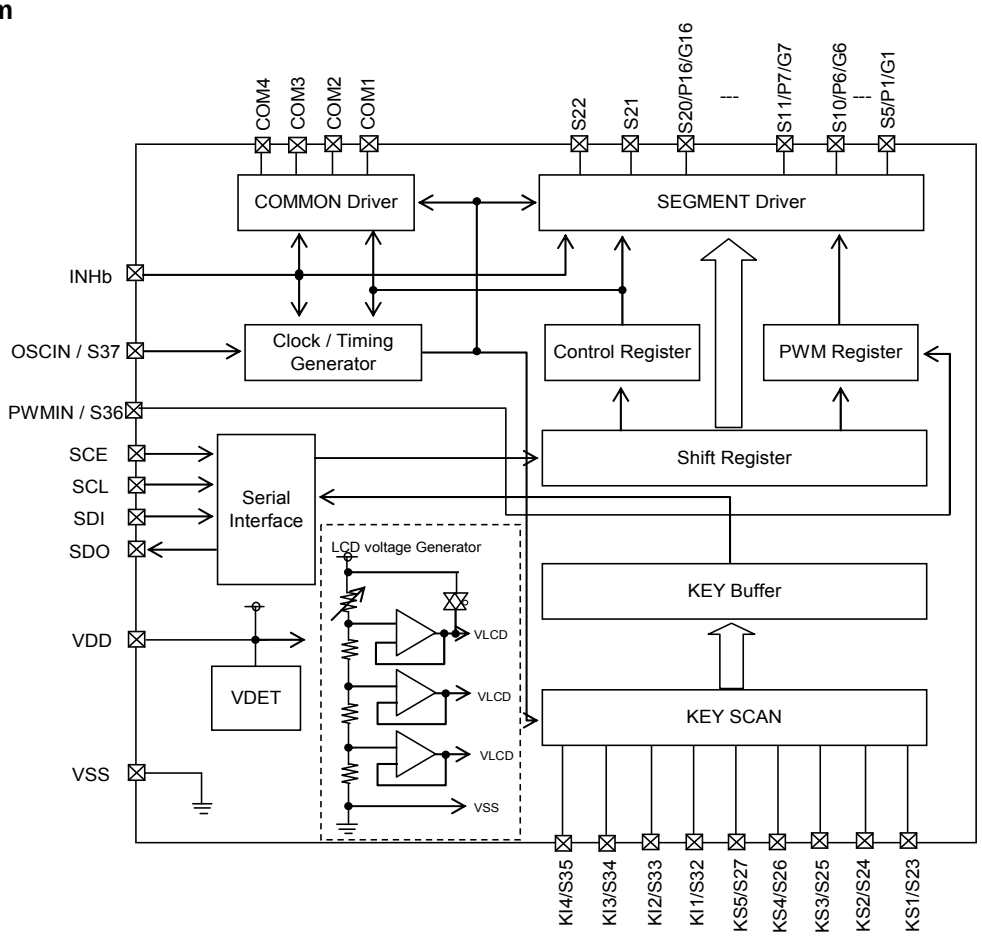


Figure 2. Block Diagram

Pin Arrangement

BU97600FV-M

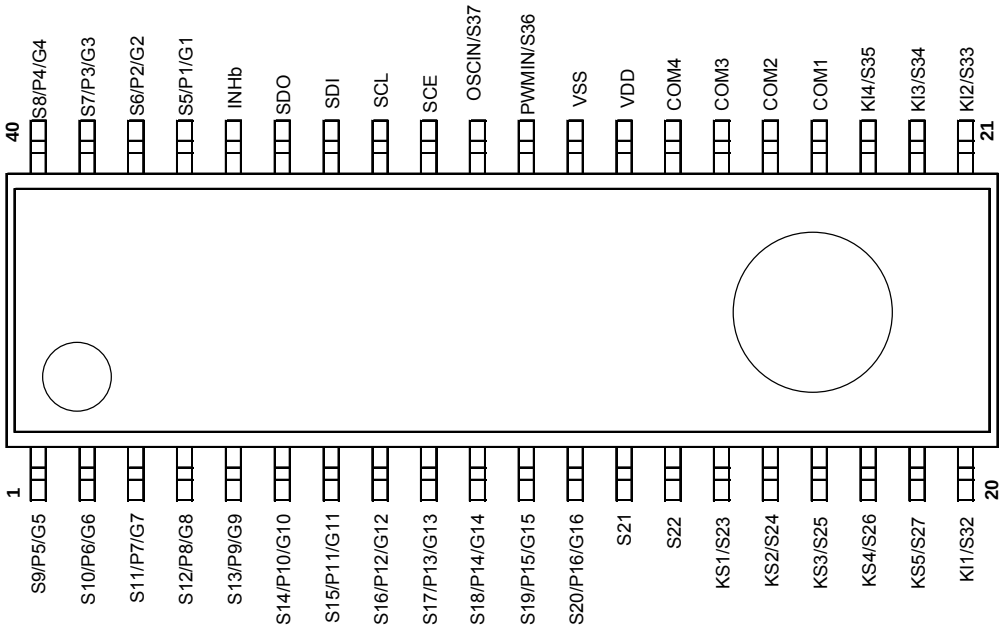


Figure 3. Pin Configuration (TOP VIEW)

Block Diagram

BU97600FUV-M

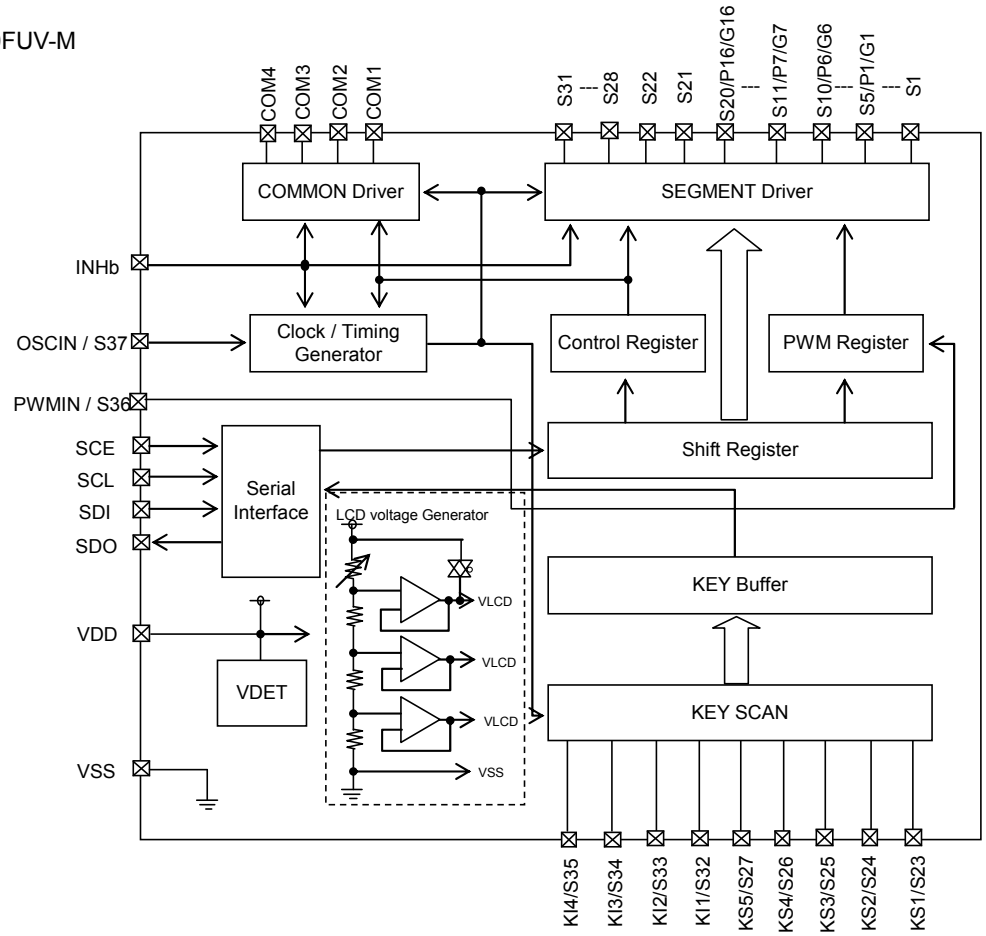


Figure 4. Block Diagram

Pin Arrangement

BU97600FUV-M

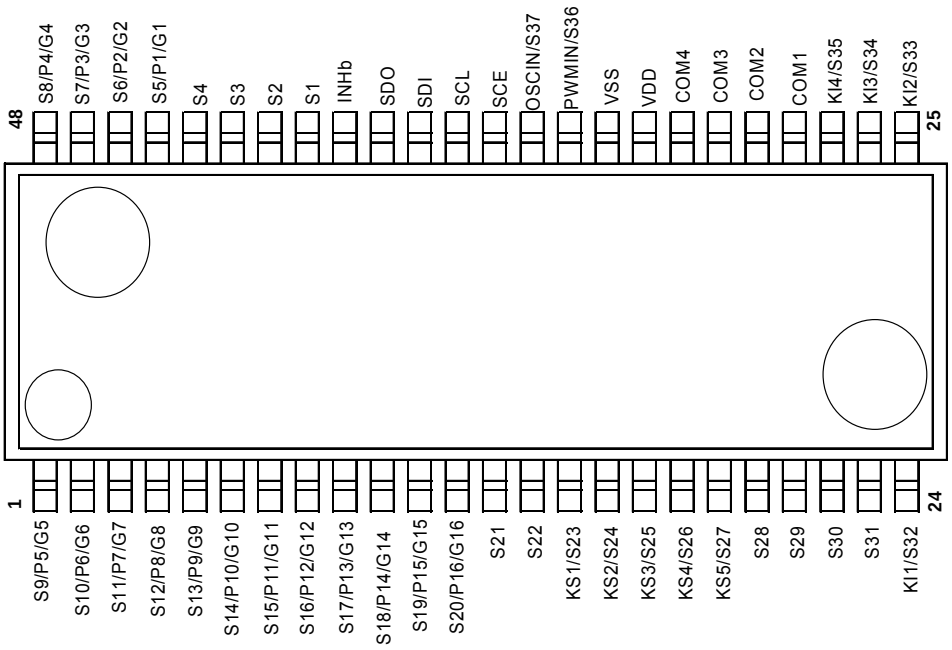


Figure 5. Pin Configuration (TOP VIEW)

Absolute Maximum Ratings(Ta = 25°C, VSS = 0.0V)

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	VDD max	VDD	-0.3 to +6.5	V
Input voltage	VIN1	SCE, SCL, SDI, INHb	-0.3 to +6.5	V
	VIN2	KI1 to KI4	-0.3 to +6.5	V
Allowable loss	Pd	BU97600FV-M	0.70 (Note3)	W
		BU97600FUV-M	0.64(Note3)	W
Operating temperature	Topr		-40 to +105	°C
Storage temperature	Tstg		-55 to +125	°C

(Note3) Derate by 7.00mW/°C when operating above Ta=25°C (when mounted in ROHM's standard board(BU97600FV-M)).
Derate by 6.40mW/°C when operating above Ta=25°C (when mounted in ROHM's standard board(BU97600FUV-M))

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta = -40 to +105°C, VSS = 0.0V)

Parameter	Symbol	Conditions	Ratings			Unit
			Min	Typ	Max	
Supply Voltage	VDD		2.7	5.0	6.0	V

Electrical Characteristics (Ta = -40 to +105°C, VDD = 2.7V to 6.0V, VSS = 0.0V)

Parameter	Symbol	Pin	Conditions	Limit			Unit
				Min	Typ	Max	
Hysteresis	VH1	SCE,SCL,SDI,INHb		-	0.03VDD	-	V
	VH2	KI1 to KI4		-	0.1VDD	-	V
Power-on Detection Voltage	VDET	VDD		1.3	1.8	2.2	V
"H" Level Input Voltage	VIH1	SCE,SCL,SDI,INHb	4.5V ≤ VDD ≤ 6.0V	0.4VDD	-	VDD	V
	VIH2	SCE,SCL,SDI,INHb	2.7V ≤ VDD < 4.5V	0.8VDD	-	VDD	V
	VIH3	KI1 to KI4		0.7VDD	-	VDD	V
"L" Level Input Voltage	VIL1	SCE,SCL,SDI,INHb, KI1 to KI4		0	-	0.2VDD	V
Input Floating Voltage	VIF	KI1 to KI4		-	-	0.05VDD	V
Pull-down Resistance	RPD	KI1 to KI4	VDD=5.0V	50	100	250	KΩ
Output Off Leakage Current	IOFFH	SDO	VO=6.0V	-	-	6.0	μA
"H" Level Input Current	IIH1	SCE,SCL,SDI,INHb	VI = 5.5V	-	-	5.0	μA
"L" Level Input Current	IIL1	SCE,SCL,SDI,INHb	VI = 0V	-5.0	-	-	μA
"H" Level Output Voltage	VOH1	S1 to S37	IO = -20μA, VLCD=1.00*VDD	VDD-0.9	-	-	V
	VOH2	COM1 to COM4	IO = -100μA, VLCD=1.00*VDD	VDD-0.9	-	-	
	VOH3	P1/G1 to P16/G16	IO = -1mA	VDD-0.9	-	-	
	VOH4	KS1 to KS5	IO = -500uA	VDD-1.0	VDD-0.5	VDD-0.2	
"L" Level Output Voltage	VOL1	S1 to S37	IO = 20μA	-	-	0.9	V
	VOL2	COM1 to COM4	IO = 100μA	-	-	0.9	
	VOL3	P1/G1 to P16/G16	IO = 1mA	-	-	0.9	
	VOL4	KS1 to KS5	IO = 25uA	0.2	0.5	1.5	
	VOL5	SDO	IO = 1mA	-	0.1	0.5	
Middle Level Output Voltage	VMID1	S1 to S37	1/2 bias IO = ±20μA VLCD=1.00*VDD	1/2VDD -0.9	-	1/2VDD +0.9	V
	VMID2	COM1 to COM4	1/2 bias IO = ±100μA VLCD=1.00*VDD	1/2VDD -0.9	-	1/2VDD +0.9	
	VMID3	S1 to S37	1/3 bias IO = ±20μA VLCD=1.00*VDD	2/3VDD -0.9	-	2/3VDD +0.9	
	VMID4	S1 to S37	1/3 bias IO = ±20μA VLCD=1.00*VDD	1/3VDD -0.9	-	1/3VDD +0.9	
	VMID5	COM1 to COM4	1/3 bias IO = ±100μA VLCD=1.00*VDD	2/3VDD -0.9	-	2/3VDD +0.9	
	VMID6	COM1 to COM4	1/3 bias IO = ±100μA VLCD=1.00*VDD	1/3VDD -0.9	-	1/3VDD +0.9	

Electrical Characteristics – continued

Parameter	Symbol	Pin	Conditions	Limit			Unit
				Min	Typ	Max	
Current Consumption	IDD1	VDD	Power-saving mode	-	-	15	μA
	IDD2	VDD	VDD = 5.0V Output open, 1/2 bias Frame frequency=80Hz VLCD=1.00*VDD	-	100	210	μA
	IDD3	VDD	VDD = 5.0V Output open,1/3 bias Frame frequency=80Hz VLCD=1.00*VDD	-	120	250	μA

Oscillation Characteristics (Ta = -40 to +105°C, VDD = 2.7V to 6.0V, VSS = 0.0V)

Parameter	Symbol	Pin	Conditions	Limit			Unit
				Min	Typ	Max	
Oscillator Frequency 1	fosc1	-	VDD = 2.7V to 6.0V	360	-	720	kHz
Oscillator Frequency 2	fosc2	-	VDD = 5V	540	600	660	kHz
External Clock Frequency(Note4)	fosc3	OSCIN	External clock mode (OC=1)	30	-	1000	kHz
External Clock Duty	tdty	OSCIN	External clock mode (OC=1)	30	50	70	%

(Note4) Frame frequency is decided external frequency and dividing ratio of FC0,FC1,FC2, FC3, FC4, FC5, FC6 setting.

【Reference Data】

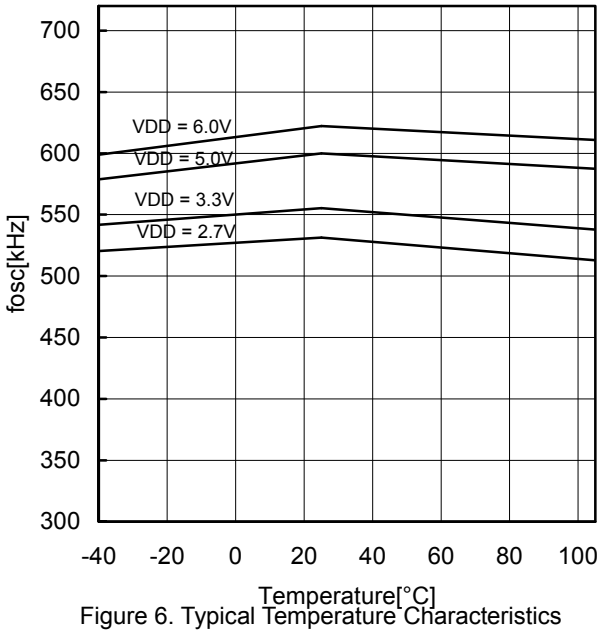
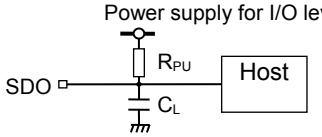


Figure 6. Typical Temperature Characteristics

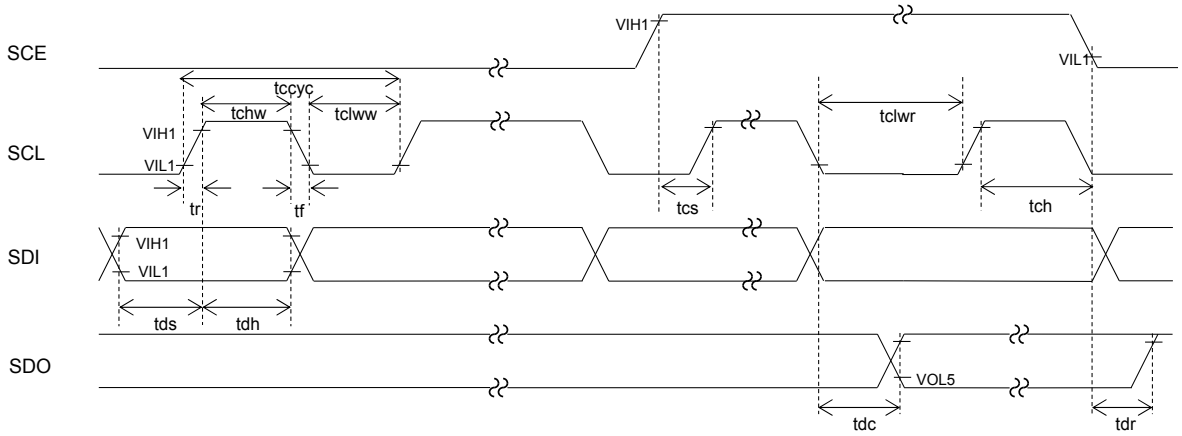
MPU Interface Characteristics (Ta = -40 to +105°C, VDD = 2.7V to 6.0V, VSS = 0.0V)

Parameter	Symbol	Pin	Conditions	Limit			Unit
				Min	Typ	Max	
Data Setup Time	tds	SCL, SDI		120	-	-	ns
Data Hold Time	tdh	SCL, SDI		120	-	-	ns
SCE Wait Time	tcp	SCE, SCL		120	-	-	ns
SCE Setup Time	tcs	SCE, SCL		120	-	-	ns
SCE Hold Time	tch	SCE, SCL		120	-	-	ns
Clock Cycle Time	tccyc	SCL		320	-	-	ns
High-level Clock Pulse Width	tchw	SCL		120	-	-	ns
Low-level Clock Pulse Width (Write)	tclww	SCL		120	-	-	ns
Low-level Clock Pulse Width (Read)	tclwr	SCL	RPU=4.7KΩ CL=10pf(Note5)	1.6	-	-	us
Rise Time	tr	SCE, SCL, SDI		-	160	-	ns
Fall Time	tf	SCE, SCL, SDI		-	160	-	ns
INH Switching Time	tc	INHb, SCE		10	-	-	µs
SDO Output Delay Time	tdc	SDO	RPU=4.7KΩ CL=10pf(Note5)	-	-	1.5	µs
SDO Rise Time	Tdr	SDO	RPU=4.7KΩ CL=10pf(Note5)	-	-	1.5	µs

(Note5) Since SDO is an open-drain output, "tdc" and "tdr" depend on the resistance of the pull-up resistor RPU and the load capacitance SCL.
RPU: 1kΩ≤RPU≤10kΩ is recommended.
CL: A parasitic capacitance to VSS in an application circuit. Any component is not necessary to be attached.



1. When SCL is stopped at the low level



2. When SCL is stopped at the high level

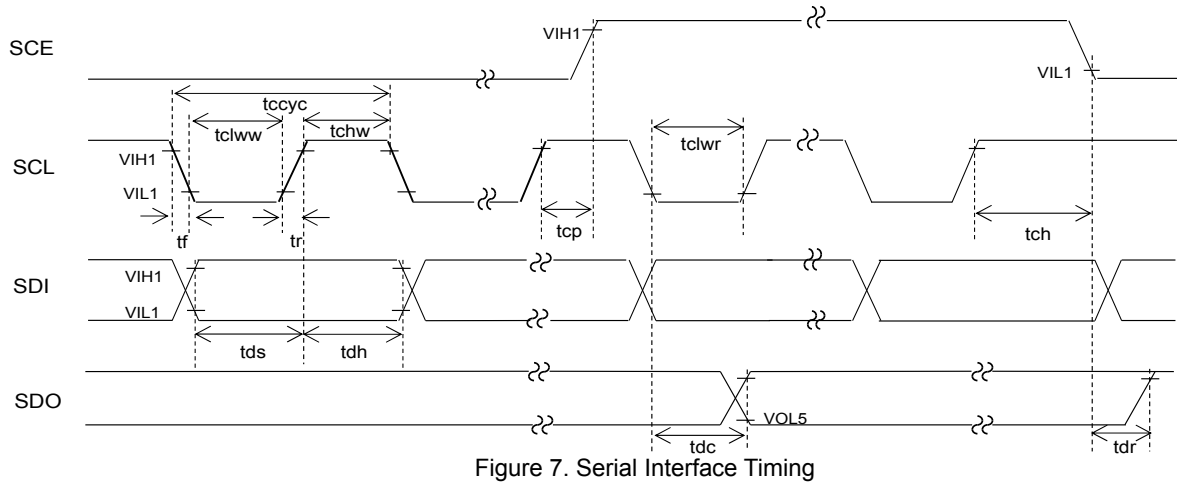


Figure 7. Serial Interface Timing

Pin Description

BU97600FV-M

Symbol	Pin No.	Function	Active	I/O	Handling when unused
S5/P1/G1 to S10/P6/G6	1 to 2 37 to 40	Segment output for displaying the display data transferred by serial data input. The S5/P1/G1 to S10/P6/G6 pins can also be used as General –purpose / PWM outputs when so set up by the control data.	-	O	OPEN
S11/P7/G7 to S20/P16/G16	3 to 12	Segment output for displaying the display data transferred by serial data input. The S11/P7/G7 to S20/P16/G16 pins can also be used as General –purpose outputs / PWM outputs (by EXTPWM) when so set up by the control data.	-	O	OPEN
S21 to S22	13 to14	Segment output for displaying the display data transferred by serial data input.	-	O	OPEN
KS1/S23 to KS5/S27	15 to 19	Key scan outputs Although normal key scan timing lines require diodes to be inserted in the timing lines to prevent shorts, since these outputs are unbalanced CMOS transistor outputs, these outputs will not be damaged by shorting when these outputs are used to form a key matrix. The KS1/S23 to KS5/S27 pins can be used as segment outputs when so specified by the control data.	-	O	OPEN
KI1/S32 to KI4/S35	20 to 23	Key scan inputs These pins have built-in pull-down resistors. The KI1/S32 to KI4/S35 pins can be used as segment outputs when so specified by the control data.	-	I/O	OPEN
COM1 to COM4	24 to 27	Common driver output pins. The frame frequency is fo[Hz].	-	O	OPEN
PWMIN/S36	30	Segment output for displaying the display data transferred by serial data input. The pin PWMIN/S36 can be used external PWM input pin or segment output when set up by the control data.	-	I/O	OPEN
OSCIN/S37	31	Segment output for displaying the display data transferred by serial data input. The pin OSCIN/S37 can be used as external frequency input pin or segment output when set up by the control data.	-	I/O	OPEN
SCE SCL SDI	32 33 34	Serial data transfer inputs. Must be connected to the controller. SCE: Chip enable SCL: Synchronization clock SDI: Transfer data	H ↑ -	I I I	GND
SDO	35	Output data	-	O	OPEN
INHb	36	Display off control input. When INHb = low (VSS), Display forced off S5/P1/G1 to S10/P6/G6 = low (VSS) S11/P7/G7 to S20/P16/G16 = low (VSS) S21 to S22 = low (VSS) KS1/S23 to KS5/S27 = low (VSS) KI1/S32 to KI4/S35 = low (VSS) PWMIN/S36 = low (VSS) OSCIN/S37 = low (VSS) COM1 to COM4 = low (VSS) Stop the LCD drive bias voltage generation divider resistors. Stop the internal oscillation circuit. When INHb = high (VDD), Display on However, serial data transfer is possible when the display is forced off.	L	I	VDD
VDD	28	Power supply pin of the IC A power voltage of 2.7V to 6.0V must be applied to this pin.	-	-	-
VSS	29	Power supply pin. Must be connected to ground.	-	-	-

Pin Description

BU97600FUV-M

Symbol	Pin No.	Function	Active	I/O	Handling when unused
S5/P1/G1 to S10/P6/G6	1 to 2 45 to 48	Segment output for displaying the display data transferred by serial data input. The S5/P1/G1 to S10/P6/G6 pins can also be used as General –purpose / PWM outputs when so set up by the control data.	-	O	OPEN
S11/P7/G7 to S20/P16/G16	3 to 12	Segment output for displaying the display data transferred by serial data input. The S11/P7/G7 to S20/P16/G16 pins can also be used as General –purpose outputs / PWM outputs (by EXTPWM) when so set up by the control data.	-	O	OPEN
S1 to S4 S21 to S22 S28 to S31	41 to 44 13 to 14 20 to 23	Segment output for displaying the display data transferred by serial data input.	-	O	OPEN
KS1/S23 to KS5/S27	15 to 19	Key scan outputs Although normal key scan timing lines require diodes to be inserted in the timing lines to prevent shorts, since these outputs are unbalanced CMOS transistor outputs, these outputs will not be damaged by shorting when these outputs are used to form a key matrix. The KS1/S23 to KS5/S27 pins can be used as segment outputs when so specified by the control data.	-	O	OPEN
KI1/S32 to KI4/S35	24 to 27	Key scan inputs These pins have built-in pull-down resistors. The KI1/S32 to KI4/S35 pins can be used as segment outputs when so specified by the control data.	-	I/O	OPEN
COM1 to COM4	28 to 31	Common driver output pins. The frame frequency is fo[Hz].	-	O	OPEN
PWMIN/S36	34	The pin PWMIN/S36 can be used external PWM input pin or segment output when set up by the control data.	-	I/O	OPEN
OSCIN/S37	35	The pin OSCIN/S37 can be used as external frequency input pin or segment output when set up by the control data.	-	I/O	OPEN
SCE SCL SDI	36 37 38	Serial data transfer inputs. Must be connected to the controller. SCE: Chip enable SCL: Synchronization clock SDI: Transfer data	 H ↑ -	 I I I	GND
SDO	39	Output data	-	O	OPEN
INHb	40	Display off control input. When INHb = low (VSS), Display forced off S1 to S4 = low (VSS) S5/P1/G1 to S10/P6/G6 = low (VSS) S11/P7/G7 to S20/P16/G16 = low (VSS) S21 to S22 = low (VSS) KS1/S23 to KS5/S27 = low (VSS) S28 to S31 = low (VSS) KI1/S32 to KI4/S35 = low (VSS) PWMIN/S36 = low (VSS) OSCIN/S37 = low (VSS) COM1 to COM4 = low (VSS) Stop the LCD drive bias voltage generation divider resistors. Stop the internal oscillation circuit. When INHb = high (VDD), Display on However, serial data transfer is possible when the display is forced off.	L	I	VDD
VDD	32	Power supply pin of the IC A power voltage of 2.7V to 6.0V must be applied to this pin.	-	-	-
VSS	33	Power supply pin. Must be connected to ground.	-	-	-

IO Equivalent Circuit

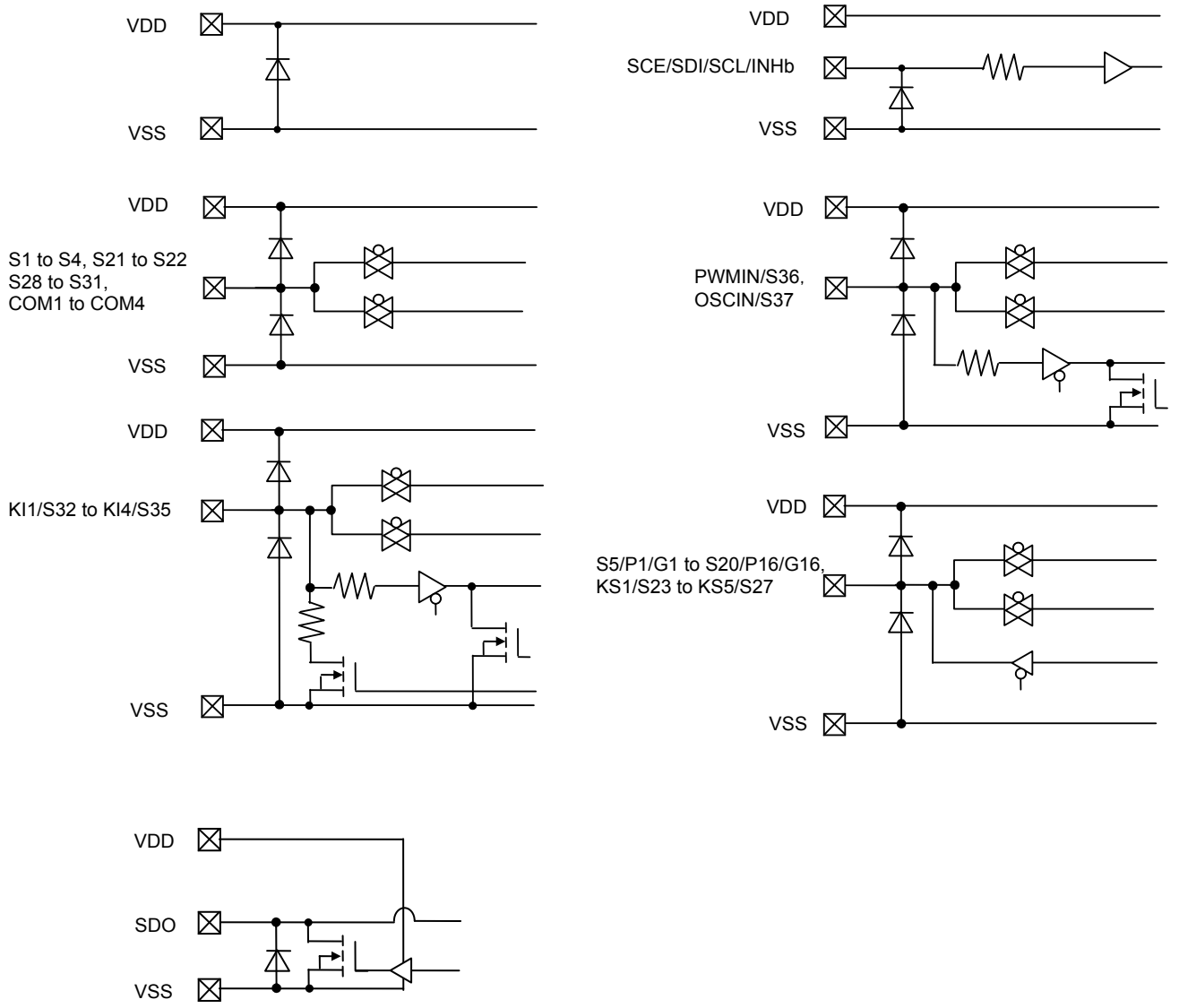


Figure8. I/O Equivalent Circuit

Serial Data Transfer Formats

1. 1/4-Duty

(1)When SCL is stopped at the low level

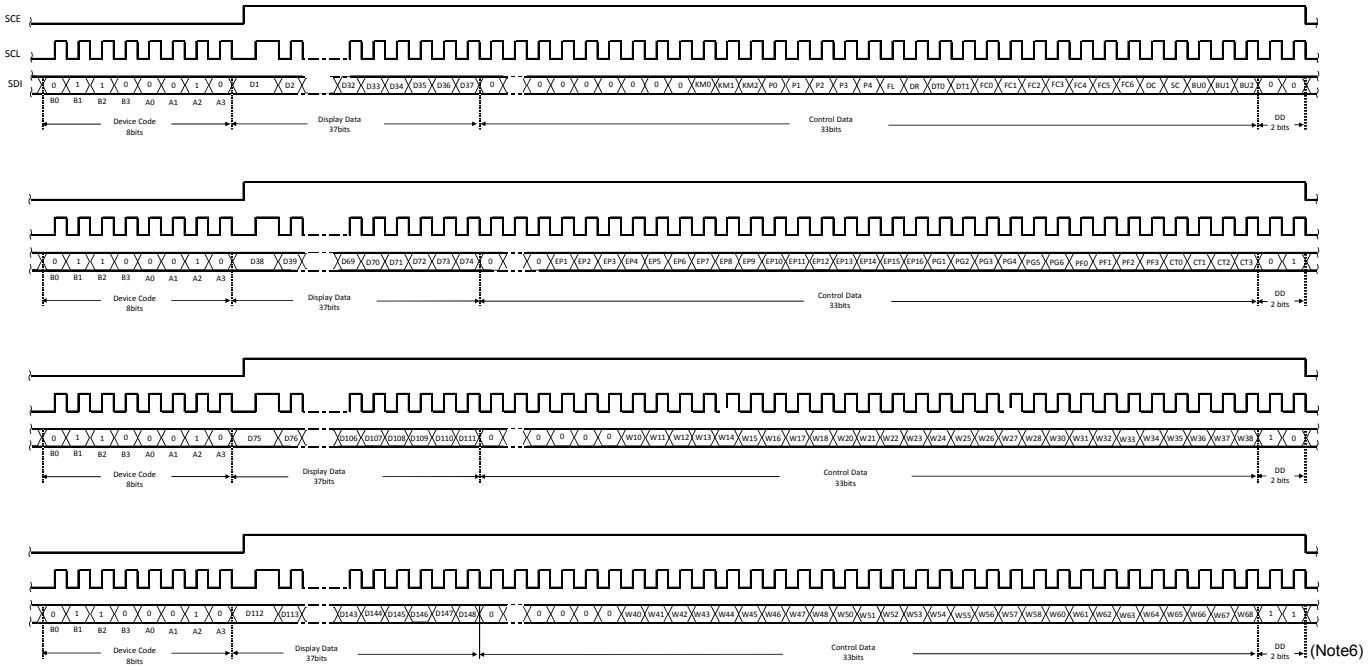


Figure 9. 3-SPI Data Transfer Format

(Note6) DD is direction data.

(2)When SCL is stopped at the high level

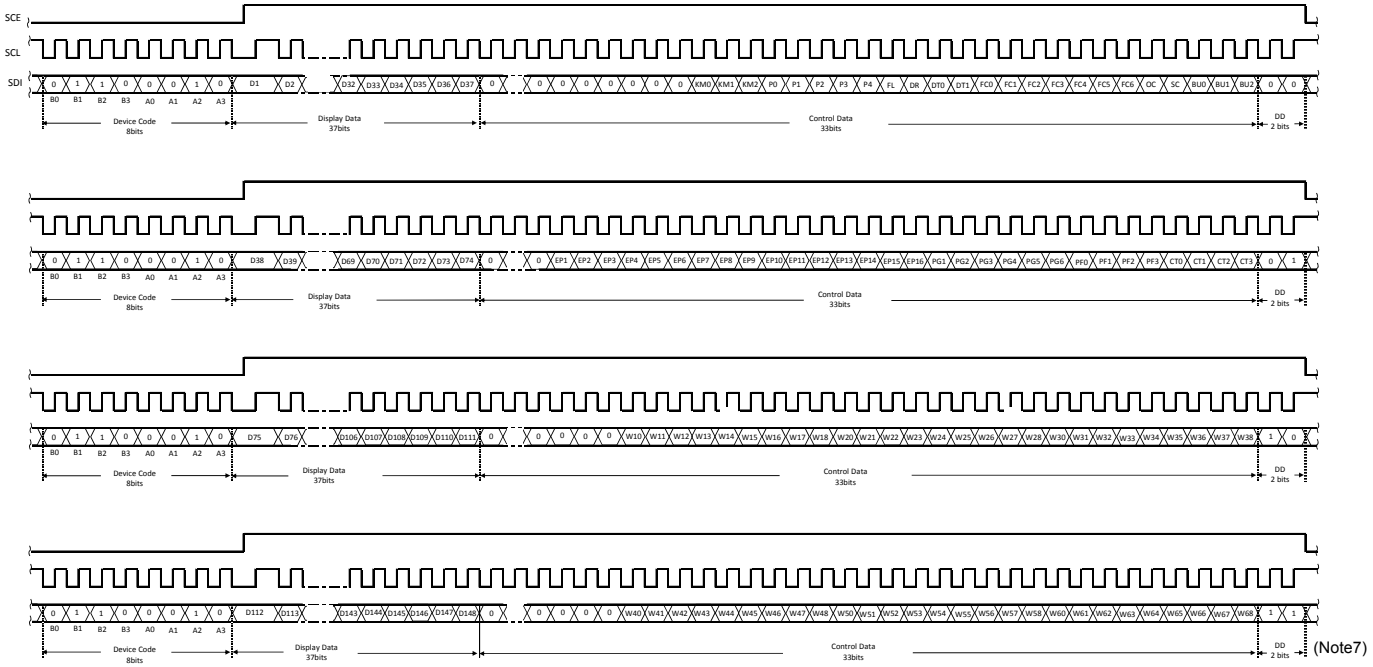


Figure 10. 3-SPI Data Transfer Format

(Note7) DD is direction data.

- Device code·····”46H”
- KM0～KM2·····Key Scan output port/Segment output port switching control data
- D1～D148·····Display data
- P0～P4·····Segment / PWM / General Purpose output port switching control data
- FL·····Line Inversion or Frame Inversion switching control data
- DR·····1/3 bias drive or 1/2 bias drive switching control data
- DT0~DT1·····1/4 duty drive, 1/3 duty drive, 1/2 duty drive or 1/1 duty(static) drive switching control data
- FC0～FC6·····Common/Segment output waveform frame frequency switching control data
- OC····· Internal oscillator operating mode/External clock operating mode switching control data
- SC·····Segment on/off switching control data
- BU0～BU2·····Normal mode/power-saving mode switching control data
- PG1 to PG6·····PWM/General Purpose Output(GPO) switching control data
- EP1 to EP16·····Internal PWM/External PWM switching control data (EP1-EP6),
  GPO/External PWM switching control data (EP7-EP16)
- PF0～PF3·····PWM output waveform frame frequency switching control data.
- CT0～CT3·····LCD display contrast switching control data.
- W10～W18, W20～W28, W30～W38, W40～W48, W50～W58, W60～W68
  ·····PWM output duty switching control data

2. 1/3-Duty

(1) When SCL is stopped at the low level

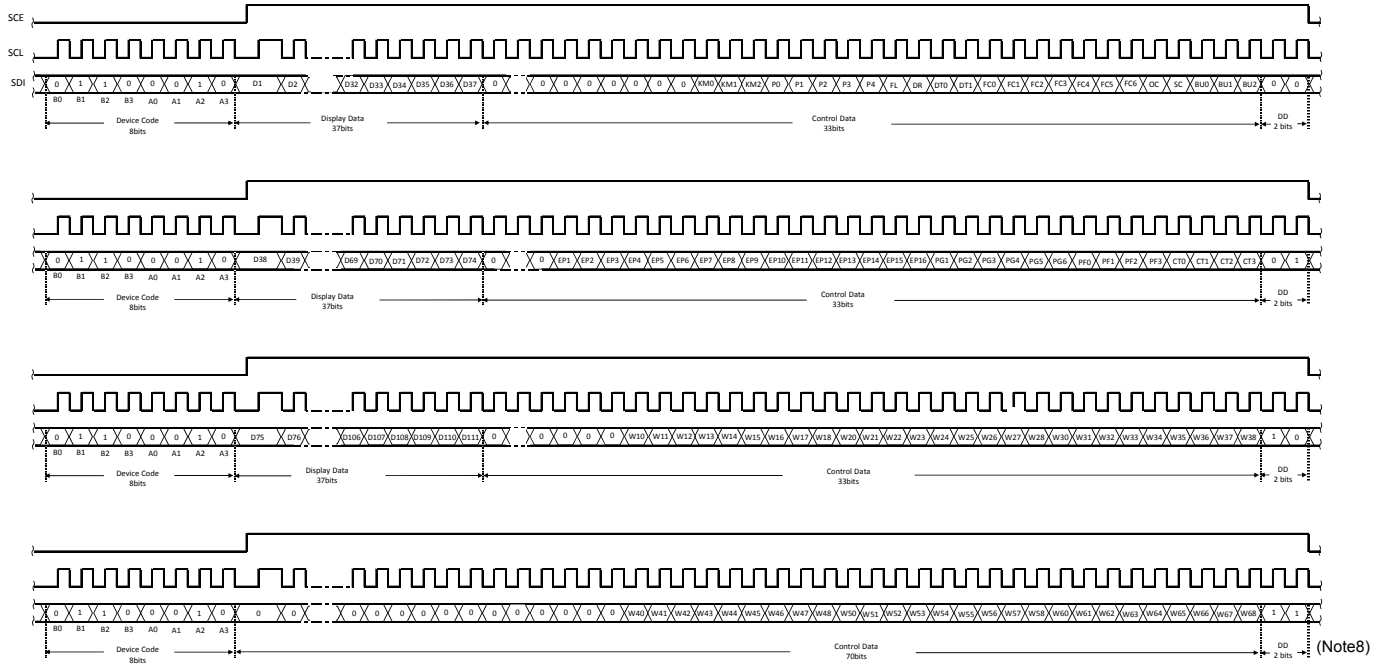


Figure 11. 3-SPI Data Transfer Format

(Note8) DD is direction data.

(2)When SCL is stopped at the high level

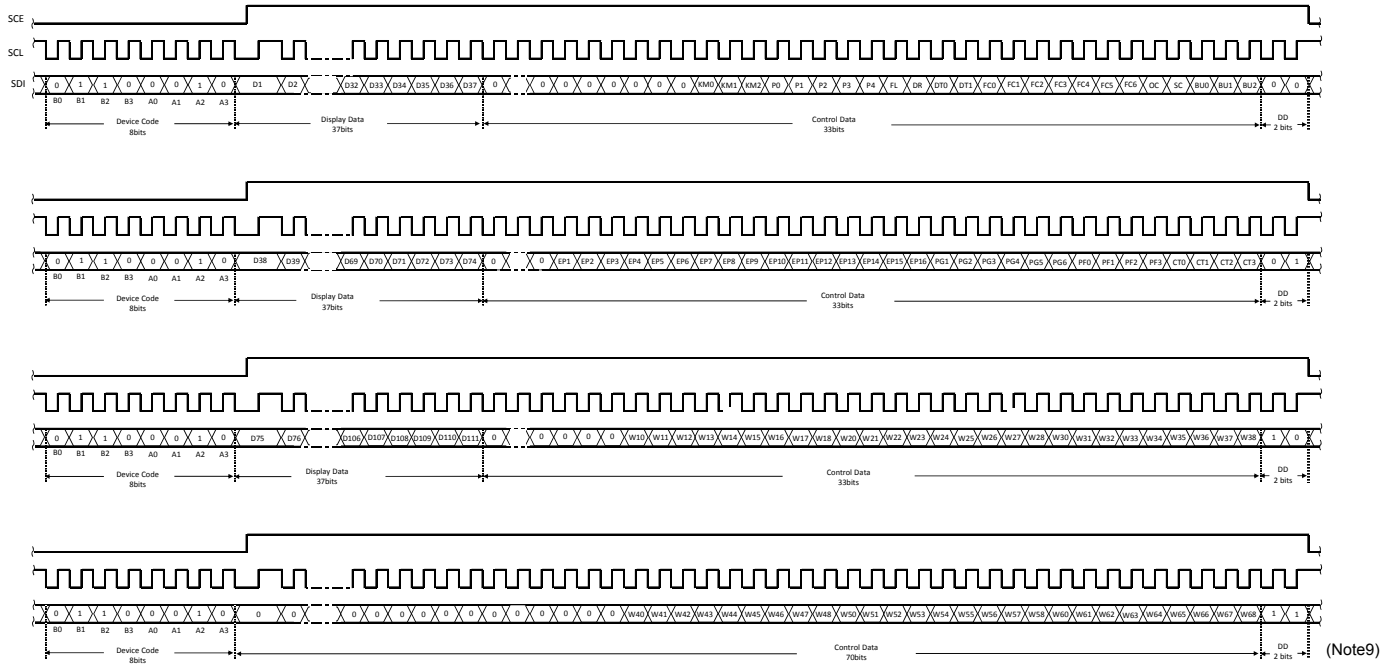


Figure 12. 3-SPI Data Transfer Format

(Note9) DD is direction data.

・Device code・・・・・・・・・・・・・・・・・”46H”
・KM0～KM2・・・・・・・・・・・・・・・・・・Key Scan output port/Segment output port switching control data
・D1～D111・・・・・・・・・・・・・・・・・・Display data
・P0～P4・・・・・・・・・・・・・・・・・・・・Segment / PWM / General Purpose output port switching control data
・FL・・・・・・・・・・・・・・・・・・・・・・・Line Inversion or Frame Inversion switching control data
・DR・・・・・・・・・・・・・・・・・・・・・・・1/3 bias drive or 1/2 bias drive switching control data
・DT0~DT1・・・・・・・・・・・・・・・・・・・1/4 duty drive, 1/3 duty drive, 1/2 duty drive or 1/1 duty(static) drive switching control data
・FC0～FC6・・・・・・・・・・・・・・・・・・Common/Segment output waveform frame frequency switching control data
・OC・・・・・・・・・・・・・・・・・・・・・・・ Internal oscillator operating mode/External clock operating mode switching control data
・SC・・・・・・・・・・・・・・・・・・・・・・・Segment on/off switching control data
・BU0～BU2・・・・・・・・・・・・・・・・・・Normal mode/power-saving mode switching control data
・PG1 to PG6・・・・・・・・・・・・・・・・・PWM/General Purpose Output(GPO) switching control data
・EP1 to EP16・・・・・・・・・・・・・・・・・Internal PWM/External PWM switching control data (EP1-EP6),
GPO/External PWM switching control data (EP7-EP16)
・PF0～PF3・・・・・・・・・・・・・・・・・・PWM output waveform frame frequency switching control data.
・CT0～CT3・・・・・・・・・・・・・・・・・・LCD display contrast switching control data.
・W10～W18, W20～W28, W30～W38, W40～W48, W50～W58, W60～W68
・・・・・・・・・・・・・・・・・・・・・・・・・・・・・・・・PWM output duty switching control data

3. 1/2-Duty

(1) When SCL is stopped at the low level

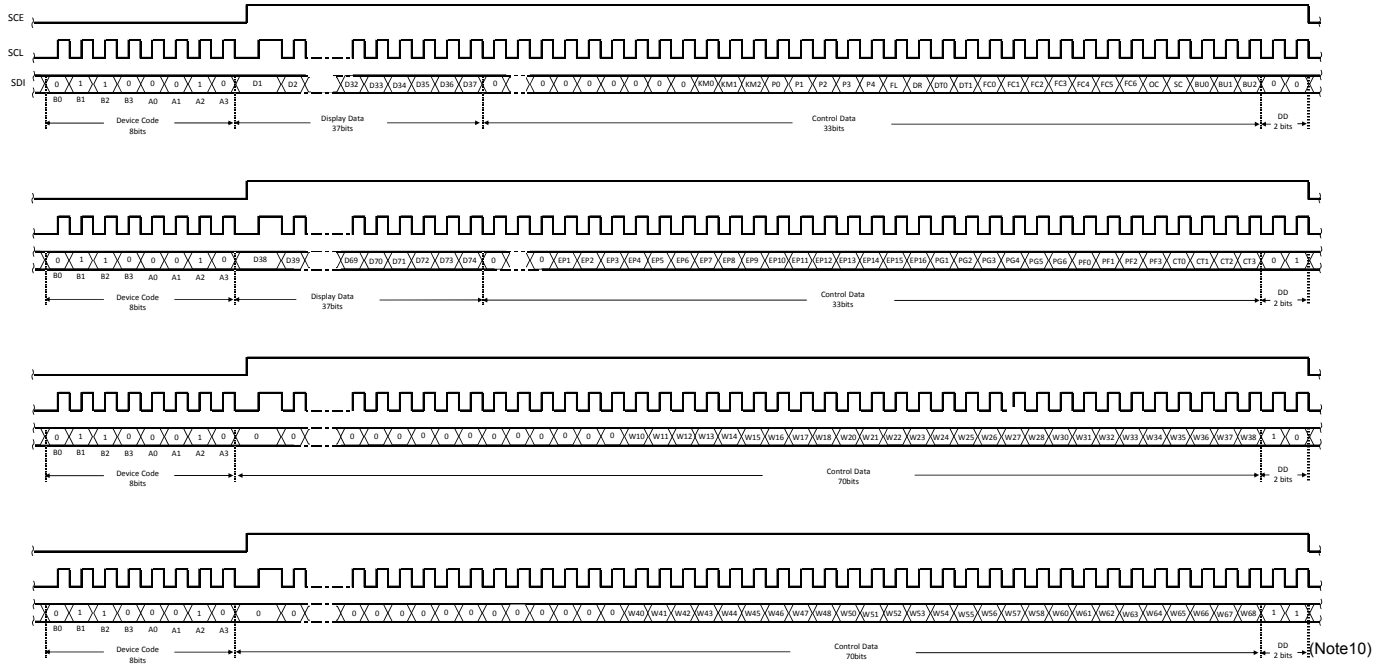


Figure 13. 3-SPI Data Transfer Format

(Note10) DD is direction data.

(2)When SCL is stopped at the high level

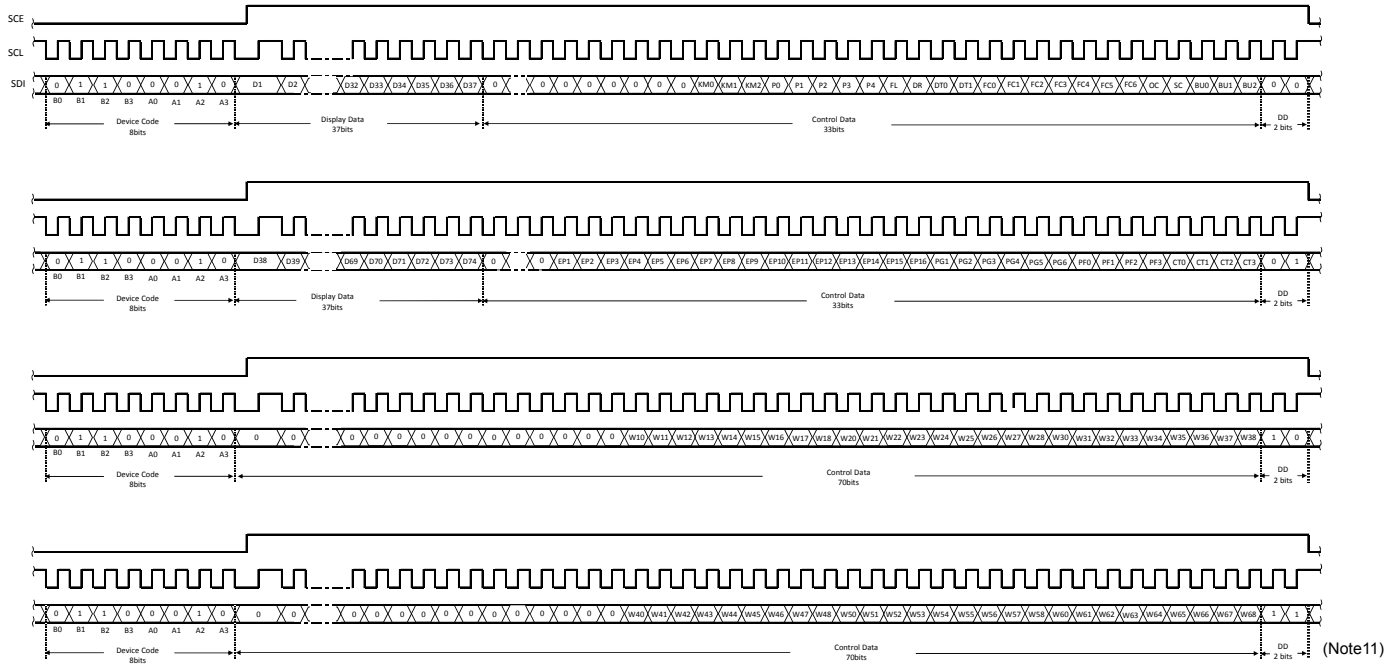


Figure 14. 3-SPI Data Transfer Format

(Note11) DD is direction data.

- Device code·····”46H”
- KM0～KM2·····Key Scan output port/Segment output port switching control data
- D1～D74·····Display data
- P0～P4·····Segment / PWM / General Purpose output port switching control data
- FL·····Line Inversion or Frame Inversion switching control data
- DR·····1/3 bias drive or 1/2 bias drive switching control data
- DT0~DT1·····1/4 duty drive, 1/3 duty drive, 1/2 duty drive or 1/1 duty(static) drive switching control data
- FC0～FC6·····Common/Segment output waveform frame frequency switching control data
- OC·····Internal oscillator operating mode/External clock operating mode switching control data
- SC·····Segment on/off switching control data
- BU0～BU2·····Normal mode/power-saving mode switching control data
- PG1 to PG6·····PWM/General Purpose Output(GPO) switching control data
- EP1 to EP16·····Internal PWM/External PWM switching control data (EP1-EP6), GPO/External PWM switching control data (EP7-EP16)
- PF0～PF3·····PWM output waveform frame frequency switching control data.
- CT0～CT3·····LCD display contrast switching control data.
- W10～W18, W20～W28, W30～W38, W40～W48, W50～W58, W60～W68 ·····PWM output duty switching control data

4. 1/1-Duty(Static)

(1)When SCL is stopped at the low level

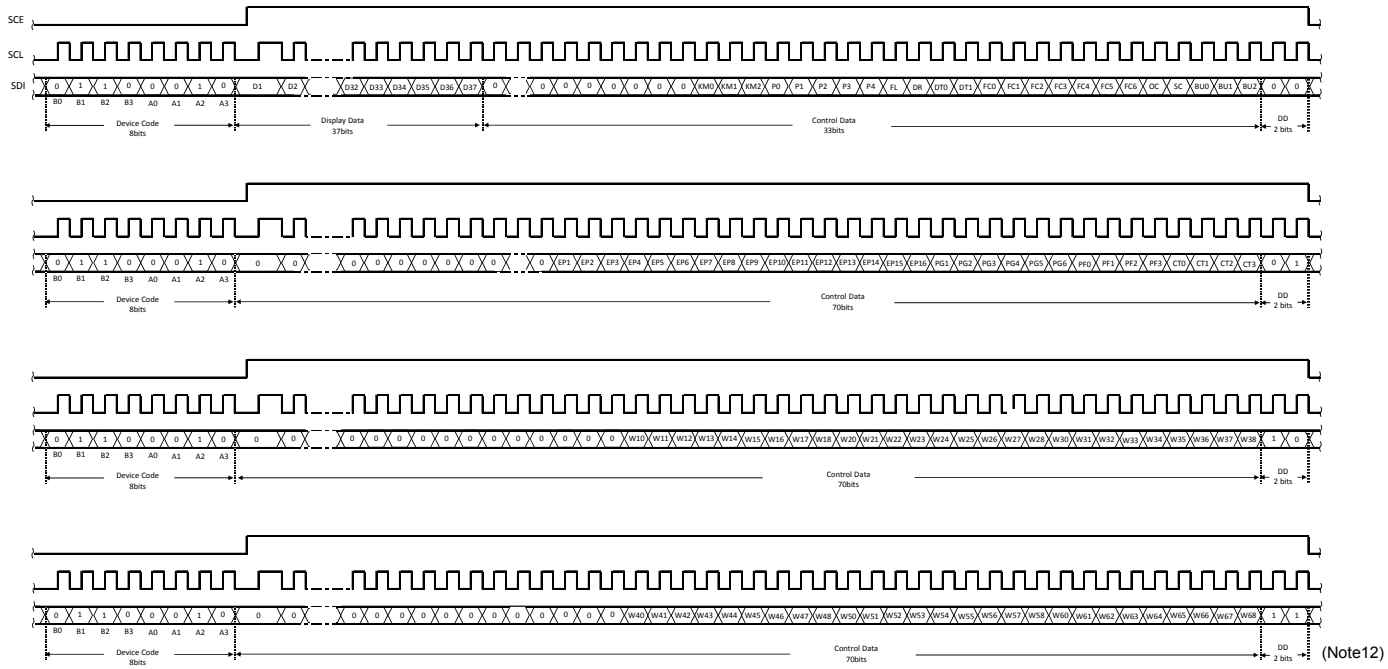


Figure 15. 3-SPI Data Transfer Format

(Note12) DD is direction data.

(2)When SCL is stopped at the high level

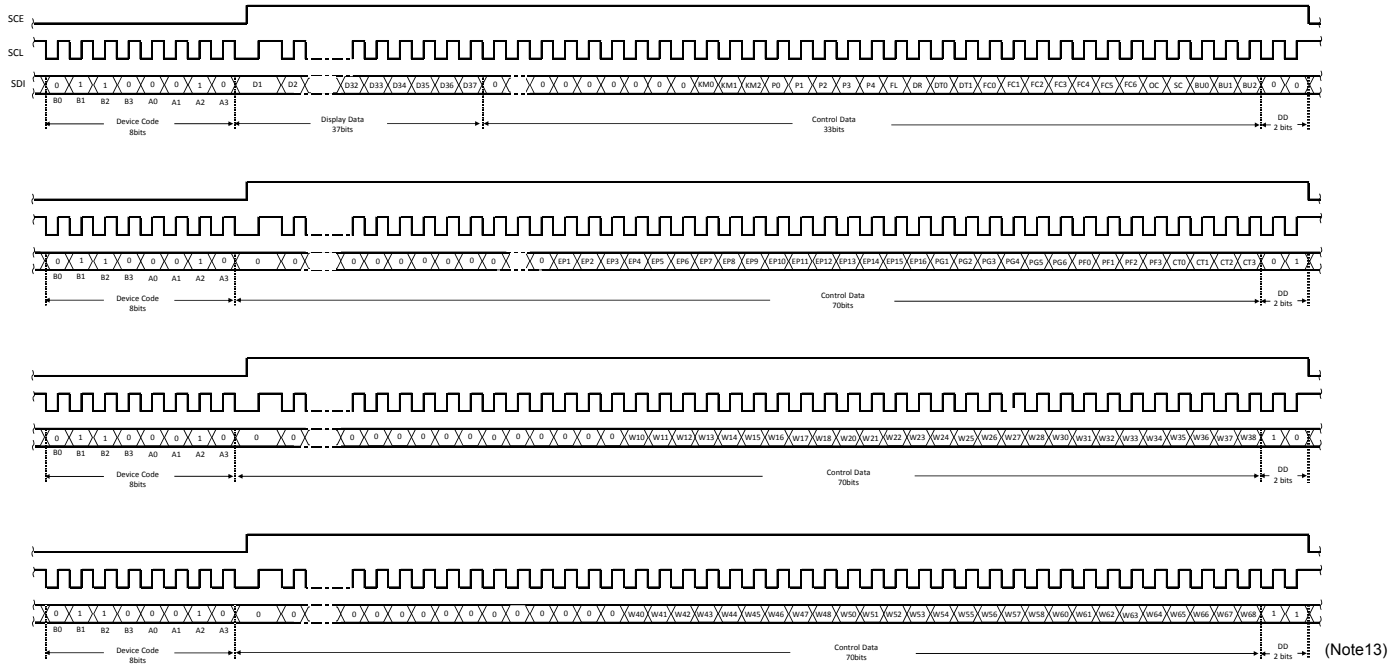


Figure 16. 3-SPI Data Transfer Format

(Note13) DD is direction data.

・Device code・・・・・・・・・・・・・・・・・・”46H”
・KM0～KM2・・・・・・・・・・・・・・・・・・Key Scan output port/Segment output port switching control data
・D1～D37・・・・・・・・・・・・・・・・・・・Display data
・P0～P4・・・・・・・・・・・・・・・・・・・・Segment / PWM / General Purpose output port switching control data
・FL・・・・・・・・・・・・・・・・・・・・・・・Line Inversion or Frame Inversion switching control data
・DR・・・・・・・・・・・・・・・・・・・・・・・1/3 bias drive or 1/2 bias drive switching control data
・DT0~DT1・・・・・・・・・・・・・・・・・・・1/4 duty drive, 1/3 duty drive, 1/2 duty drive or 1/1 duty(static) drive switching control data
・FC0～FC6・・・・・・・・・・・・・・・・・・Common/Segment output waveform frame frequency switching control data
・OC・・・・・・・・・・・・・・・・・・・・・・・ Internal oscillator operating mode/External clock operating mode switching control data
・SC・・・・・・・・・・・・・・・・・・・・・・・Segment on/off switching control data
・BU0～BU2・・・・・・・・・・・・・・・・・・Normal mode/power-saving mode switching control data
・PG1 to PG6・・・・・・・・・・・・・・・・・PWM/General Purpose Output(GPO) switching control data
・EP1 to EP16・・・・・・・・・・・・・・・・・Internal PWM/External PWM switching control data (EP1-EP6),
GPO/External PWM switching control data (EP7-EP16)
・PF0～PF3・・・・・・・・・・・・・・・・・・PWM output waveform frame frequency switching control data.
・CT0～CT3・・・・・・・・・・・・・・・・・・LCD display contrast switching control data.
・W10～W18, W20～W28, W30～W38,W40～W48, W50～W58, W60～W68
・・PWM output duty switching control data

Control Data Functions

1. KM0,KM1 and KM2: Key Scan output port/Segment output port switching control data
   These control data bits switch the functions of the KS1/S23 to KS5/S27 output pins between key scan output and segment output.

KM0	KM1	KM2	Output Pin State					Maximum Number of Input keys
			KS1/S23	KS2/S24	KS3/S25	KS4/S26	KS5/S27	
0	0	0	KS1	KS2	KS3	KS4	KS5	20
0	0	1	S23	KS2	KS3	KS4	KS5	16
0	1	0	S23	S24	KS3	KS4	KS5	12
0	1	1	S23	S24	S25	KS4	KS5	8
1	0	0	S23	S24	S25	S26	KS5	4
1	0	1	S23	S24	S25	S26	S27	0
1	1	0	S23	S24	S25	S26	S27	0
1	1	1	S23	S24	S25	S26	S27	0

2. P0,P1,P2,P3 and P4: Segment / PWM / General Purpose output port switching control data
   These control bits are used to select the function of the S5/P1/G1 to S20/P16/G16 output pins (Segment Output Pins or PWM Output Pins or General Purpose Output Pins).

P0	P1	P2	P3	P4	S5/ P1/ G1	S6/ P2/ G2	S7/ P3/ G3	S8/ P4/ G4	S9/ P5/ G5	S10/ P6/ G6	S11/ P7/ G7	S12/ P8/ G8
0	0	0	0	0	S5	S6	S7	S8	S9	S10	S11	S12
0	0	0	0	1	P1/G1	S6	S7	S8	S9	S10	S11	S12
0	0	0	1	0	P1/G1	P2/G2	S7	S8	S9	S10	S11	S12
0	0	0	1	1	P1/G1	P2/G2	P3/G3	S8	S9	S10	S11	S12
0	0	1	0	0	P1/G1	P2/G2	P3/G3	P4/G4	S9	S10	S11	S12
0	0	1	0	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	S10	S11	S12
0	0	1	1	0	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	S11	S12
0	0	1	1	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	S12
0	1	0	0	0	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8
0	1	0	0	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8
0	1	0	1	0	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8
0	1	0	1	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8
0	1	1	0	0	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8
0	1	1	0	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8
0	1	1	1	0	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8
0	1	1	1	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8
1	0	0	0	0	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8
1	0	0	0	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8
1	0	0	1	0	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8
1	0	0	1	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8
1	0	1	0	0	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8
1	0	1	0	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8
1	0	1	1	0	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8
1	0	1	1	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8
1	1	0	0	0	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8
1	1	0	0	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8
1	1	0	1	0	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8
1	1	0	1	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8
1	1	1	0	0	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8
1	1	1	0	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8
1	1	1	1	0	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8
1	1	1	1	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8

P0	P1	P2	P3	P4	S13/ P9/ G9	S14/ P10/ G10	S15/ P11/ G11	S16/ P12/ G12	S17/ P13/ G13	S18/ P14/ G14	S19/ P15/ G15	S20/ P16 G16
0	0	0	0	0	S13	S14	S15	S16	S17	S18	S19	S20
0	0	0	0	1	S13	S14	S15	S16	S17	S18	S19	S20
0	0	0	1	0	S13	S14	S15	S16	S17	S18	S19	S20
0	0	0	1	1	S13	S14	S15	S16	S17	S18	S19	S20
0	0	1	0	0	S13	S14	S15	S16	S17	S18	S19	S20
0	0	1	0	1	S13	S14	S15	S16	S17	S18	S19	S20
0	0	1	1	0	S13	S14	S15	S16	S17	S18	S19	S20
0	0	1	1	1	S13	S14	S15	S16	S17	S18	S19	S20
0	1	0	0	0	S13	S14	S15	S16	S17	S18	S19	S20
0	1	0	0	1	P9/G9	S14	S15	S16	S17	S18	S19	S20
0	1	0	1	0	P9/G9	P10/G10	S15	S16	S17	S18	S19	S20
0	1	0	1	1	P9/G9	P10/G10	P11/G11	S16	S17	S18	S19	S20
0	1	1	0	0	P9/G9	P10/G10	P11/G11	P12/G12	S17	S18	S19	S20
0	1	1	0	1	P9/G9	P10/G10	P11/G11	P12/G12	P13/G13	S18	S19	S20
0	1	1	1	0	P9/G9	P10/G10	P11/G11	P12/G12	P13/G13	P14/G14	S19	S20
0	1	1	1	1	P9/G9	P10/G10	P11/G11	P12/G12	P13/G13	P14/G14	P15/G15	S20
1	0	0	0	0	P9/G9	P10/G10	P11/G11	P12/G12	P13/G13	P14/G14	P15/G15	P16/G16
1	0	0	0	1	P9/G9	P10/G10	P11/G11	P12/G12	P13/G13	P14/G14	P15/G15	P16/G16
1	0	0	1	0	P9/G9	P10/G10	P11/G11	P12/G12	P13/G13	P14/G14	P15/G15	P16/G16
1	0	0	1	1	P9/G9	P10/G10	P11/G11	P12/G12	P13/G13	P14/G14	P15/G15	P16/G16
1	0	1	0	0	P9/G9	P10/G10	P11/G11	P12/G12	P13/G13	P14/G14	P15/G15	P16/G16
1	0	1	0	1	P9/G9	P10/G10	P11/G11	P12/G12	P13/G13	P14/G14	P15/G15	P16/G16
1	0	1	1	0	P9/G9	P10/G10	P11/G11	P12/G12	P13/G13	P14/G14	P15/G15	P16/G16
1	0	1	1	1	P9/G9	P10/G10	P11/G11	P12/G12	P13/G13	P14/G14	P15/G15	P16/G16
1	1	0	0	0	P9/G9	P10/G10	P11/G11	P12/G12	P13/G13	P14/G14	P15/G15	P16/G16
1	1	0	0	1	P9/G9	P10/G10	P11/G11	P12/G12	P13/G13	P14/G14	P15/G15	P16/G16
1	1	0	1	0	P9/G9	P10/G10	P11/G11	P12/G12	P13/G13	P14/G14	P15/G15	P16/G16
1	1	0	1	1	P9/G9	P10/G10	P11/G11	P12/G12	P13/G13	P14/G14	P15/G15	P16/G16
1	1	1	0	0	P9/G9	P10/G10	P11/G11	P12/G12	P13/G13	P14/G14	P15/G15	P16/G16
1	1	1	0	1	P9/G9	P10/G10	P11/G11	P12/G12	P13/G13	P14/G14	P15/G15	P16/G16
1	1	1	1	0	P9/G9	P10/G10	P11/G11	P12/G12	P13/G13	P14/G14	P15/G15	P16/G16
1	1	1	1	1	P9/G9	P10/G10	P11/G11	P12/G12	P13/G13	P14/G14	P15/G15	P16/G16

PWM output or General Purpose output is selected by PGx(x=1～6) control data bit
Internal PWM or external PWM output or General Purpose output is selected by EPx(x=1～6).
General Purpose or External PWM output or output is selected by EPx(x=7～16).

When the General Purpose Output Port Function is selected, the correspondence between the output pins and the respective display data is given in the table below.

Output Pins	Corresponding Display Data			
	1/4 Duty mode	1/3 Duty mode	1/2 Duty mode	1/1 Duty (static) mode
S5/P1/G1	D17	D13	D9	D5
S6/P2/G2	D21	D16	D11	D6
S7/P3/G3	D25	D19	D13	D7
S8/P4/G4	D29	D22	D15	D8
S9/P5/G5	D33	D25	D17	D9
S10/P6/G6	D37	D28	D19	D10
S11/P7/G7	D41	D31	D21	D11
S12/P8/G8	D45	D34	D23	D12
S13/P9/G9	D49	D37	D25	D13
S14/P10/G10	D53	D40	D27	D14
S15/P11/G11	D57	D43	D29	D15
S16/P12/G12	D61	D46	D31	D16
S17/P13/G13	D65	D49	D33	D17
S18/P14/G14	D69	D52	D35	D18
S19/P15/G15	D73	D55	D37	D19
S20/P16/G16	D77	D58	D39	D20

When the General Purpose Output Port Function is selected, the respective output pin outputs a “HIGH” level when its corresponding display data is set to “1”. Likewise, it will output a “LOW” level, if its corresponding display data is set to “0”. For example, at 1/4 Duty mode, S8/P4/G4 is used as a General Purpose Output Port, if its corresponding display data D29 is set to “1”, then S8/P4/G4 will output “HIGH” level. Likewise, if D29 is set to “0”, then S8/P4/G4 will output “LOW” level.

3. FL: Line Inversion or Frame Inversion switching control data
This control data bit selects either line inversion mode or frame inversion mode.

FL	Inversion mode
0	Line Inversion
1	Frame Inversion

4. DR: 1/3 bias drive or 1/2 bias drive switching control data
This control data bit selects either 1/3 bias drive or 1/2 bias drive.

DR	Bias drive scheme
0	1/3 bias drive
1	1/2 bias drive

5. DT: 1/4 duty drive, 1/3 duty drive, 1/2 duty drive or 1/1 duty(static) drive switching control data
These control data bits select either 1/4 duty drive, 1/3 duty drive, 1/2 duty drive or 1/1 duty (static) drive

DT0	DT1	Duty drive scheme
0	0	1/1 duty (static) drive
0	1	1/2 duty drive
1	0	1/3 duty drive
1	1	1/4 duty drive

6. FC0, FC1, FC2, FC3, FC4, FC5, and FC6: Common/Segment output waveform frame frequency switching control data
These control data bits set the frame frequency for common and segment output waveforms.

FC0	FC1	FC2	FC3	FC4	FC5	FC6	Frame Frequency fo(Hz)
0	0	0	0	0	0	0	fosc(Note14) /12000
0	0	0	0	0	0	1	fosc /10908
0	0	0	0	0	1	0	fosc /10000
0	0	0	0	0	1	1	fosc /9230
0	0	0	0	1	0	0	fosc /8572
0	0	0	0	1	0	1	fosc /8000
0	0	0	0	1	1	0	fosc /7500
0	0	0	0	1	1	1	fosc /7058
0	0	0	1	0	0	0	fosc /6666
0	0	0	1	0	0	1	fosc /6316
0	0	0	1	0	1	0	fosc /6000
0	0	0	1	0	1	1	fosc /5714
0	0	0	1	1	0	0	fosc /5454
0	0	0	1	1	0	1	fosc /5218
0	0	0	1	1	1	0	fosc /5000
0	0	0	1	1	1	1	fosc /4800
0	0	1	0	0	0	0	fosc /4616
0	0	1	0	0	0	1	fosc /4444
0	0	1	0	0	1	0	fosc /4286
0	0	1	0	0	1	1	fosc /4138
0	0	1	0	1	0	0	fosc /4000
0	0	1	0	1	0	1	fosc /3870
0	0	1	0	1	1	0	fosc /3750
0	0	1	0	1	1	1	fosc /3636
0	0	1	1	0	0	0	fosc /3530
0	0	1	1	0	0	1	fosc /3428
0	0	1	1	0	1	0	fosc /3334
0	0	1	1	0	1	1	fosc /3244
0	0	1	1	1	0	0	fosc /3158
0	0	1	1	1	0	1	fosc /3076
0	0	1	1	1	1	0	fosc /3000

FC0	FC1	FC2	FC3	FC4	FC5	FC6	Frame Frequency fo(Hz)
0	0	1	1	1	1	1	fosc /2926
0	1	0	0	0	0	0	fosc /2858
0	1	0	0	0	0	1	fosc /2790
0	1	0	0	0	1	0	fosc /2728
0	1	0	0	0	1	1	fosc /2666
0	1	0	0	1	0	0	fosc /2608
0	1	0	0	1	0	1	fosc /2554
0	1	0	0	1	1	0	fosc /2500
0	1	0	0	1	1	1	fosc /2448
0	1	0	1	0	0	0	fosc /2400
0	1	0	1	0	0	1	fosc /2352
0	1	0	1	0	1	0	fosc /2308
0	1	0	1	0	1	1	fosc /2264
0	1	0	1	1	0	0	fosc /2222
0	1	0	1	1	0	1	fosc /2182
0	1	0	1	1	1	0	fosc /2142
0	1	0	1	1	1	1	fosc /2106
0	1	1	0	0	0	0	fosc /2068
0	1	1	0	0	0	1	fosc /2034
0	1	1	0	0	1	0	fosc /2000
0	1	1	0	0	1	1	fosc /1968
0	1	1	0	1	0	0	fosc /1936
0	1	1	0	1	0	1	fosc /1904
0	1	1	0	1	1	0	fosc /1874
0	1	1	0	1	1	1	fosc /1846
0	1	1	1	0	0	0	fosc /1818
0	1	1	1	0	0	1	fosc /1792
0	1	1	1	0	1	0	fosc /1764
0	1	1	1	0	1	1	fosc /1740
0	1	1	1	1	0	0	fosc /1714
0	1	1	1	1	0	1	fosc /1690
0	1	1	1	1	1	0	fosc /1666
0	1	1	1	1	1	1	fosc /1644
1	0	0	0	0	0	0	fosc /1622
1	0	0	0	0	0	1	fosc /1600
1	0	0	0	0	1	0	fosc /1578
1	0	0	0	0	1	1	fosc /1558
1	0	0	0	1	0	0	fosc /1538
1	0	0	0	1	0	1	fosc /1518
1	0	0	0	1	1	0	fosc /1500
1	0	0	0	1	1	1	fosc /1482
1	0	0	1	0	0	0	fosc /1464
1	0	0	1	0	0	1	fosc /1446
1	0	0	1	0	1	0	fosc /1428
1	0	0	1	0	1	1	fosc /1412
1	0	0	1	1	0	0	fosc /1396
1	0	0	1	1	0	1	fosc /1380
1	0	0	1	1	1	0	fosc /1364
1	0	0	1	1	1	1	fosc /1348
1	0	1	0	0	0	0	fosc /1334

FC0	FC1	FC2	FC3	F4	FC5	FC6	Frame Frequency fo(Hz)
1	0	1	0	0	0	1	fosc /1318
1	0	1	0	0	1	0	fosc /1304
1	0	1	0	0	1	1	fosc /1290
1	0	1	0	1	0	0	fosc /1276
1	0	1	0	1	0	1	fosc /1264
1	0	1	0	1	1	0	fosc /1250
1	0	1	0	1	1	1	fosc /1238
1	0	1	1	0	0	0	fosc /1224
1	0	1	1	0	0	1	fosc /1212
1	0	1	1	0	1	0	fosc /1200
1	0	1	1	0	1	1	fosc /1188
1	0	1	1	1	0	0	fosc /1176
1	0	1	1	1	0	1	fosc /1166
1	0	1	1	1	1	0	fosc /1154
1	0	1	1	1	1	1	fosc /1142
1	1	0	0	0	0	0	fosc /1132
1	1	0	0	0	0	1	fosc /1122
1	1	0	0	0	1	0	fosc /1112
1	1	0	0	0	1	1	fosc /1100
1	1	0	0	1	0	0	fosc /1090
1	1	0	0	1	0	1	fosc /1082
1	1	0	0	1	1	0	fosc /1072
1	1	0	0	1	1	1	fosc /1062
1	1	0	1	0	0	0	fosc /1052
1	1	0	1	0	0	1	fosc /1044
1	1	0	1	0	1	0	fosc /1034
1	1	0	1	0	1	1	fosc /1026
1	1	0	1	1	0	0	fosc /1016
1	1	0	1	1	0	1	fosc /1008
1	1	0	1	1	1	0	fosc /1000
1	1	0	1	1	1	1	fosc /992
1	1	1	0	0	0	0	fosc /984
1	1	1	0	0	0	1	fosc /976
1	1	1	0	0	1	0	fosc /968
1	1	1	0	0	1	1	fosc /960
1	1	1	0	1	0	0	fosc /952
1	1	1	0	1	0	1	fosc /944
1	1	1	0	1	1	0	fosc /938
1	1	1	0	1	1	1	fosc /930
1	1	1	1	0	0	0	fosc /924
1	1	1	1	0	0	1	fosc /916
1	1	1	1	0	1	0	fosc /910
1	1	1	1	0	1	1	fosc /902
1	1	1	1	1	0	0	fosc /896
1	1	1	1	1	0	1	fosc /888
1	1	1	1	1	1	0	fosc /882
1	1	1	1	1	1	1	fosc /876

(Note14) fosc: Internal oscillation frequency (600 [kHz] typ.)

7. OC: Internal oscillator operating mode/External clock operating mode switching control data in OSCIN/S37
These control data bits select

OC	Operating mode	In/Out pin(OSCIN/S37) status
0	Internal oscillator	S37 (segment output)
1	External Clock	OSCIN (clock input)

8. SC: Segment on/off switching control data
This control data bit controls the on/off state of the segments.

SC	Display state
0	On
1	Off

Note that when the segments are turned off by setting SC to "1", the segments are turned off by outputting segment off waveforms from the segment output pins.

9. BU0,BU1 and BU2: Normal mode/power-saving mode switching control data
These control data bits select either normal mode or power-saving mode.

BU0	BU1	BU2	Mode	OSC Oscillator	Segment outputs Common outputs	Output Pin States During Key Scan Standby				
						KS1	KS2	KS3	KS4	KS5
0	0	0	Normal	Operating	Operating	H	H	H	H	H
0	0	1	Power-saving	Stopped	Low(VSS)	L	L	L	L	H
0	1	0				L	L	L	H	H
0	1	1				L	L	H	H	H
1	0	0				L	H	H	H	H
1	0	1				H	H	H	H	H
1	1	0				H	H	H	H	H
1	1	1				H	H	H	H	H

Power-saving mode status: S5/P1/G1 to S20/P16/G16 = active only General Purpose output
S21 to S22 = low (VSS)
KS1/S23 to KS5/S27 = low (VSS)
KI1/S32 to KS4/S35 = low (VSS)
PWMIN/S36 = low (VSS)
OSCIN/S37 = low (VSS)
COM1 to COM4 = low (VSS)
Stop the LCD drive bias voltage generation circuit
Stop the Internal oscillation circuit
However, serial data transfer is possible when at Power-saving mode.

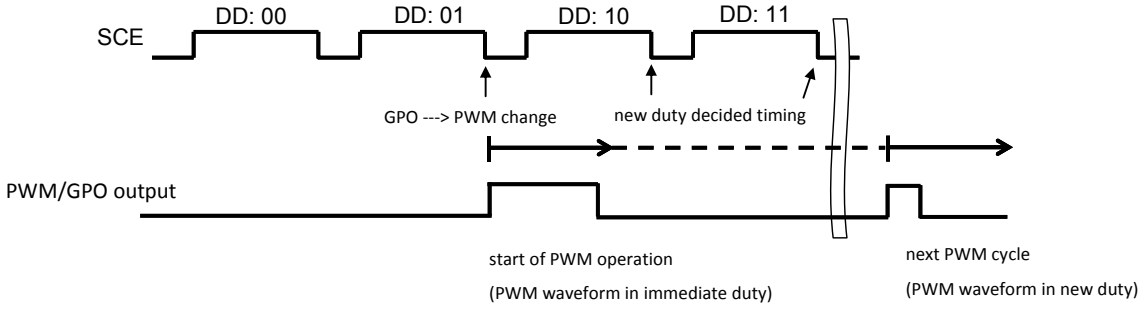
10. PG1, PG2, PG3, PG4, PG5 and PG6 : PWM/General Purpose output switching control data
This control data bit select either PWM output or General Purpose output of Px/Gx pins. (x=1～6)

PGx(x=1～6)	Px/Gx pin status
0	PWM output
1	General Purpose output

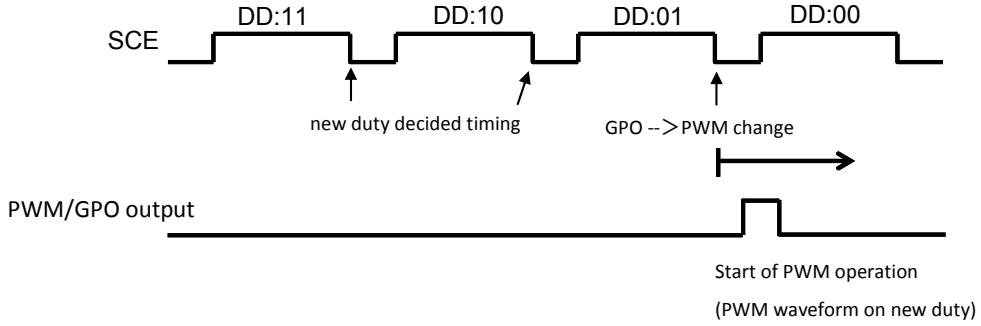
<PWM<->GPO Changing function>

Normal behavior of changing GPO to PWM is below.

- PWM operation is started by command import timing of DD: 01 during GPO -→ PWM change.
- Please take care of reflect timing of new duty setting of DD: 10 and DD: 11 is from the next PWM.



In order to avoid this operation, please input commands in reverse as below.



11. PF0, PF1, PF2, and PF3: PWM output waveform frame frequency switching control data
These control data bits set the frame frequency for PWM output waveforms.

PF0	PF1	PF2	PF3	PWM output Frame Frequency fp(Hz)
0	0	0	0	fosc / 4096
0	0	0	1	fosc / 3840
0	0	1	0	fosc / 3584
0	0	1	1	fosc / 3328
0	1	0	0	fosc / 3072
0	1	0	1	fosc / 2816
0	1	1	0	fosc / 2560
0	1	1	1	fosc / 2304
1	0	0	0	fosc / 2048
1	0	0	1	fosc / 1792
1	0	1	0	fosc / 1536
1	0	1	1	fosc / 1280
1	1	0	0	fosc / 1024
1	1	0	1	fosc / 768
1	1	1	0	fosc / 512
1	1	1	1	fosc / 256

12. CT0, CT1, CT2 and CT3: LCD display contrast switching control data
These control data bits set display contrast

CT0	CT1	CT2	CT3	LCD Drive bias voltage for VLCD Level
0	0	0	0	1.000*VDD
0	0	0	1	0.975*VDD
0	0	1	0	0.950*VDD
0	0	1	1	0.925*VDD
0	1	0	0	0.900*VDD
0	1	0	1	0.875*VDD
0	1	1	0	0.850*VDD
0	1	1	1	0.825*VDD
1	0	0	0	0.800*VDD
1	0	0	1	0.775*VDD
1	0	1	0	0.750*VDD
1	0	1	1	0.725*VDD
1	1	0	0	0.700*VDD
1	1	0	1	0.675*VDD
1	1	1	0	0.650*VDD
1	1	1	1	0.625*VDD

13. EP1, EP2, EP3, EP4, EP5,EP7,EP8,EP9,EP10,EP11,EP12,EP13,EP14,EP15 and EP16 :
Internal PWM/External PWM switching control data (EP1-EP6),
GPO/External PWM switching control data (EP7-EP16)
This control data bit select either External PWM output or internal generation PWM output of Px/Gx pins by x=1～6.

EPx(x=1～6)	Mode
0	Internal PWM output
1	External PWM output

When a state of PGx(x=1～6) = “0”, the setting of EPx(x=1～6) becomes effective.

This control data bit select either GPO or external PWM output of Px/Gx pins by x=7～16.

EPx(x=7～16)	Mode
0	GPO
1	External PWM output

14. W10～W18[(Note15)], W20～W28, W30～W38, W40～W48, W50～W58 and W60～W68 : PWM output waveform duty setting control data.
These control data bits set the high level pulse width (duty) for PWM output waveforms.

N = 1 ~ 6 , Tp = 1/fp

Wn0	Wn1	Wn2	Wn3	Wn4	Wn5	Wn6	Wn7	Wn8	PWM duty
0	0	0	0	0	0	0	0	0	(0/256) x Tp
0	0	0	0	0	0	0	0	1	(1/256) x Tp
0	0	0	0	0	0	0	1	0	(2/256) x Tp
0	0	0	0	0	0	0	1	1	(3/256) x Tp
0	0	0	0	0	0	1	0	0	(4/256) x Tp
0	0	0	0	0	0	1	0	1	(5/256) x Tp
0	0	0	0	0	0	1	1	0	(6/256) x Tp
0	0	0	0	0	0	1	1	1	(7/256) x Tp
0	0	0	0	0	1	0	0	0	(8/256) x Tp
0	0	0	0	0	1	0	0	1	(9/256) x Tp
0	0	0	0	0	1	0	1	0	(10/256) x Tp
0	0	0	0	0	1	0	1	1	(11/256) x Tp
0	0	0	0	0	1	1	0	0	(12/256) x Tp
0	0	0	0	0	1	1	0	1	(13/256) x Tp
0	0	0	0	0	1	1	1	0	(14/256) x Tp
0	0	0	0	0	1	1	1	1	(15/256) x Tp
0	0	0	0	1	0	0	0	0	(16/256) x Tp
0	0	0	0	1	0	0	0	1	(17/256) x Tp
0	0	0	0	1	0	0	1	0	(18/256) x Tp
0	0	0	0	1	0	0	1	1	(19/256) x Tp
0	0	0	0	1	0	1	0	0	(20/256) x Tp
・・・	・・・	・・・	・・・	・・・	・・・	・・・	・・・	・・・	・・・
0	1	1	1	0	1	0	1	1	(235/256) x Tp
0	1	1	1	0	1	1	0	0	(236/256) x Tp
0	1	1	1	0	1	1	0	1	(237/256) x Tp
0	1	1	1	0	1	1	1	0	(238/256) x Tp
0	1	1	1	0	1	1	1	1	(239/256) x Tp
0	1	1	1	1	0	0	0	0	(240/256) x Tp
0	1	1	1	1	0	0	0	1	(241/256) x Tp
0	1	1	1	1	0	0	1	0	(242/256) x Tp
0	1	1	1	1	0	0	1	1	(243/256) x Tp
0	1	1	1	1	0	1	0	0	(244/256) x Tp
0	1	1	1	1	0	1	0	1	(245/256) x Tp
0	1	1	1	1	0	1	1	0	(246/256) x Tp
0	1	1	1	1	0	1	1	1	(247/256) x Tp
0	1	1	1	1	1	0	0	0	(248/256) x Tp
0	1	1	1	1	1	0	0	1	(249/256) x Tp
0	1	1	1	1	1	0	1	0	(250/256) x Tp
0	1	1	1	1	1	0	1	1	(251/256) x Tp
0	1	1	1	1	1	1	0	0	(252/256) x Tp
0	1	1	1	1	1	1	0	1	(253/256) x Tp
0	1	1	1	1	1	1	1	0	(254/256) x Tp
0	1	1	1	1	1	1	1	1	(255/256) x Tp
1	0	0	0	0	0	0	0	0	(256/256) x Tp
1	0	0	0	0	0	0	0	1	(256/256) x Tp
1	0	0	0	0	0	0	1	0	(256/256) x Tp
1	0	0	0	0	0	0	1	1	(256/256) x Tp
・・・	・・・	・・・	・・・	・・・	・・・	・・・	・・・	・・・	・・・
1	1	1	1	1	1	1	0	0	(256/256) x Tp
1	1	1	1	1	1	1	0	1	(256/256) x Tp
1	1	1	1	1	1	1	1	0	(256/256) x Tp
1	1	1	1	1	1	1	1	1	(256/256) x Tp

(Note15) W10～W18:S5/P1/G1 pwm duty data
W20～W28:S6/P2/G2 pwm duty data
W30～W38:S7/P3/G3 pwm duty data
W40～W48:S8/P4/G4 pwm duty data
W50～W58:S9/P5/G5 pwm duty data
W60～W68:S10/P6/G6 pwm duty data

Display Data and Output Pin Correspondence

1.1/4 duty

Output pin(Note16)	COM1	COM2	COM3	COM4
S1	D1	D2	D3	D4
S2	D5	D6	D7	D8
S3	D9	D10	D11	D12
S4	D13	D14	D15	D16
S5/P1/G1	D17	D18	D19	D20
S6/P2/G2	D21	D22	D23	D24
S7/P3/G3	D25	D26	D27	D28
S8/P4/G4	D29	D30	D31	D32
S9/P5/G5	D33	D34	D35	D36
S10/P6/G6	D37	D38	D39	D40
S11/P7/G7	D41	D42	D43	D44
S12/P8/G8	D45	D46	D47	D48
S13/P9/G9	D49	D50	D51	D52
S14/P10/G10	D53	D54	D55	D56
S15/P11/G11	D57	D58	D59	D60
S16/P12/G12	D61	D62	D63	D64
S17/P13/G13	D65	D66	D67	D68
S18/P14/G14	D69	D70	D71	D72
S19/P15/G15	D73	D74	D75	D76
S20/P16/G16	D77	D78	D79	D80
S21	D81	D82	D83	D84
S22	D85	D86	D87	D88
KS1/S23	D89	D90	D91	D92
KS2/S24	D93	D94	D95	D96
KS3/S25	D97	D98	D99	D100
KS4/S26	D101	D102	D103	D104
KS5/S27	D105	D106	D107	D108
S28	D109	D110	D111	D112
S29	D113	D114	D115	D116
S30	D117	D118	D119	D120
S31	D121	D122	D123	D124
KI1/S32	D125	D126	D127	D128
KI2/S33	D129	D130	D131	D132
KI3/S34	D133	D134	D135	D136
KI4/S35	D137	D138	D139	D140
PWMIN/S36	D141	D142	D143	D144
OSCIN/S37	D145	D146	D147	D148

(Note16) The Segment Output Port function is assumed to be selected for the output pins – S5/P1/G1 to S20/P16/G16, KS1/S23 to KS5/S27, KI1/S32 to KI4/S35, PWMIN/S36, OSCIN/S37.
In BU97600FV-M, S1-S4 and S28-S31 are not available.

To illustrate further, the states of the S21 output pin is given in the table below.

Display data				State of S21 Output Pin
D81	D82	D83	D84	
0	0	0	0	LCD Segments corresponding to COM1 to COM4 are OFF.
0	0	0	1	LCD Segment corresponding to COM4 is ON.
0	0	1	0	LCD Segment corresponding to COM3 is ON.
0	0	1	1	LCD Segments corresponding to COM3 and COM4 are ON.
0	1	0	0	LCD Segment corresponding to COM2 is ON.
0	1	0	1	LCD Segments corresponding to COM2 and COM4 are ON.
0	1	1	0	LCD Segments corresponding to COM2 and COM3 are ON.
0	1	1	1	LCD Segments corresponding to COM2, COM3 and COM4 are ON.
1	0	0	0	LCD Segment corresponding to COM1 is ON.
1	0	0	1	LCD Segments corresponding to COM1 and COM4 are ON.
1	0	1	0	LCD Segments corresponding to COM1 and COM3 are ON.
1	0	1	1	LCD Segments corresponding to COM1, COM3 and COM4 are ON.
1	1	0	0	LCD Segments corresponding to COM1 and COM2 are ON.
1	1	0	1	LCD Segments corresponding to COM1, COM2, and COM4 are ON.
1	1	1	0	LCD Segments corresponding to COM1, COM2, and COM3 are ON.
1	1	1	1	LCD Segments corresponding to COM1, COM2, COM3 and COM4 are ON.

2. 1/3 duty

Output pin(Note17)	COM1	COM2	COM3
S1	D1	D2	D3
S2	D4	D5	D6
S3	D7	D8	D9
S4	D10	D11	D12
S5/P1/G1	D13	D14	D15
S6/P2/G2	D16	D17	D18
S7/P3/G3	D19	D20	D21
S8/P4/G4	D22	D23	D24
S9/P5/G5	D25	D26	D27
S10/P6/G6	D28	D29	D30
S11/P7/G7	D31	D32	D33
S12/P8/G8	D34	D35	D36
S13/P9/G9	D37	D38	D39
S14/P10/G10	D40	D41	D42
S15/P11/G11	D43	D44	D45
S16/P12/G12	D46	D47	D48
S17/P13/G13	D49	D50	D51
S18/P14/G14	D52	D53	D54
S19/P15/G15	D55	D56	D57
S20/P16/G16	D58	D59	D60
S21	D61	D62	D63
S22	D64	D65	D66
KS1/S23	D67	D68	D69
KS2/S24	D70	D71	D72
KS3/S25	D73	D74	D75
KS4/S26	D76	D77	D78
KS5/S27	D79	D80	D81
S28	D82	D83	D84
S29	D85	D85	D87
S30	D88	D89	D90
S31	D91	D92	D93
KI1/S32	D94	D95	D96
KI2/S33	D97	D98	D99
KI3/S34	D100	D101	D102
KI4/S35	D103	D104	D105
PWMIN/S36	D106	D107	D108
OSCIN/S37	D109	D110	D111

(Note17) The Segment Output Port function is assumed to be selected for the output pins – S5/P1/G1 to S20/P16/G16, KS1/S23 to KS5/S27, KI1/S32 to KI4/S35, PWMIN/S36, OSCIN/S37.
In BU97600FV-M, S1-S4 and S28-S31,S32-S35 are not available.

To illustrate further, the states of the S21 output pin is given in the table below.

Display data			State of S21 Output Pin
D61	D62	D63	
0	0	0	LCD Segments corresponding to COM1 to COM3 are OFF.
0	0	1	LCD Segment corresponding to COM3 is ON.
0	1	0	LCD Segment corresponding to COM2 is ON.
0	1	1	LCD Segments corresponding to COM2 and COM3 are ON.
1	0	0	LCD Segment corresponding to COM1 is ON.
1	0	1	LCD Segments corresponding to COM1 and COM3 are ON.
1	1	0	LCD Segments corresponding to COM1 and COM2 are ON.
1	1	1	LCD Segments corresponding to COM1, COM2 and COM3 are ON.

3. 1/2 duty

Output pin(Note18)	COM1	COM2
S1	D1	D2
S2	D3	D4
S3	D5	D6
S4	D7	D8
S5/P1/G1	D9	D10
S6/P2/G2	D11	D12
S7/P3/G3	D13	D14
S8/P4/G4	D15	D16
S9/P5/G5	D17	D18
S10/P6/G6	D19	D20
S11/P7/G7	D21	D22
S12/P8/G8	D23	D24
S13/P9/G9	D25	D26
S14/P10/G10	D27	D28
S15/P11/G11	D29	D30
S16/P12/G12	D31	D32
S17/P13/G13	D33	D34
S18/P14/G14	D35	D36
S19/P15/G15	D37	D38
S20/P16/G16	D39	D40
S21	D41	D42
S22	D43	D44
KS1/S23	D45	D46
KS2/S24	D47	D48
KS3/S25	D49	D50
KS4/S26	D51	D52
KS5/S27	D53	D54
S28	D55	D56
S29	D57	D58
S30	D59	D60
S31	D61	D62
KI1/S32	D63	D64
KI2/S33	D65	D66
KI3/S34	D67	D68
KI4/S35	D69	D70
PWMIN/S36	D71	D72
OSCIN/S37	D73	D74

(Note18) The Segment Output Port function is assumed to be selected for the output pins – S5/P1/G1 to S20/P16/G16, KS1/S23 to KS5/S27, KI1/S32 to KI4/S35, PWMIN/S36, OSCIN/S37.
In BU97600FV-M, S1-S4 and S28-S31 are not available.

To illustrate further, the states of the S21 output pin is given in the table below.

Display data		State of S21 Output Pin
D41	D42	
0	0	LCD Segments corresponding to COM1 to COM2 are OFF.
0	1	LCD Segment corresponding to COM2 is ON.
1	0	LCD Segment corresponding to COM1 is ON.
1	1	LCD Segments corresponding to COM1 and COM2 are ON.

4. 1/1 duty(Static)

Output pin(Note19)	COM1
S1	D1
S2	D2
S3	D3
S4	D4
S5/P1/G1	D5
S6/P2/G2	D6
S7/P3/G3	D7
S8/P4/G4	D8
S9/P5/G5	D9
S10/P6/G6	D10
S11/P7/G7	D11
S12/P8/G8	D12
S13/P9/G9	D13
S14/P10/G10	D14
S15/P11/G11	D15
S16/P12/G12	D16
S17/P13/G13	D17
S18/P14/G14	D18
S19/P15/G15	D19
S20/P16/G16	D20
S21	D21
S22	D22
KS1/S23	D23
KS2/S24	D24
KS3/S25	D25
KS4/S26	D26
KS5/S27	D27
S28	D28
S29	D29
S30	D30
S31	D31
KI1/S32	D32
KI2/S33	D33
KI3/S34	D34
KI4/S35	D35
PWMIN/S36	D36
OSCIN/S37	D37

(Note19) The Segment Output Port function is assumed to be selected for the output pins – S5/P1/G1 to S20/P16/G16, KS1/S23 to KS5/S27, KI1/S32 to KI4/S35, PWMIN/S36, OSCIN/S37.
In BU97600FV-M, S1-S4 and S28-S31 are not available.

To illustrate further, the states of the S21 output pin is given in the table below.

Display data D21	State of S21 Output Pin
0	LCD Segment corresponding to COM1 is ON.
1	LCD Segment corresponding to COM1 is OFF.

Serial Data Output

1. When SCL is stopped at the low level(Note20)

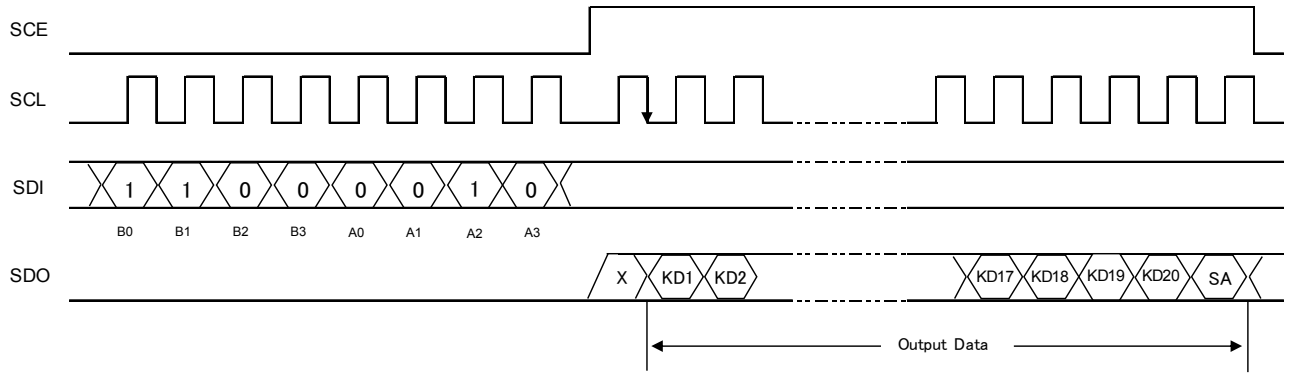


Figure 17. Serial Data Output Format

(Note20)
1. X=Don't care
2. B0 to B3, A0 to A3: Serial Interface address

2. When SCL is stopped at the high level(Note21)

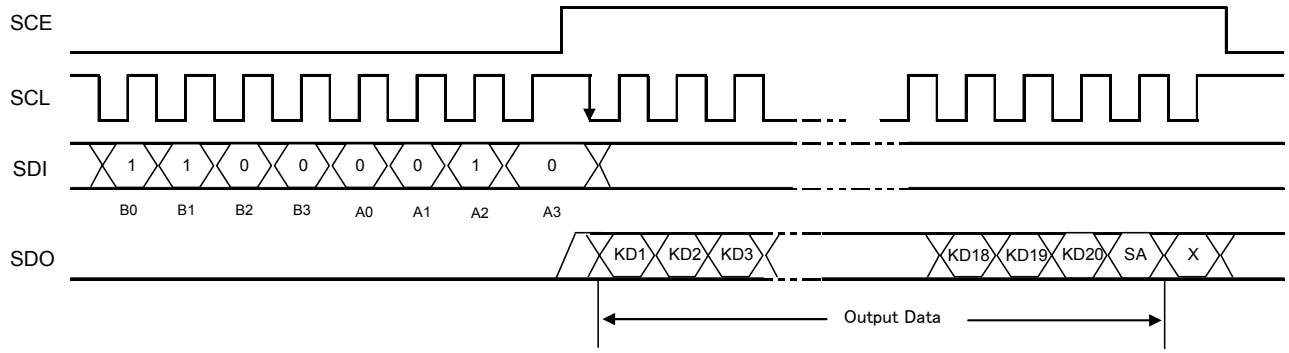


Figure 18. Serial Data Output Format

(Note21)
1. X=Don't care
2. B0 to B3, A0 to A3: Serial Interface address
3. Serial Interface address: 43H
4. KD1 to KD20: Key data
5. SA: Sleep acknowledge data
6. If a key data read operation is executed when SDO is high, the read key data (KD1 to KD20) and sleep acknowledge data (SA) will be invalid.

Output Data

1. KD1 TO KD20: KEY DATA

When a key matrix of up to 20 keys is formed from the KS1 to KS5 output pins and the KI1 to KI4 input pins and one of those keys is pressed, the key output data corresponding to that key will be set to 1. The table shows the relationship between those pins and the key data bits.

Item	KI1	KI2	KI3	KI4
KS1	KD1	KD2	KD3	KD4
KS2	KD5	KD6	KD7	KD8
KS3	KD9	KD10	KD11	KD12
KS4	KD13	KD14	KD15	KD16
KS5	KD17	KD18	KD19	KD20

2. SA: Sleep Acknowledge Data

This output data is set to the state when the key is pressed. In that case SDO will go to the low level. If serial data is input during this period and the mode is set (normal mode or sleep mode), the IC will be set to that mode. SA is set to 1 in the sleep mode and to 0 in the normal mode.

Sleep Mode

Sleep mode is set up by setting the BU0 to BU2 in the control data to 1. The segment outputs will all go low and the common outputs will also go low, and the oscillator on the OSC pin will stop (it will be started by a key press). This reduces power dissipation. This mode is cleared by sending control data with all the BU0 to BU2 set to 0. However, note that the S5/P1/G1 to S20/P16/G16 outputs can be used as general-purpose output ports according to the state of the P0 to P4 control data bits, even in sleep mode. (See Control Data Functions.)

Key Scan Operation Function

1. Key scan timing

The key scan period is 4640T(s). To reliably determine the on/off state of the keys, the BU97600FV-M/ BU97600FUV-M scans the keys twice and determines that a key has been pressed when the key data agrees. It outputs a key data read request (a low level on SDO) 9904T(s) after starting a key scan. If the key data does not agree and a key was pressed at that point, it scans the keys again. Thus the BU97600FV-M/ BU97600FUV-M cannot detect a key press shorter than 9904T(s).

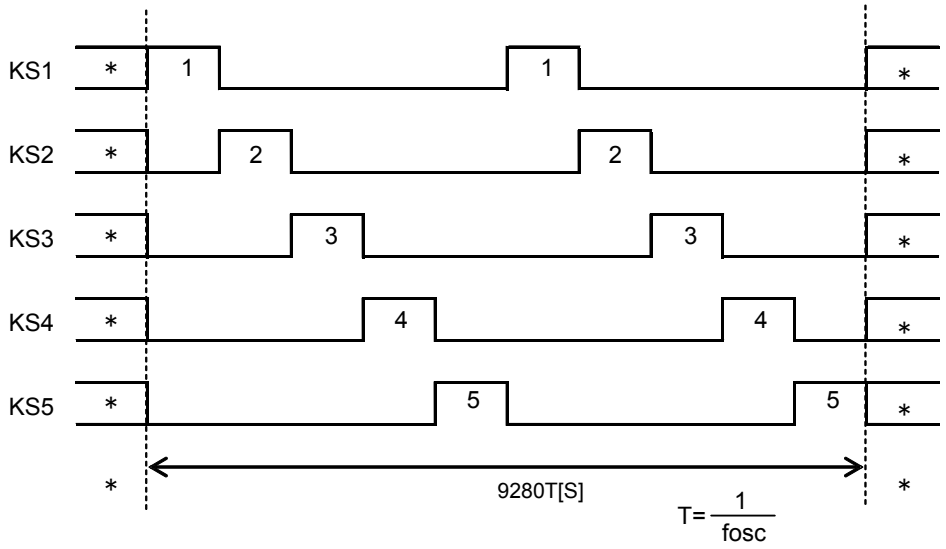


Figure 19. Key Scan Timing(Note22)

(Note22) In sleep mode the high/low state of these pins is determined by the BU0 to BU2 bits in the control data. Key scan output signals are not output from pins that are set "L".

2. In Normal Mode
The pins KS1 to KS5 are set "H".
When a key is pressed a key scan is started and the keys are scanned until all keys are released. Multiple key presses are recognized by determining whether multiple key data bits are set.
If a key is pressed for longer than 9904T(s) (Where T=1/fosc) the BU97600FV-M/ BU97600FUV-M outputs a key data read request (a low level on SDO) to the controller. The controller acknowledges this request and reads the key data. However, if SCE is high during a serial data transfer, SDO will be set "H".
After the controller reads the key data, the key data read request is cleared (SDO is set high) and the BU97600FV-M/ BU97600FUV-M performs another key scan. Also note that SDO, being an open-drain output, requires a pull-up resistor (between 1 KΩ and 10KΩ)

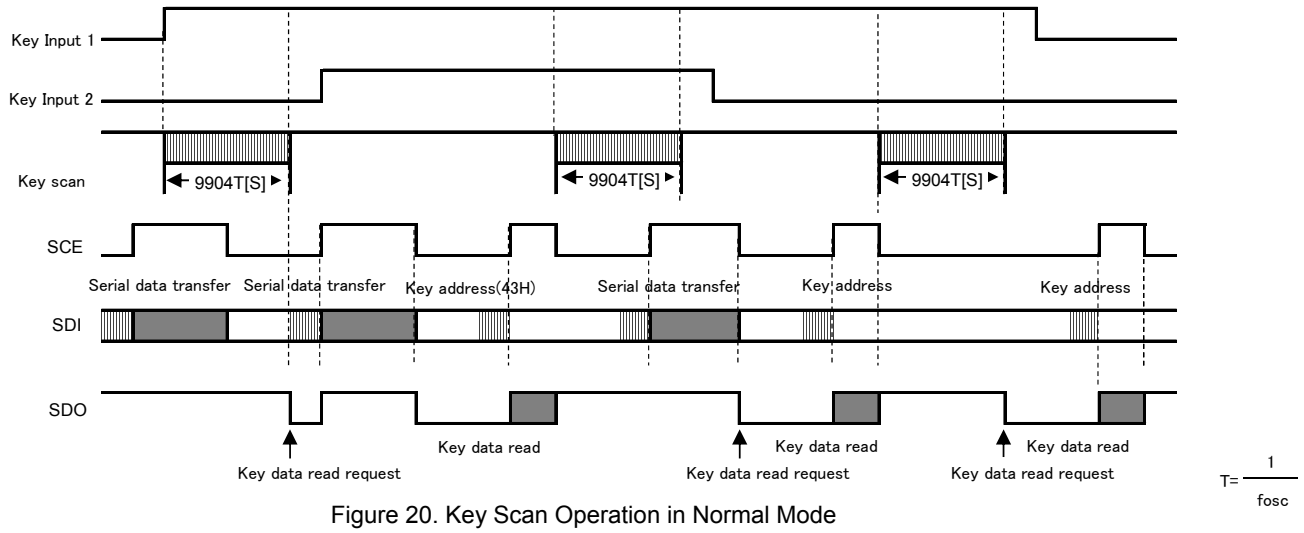
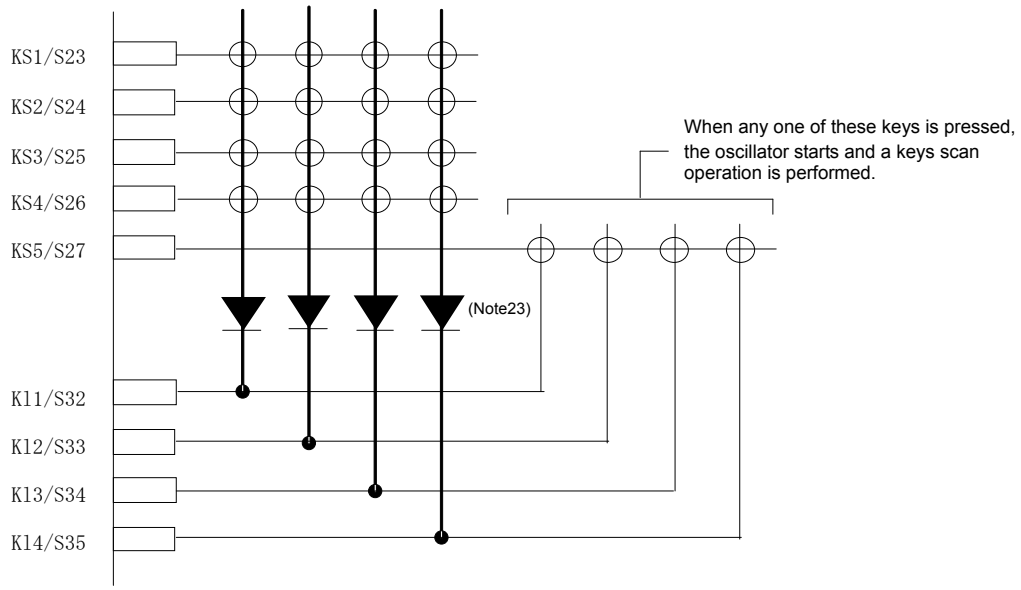


Figure 20. Key Scan Operation in Normal Mode

3. In sleep mode
The pins KS1 to KS5 are set to high or low by the BU0 to BU2 bits in the control data. (See the control data description for details.)
If a key on one of the lines corresponding to a KS1 to KS5 pin which is set high is pressed, the oscillator on the OSC pin is started and a key scan is performed. Keys are scanned until all keys are released. Multiple key presses are recognized by determining whether multiple key data bits are set.
If a key is pressed for longer than 9904T(s)(Where T=1/fosc) the BU97600FV-M/BU97600FUV-M outputs a key data read request (a low level on SDO) to the controller. The controller acknowledges this request and reads the key data. However, if SCE is high during a serial data transfer, SDO will be set high.
After the controller reads the key data, the key data read request is cleared (SDO is set high) and the BU97600FV-M/BU97600FUV-M performs another key scan. However, this does not clear sleep mode. Also note that SDO, being an open-drain output, requires a pull-up resistor (between 1 KΩ and 10KΩ).

Sleep mode key scan example

Example: BU0=0, BU1=0, BU2=1 (sleep with only KS5 high)



(Note23)
These diodes are required to reliable recognize multiple key presses on the KS5 line when sleep mode state with only KS5 high, as in the above example. That is, these diodes prevent incorrect operations due to sneak currents in the KS5 key scan output signal when keys on the KS1 to KS5 lines are pressed at the same time.

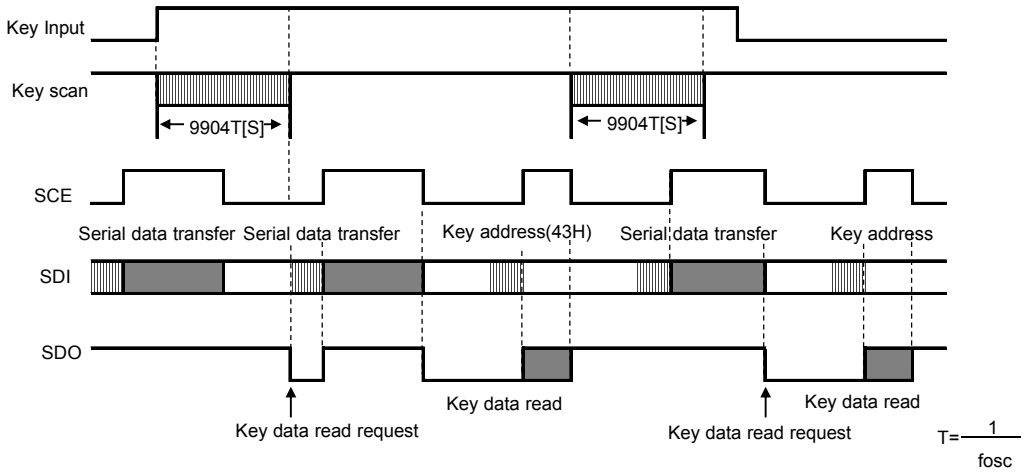


Figure 21. Key Scan Operation in Sleep Mode

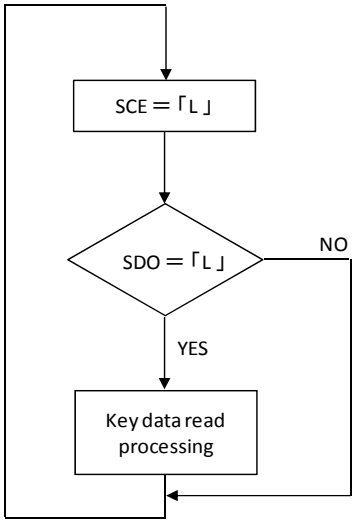
Multiple Key Presses
Although the BU97600FV-M/BU97600FUV-M is capable of key scanning without inserting diodes for dual key presses, triple key presses on the KI1 to KI4 input pin lines, or multiple key presses on the KS1 to KS5 output pin lines, multiple presses other than these cases may result in keys that were not pressed recognized as having been pressed. Therefore, a diode must be inserted in series with each key. Applications that do not recognize multiple key presses of three or more keys should check the key data for three or more 1 bit and ignore such data.

Controller Key Data Read Technique

When the controller receives a key data read request from BU97600FV-M/BU97600FUV-M, it performs a key data read acquisition operation
using either the Timer Based Key Data Acquisition or the Interrupt Based Key Data Acquisition.

Timer Based Key Data Acquisition Technique

Under the Timer Based Key Data Acquisition Technique, the controller uses a timer to determine the states of the keys (ON or OFF) and read the key data. Please refer to the flowchart below.



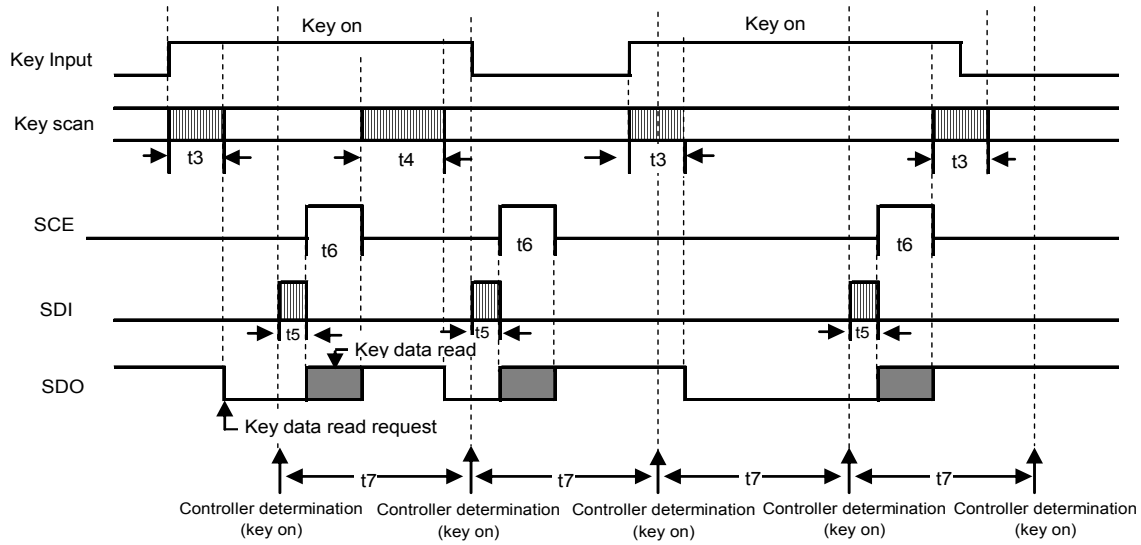
Key data read processing: Refer to “Serial Data Output”

Figure 22. Flowchart

In this technique, the controller uses a timer to determine key on/off states and read the key data. The controller must check the SDO state when SCE is low every t7 period without fail. If SDO is low, the controller recognizes that a key has been pressed and executes the key data read operation.

The period t7 in this technique must satisfy the following condition.
T7>t4+t5+t6

If a key data read operation is executed when SDO is high, the read key data (KD1 to KD20) and sleep acknowledge data (SA) will be invalid.

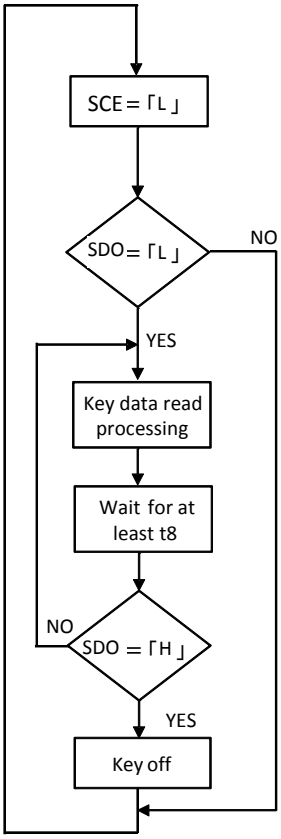


t3: Key scan execution time when the key data agreed for two key scans. (9904T(s))
t4: Key scan execution time when the key data did not agree for two key scans and the key scan was executed again. (19808T(s)) T = 1 / fosc
t5: Key address (43H) transfer time
t6: Key data read time

Figure 23. Timer based key data read operation

Interrupt Based Key Data Acquisition Technique

Under the Interrupt Based Key Data Acquisition Technique, the controller uses interrupts to determine the state of the keys (ON or OFF) and read the key data. Please refer to the flow chart diagram below.

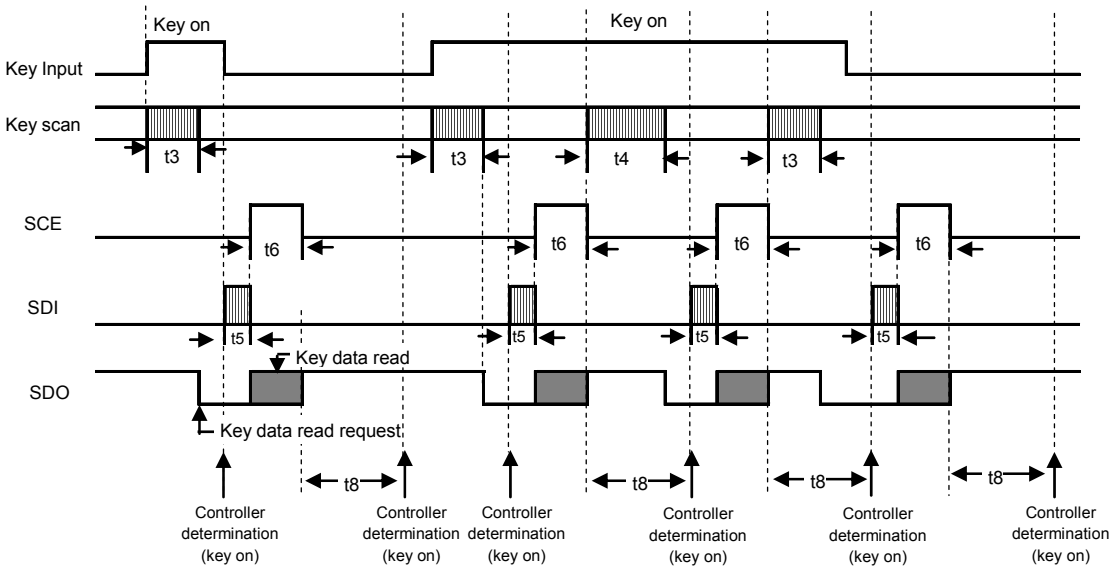


Key data read processing: Refer to “Serial Data Output”

Figure 24. Flowchart

In this technique, the controller uses interrupts to determine key on/off states and read the key data. The controller must check the SDO state when SCE is low. If SDO is low, the controller recognizes that a key has been pressed and executes the key data read operation. After that the next key on/off determination is performed after the time t8 has elapsed by checking the SDO state when SCE is low and reading the key data. The period t8 in this technique must satisfy t8 > t4.

If a key data read operation is executed when SDO is high, the read key data (KD1 to KD20) and sleep acknowledge data (SA) will be invalid.



t3: Key scan execution time when the key data agreed for two key scans. (9904T(s))
t4: Key scan execution time when the key data did not agree for two key scans and the key scan was executed again. (19808T(s)) T = 1 / fosc
t5: Key address (43H) transfer time
t6: Key data read time

Figure 25. Interrupt Based Key Data Read Operation

Output Waveform (Line Inversion 1/4 Duty 1/3 Bias Drive Scheme)

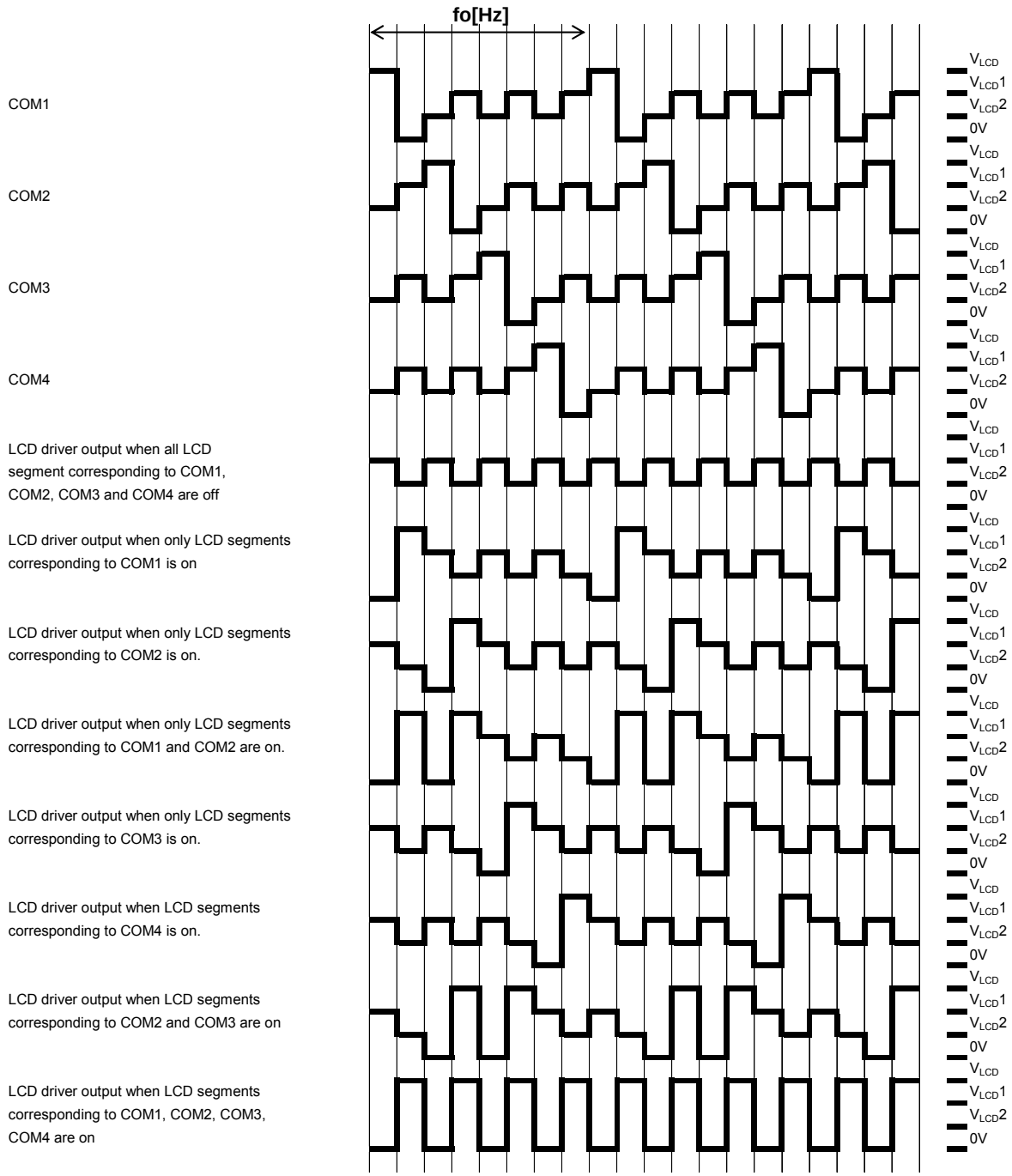


Figure 26. LCD Waveform (Line Inversion, 1/4 DUTY, 1/3 BIAS)

Output Waveform (Line Inversion 1/4 Duty 1/2 Bias Drive Scheme)

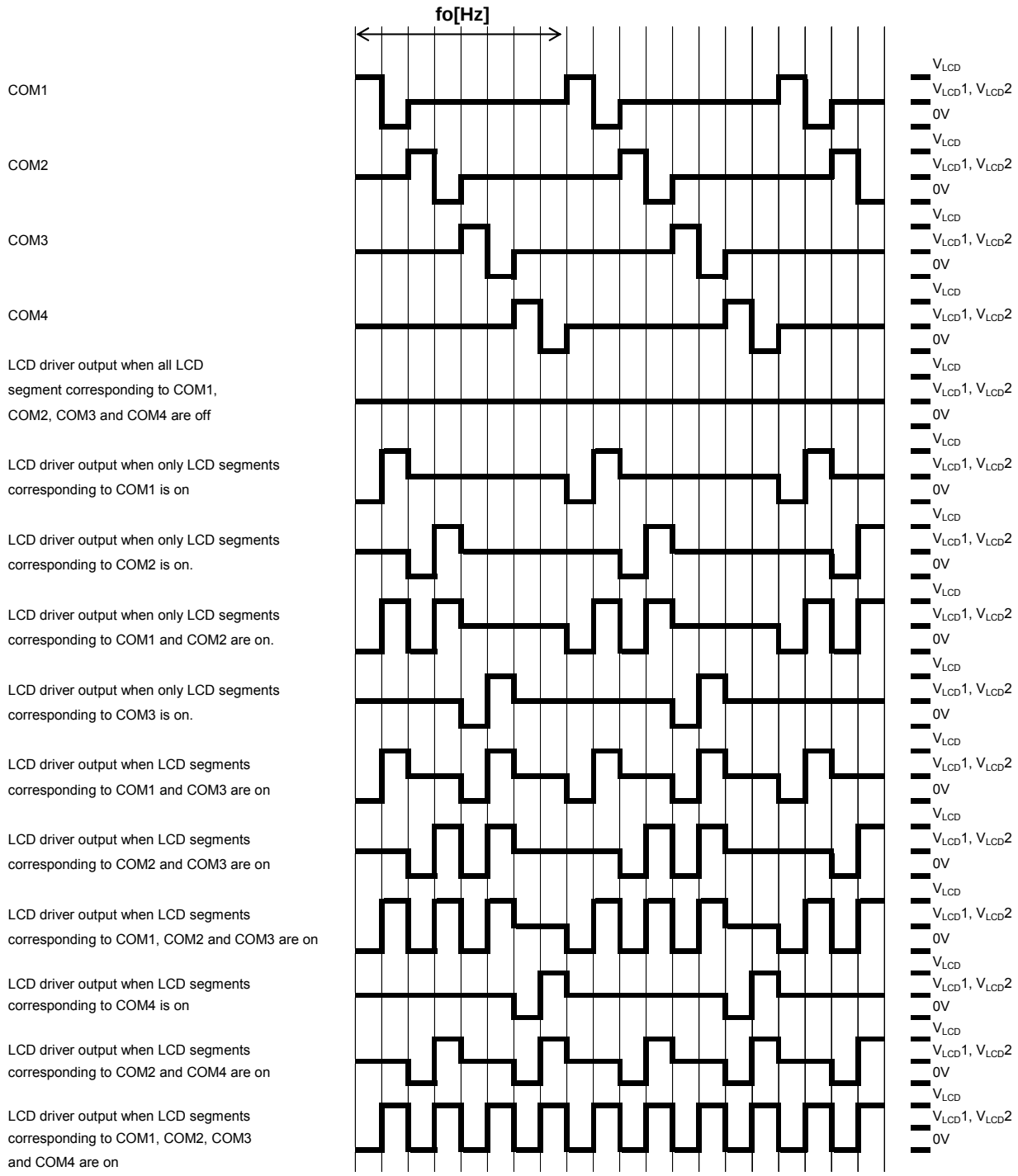


Figure 27. LCD Waveform (Line Inversion, 1/4 DUTY, 1/2 BIAS)

Output Waveform (Line Inversion 1/3 Duty 1/3 Bias Drive Scheme)

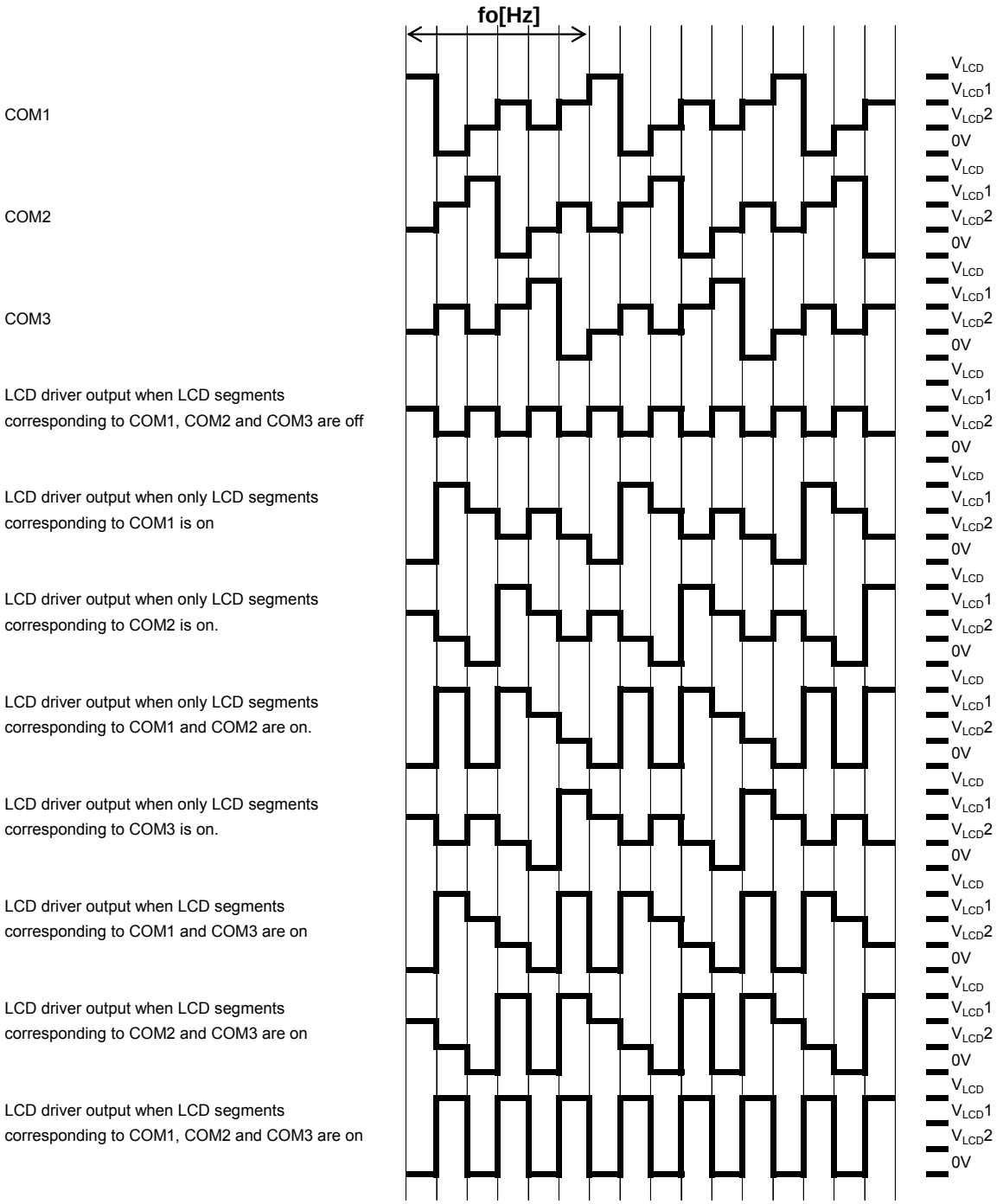


Figure 28. LCD Waveform (Line Inversion, 1/3 DUTY, 1/3 BIAS) (Note24)

(Note24) COM4 function is same as COM1 at 1/3 duty.

Output Waveform (Line Inversion 1/3 Duty 1/2 Bias Drive Scheme)

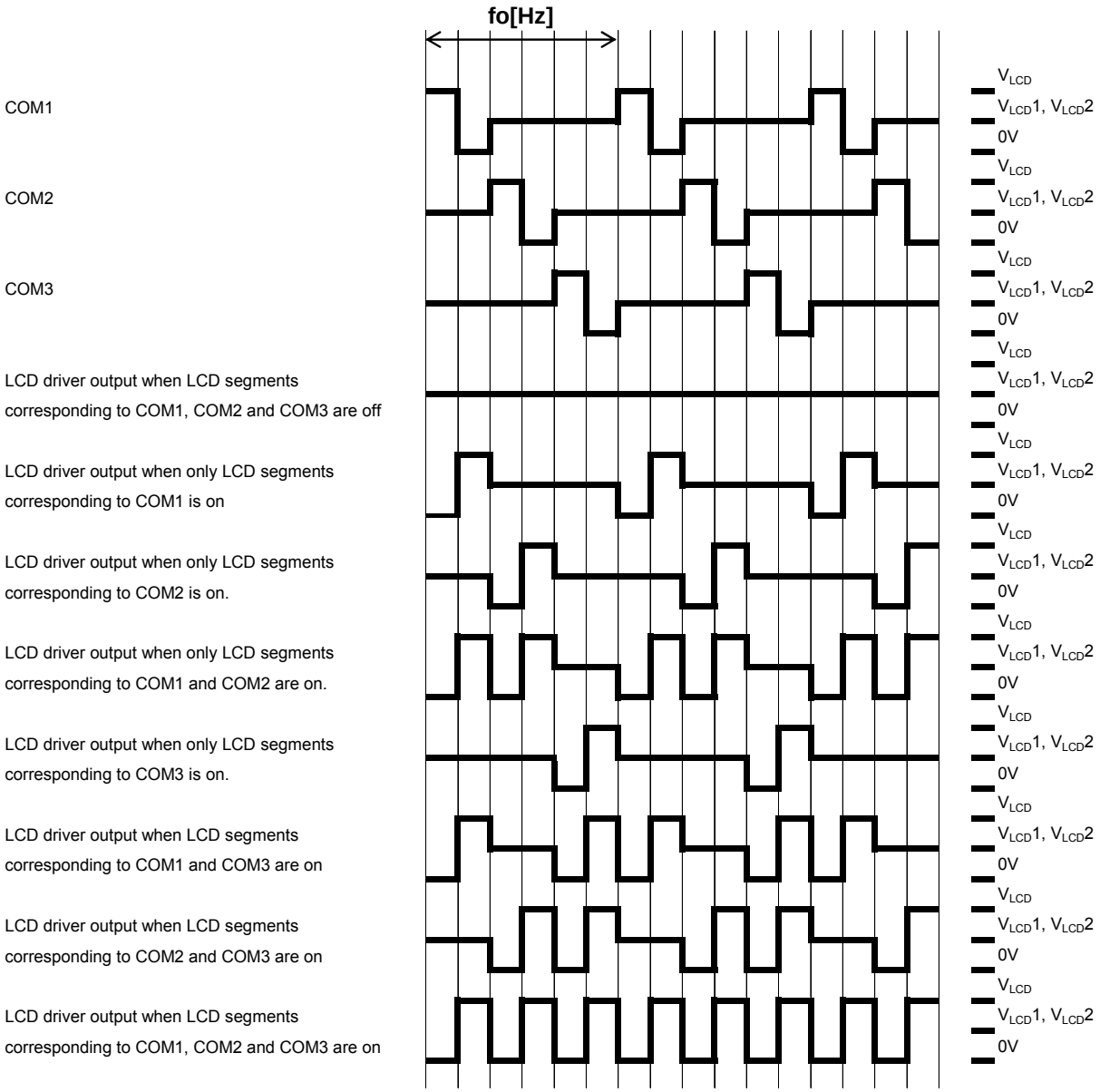


Figure 29. LCD Waveform (Line Inversion, 1/3 DUTY, 1/2BIAS) (Note25)

(Note25) COM4 function is same as COM1 at 1/3 duty.

Output Waveform (Line Inversion 1/2 Duty 1/3 Bias Drive Scheme)

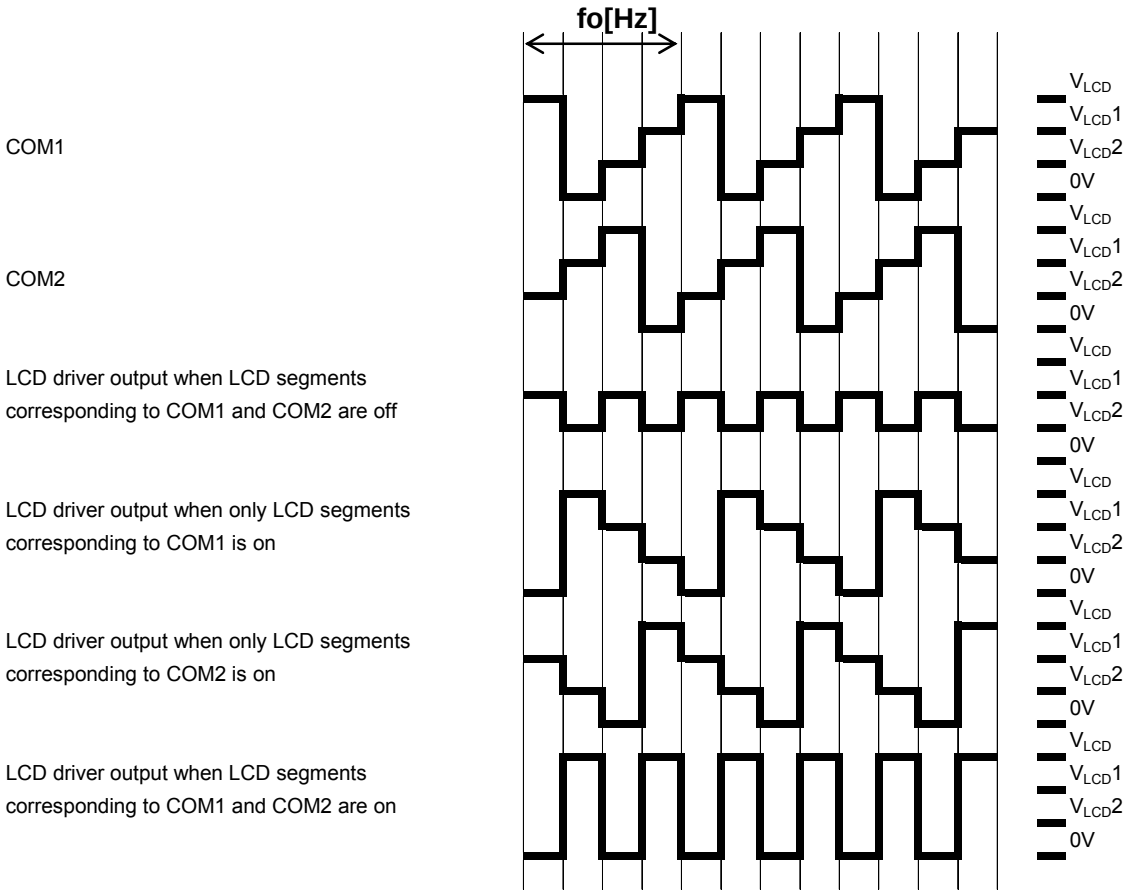


Figure 30. LCD Waveform (Line Inversion, 1/2 DUTY, 1/3 BIAS) (Note26)

(Note26) COM3 function is same as COM1 at 1/2 duty. COM4 function is same as COM2 at 1/2 duty.

Output Waveform (Line Inversion 1/2 Duty 1/2 Bias Drive Scheme)

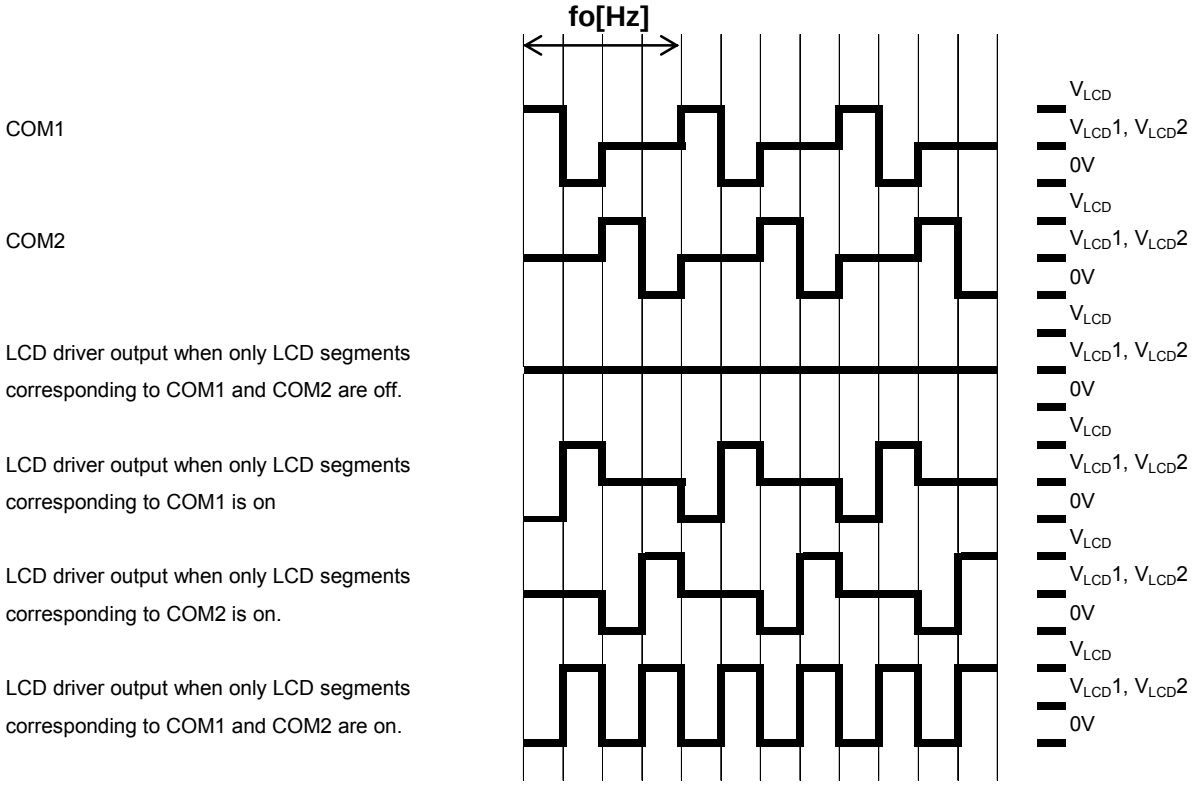


Figure 31. LCD Waveform (Line Inversion, 1/2 DUTY, 1/2BIAS) (Note27)

(Note27) COM3 function is same as COM1 at 1/2 duty. COM4 function is same as COM2 at 1/2 duty.

Output Waveform (Line Inversion 1/1 Duty [Static] Drive Scheme)

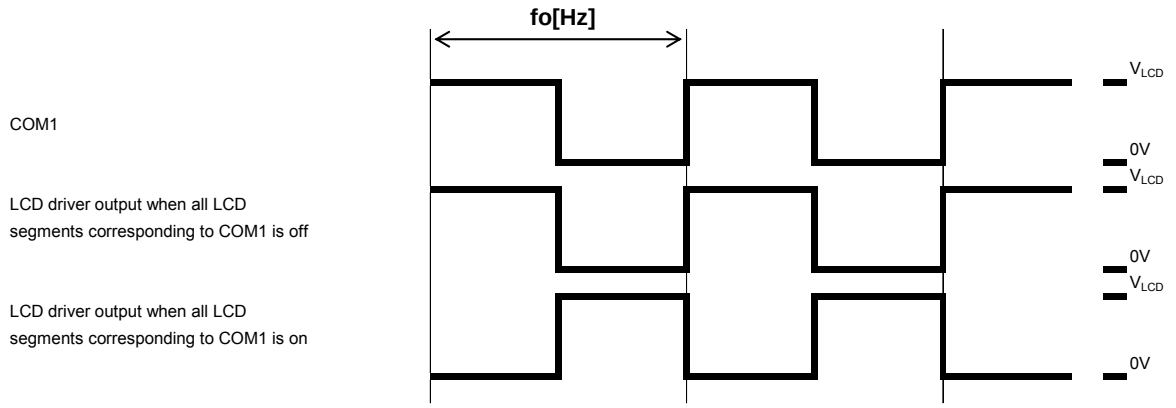


Figure 32. LCD Waveform (Line Inversion, 1/1 DUTY) (Note28)

(Note28) COM2, COM3 and COM4 function are same as COM1 at 1/1 duty.

Output Waveform (Frame Inversion 1/4 Duty 1/3 Bias Drive Scheme)

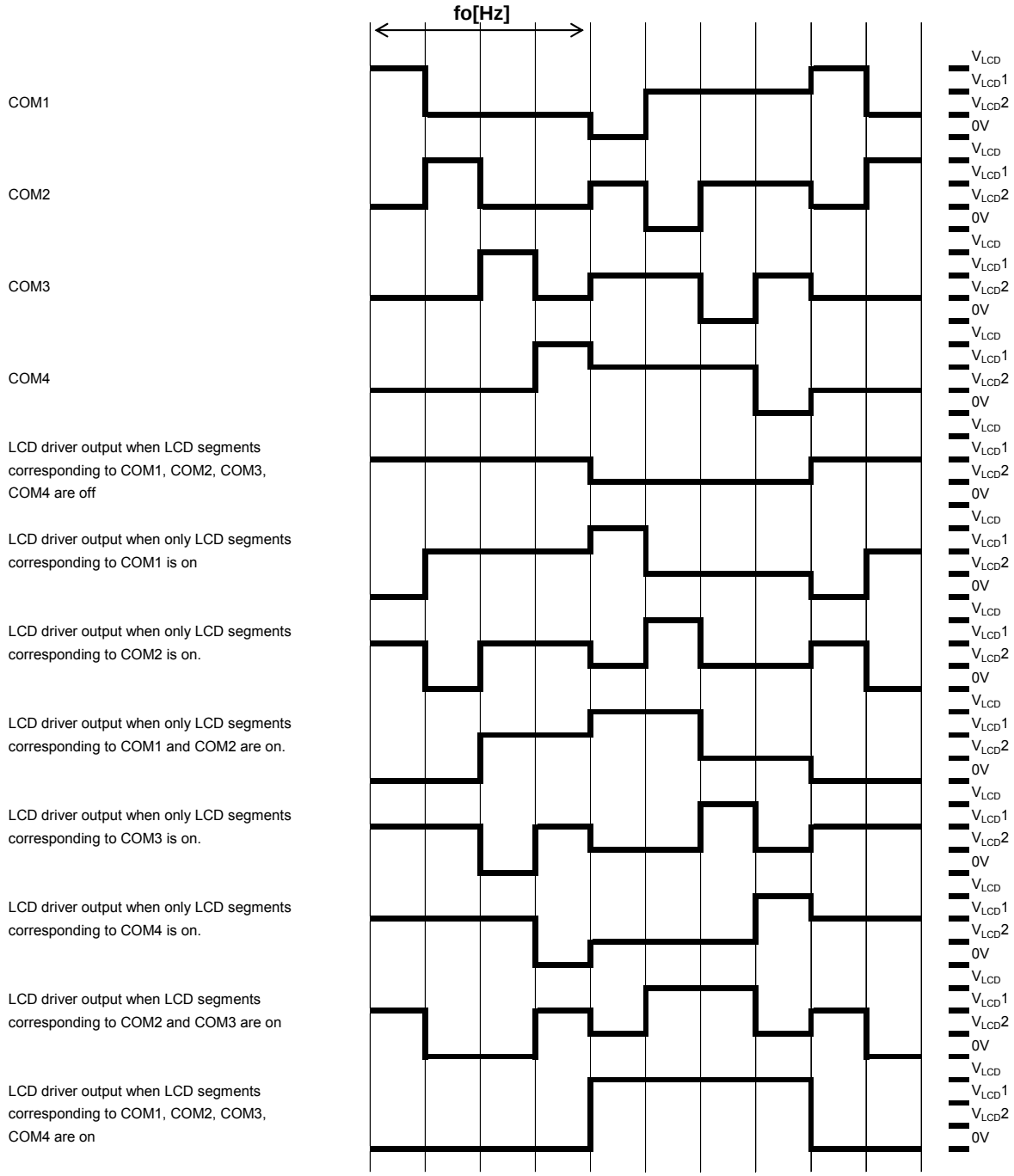


Figure 33. LCD Waveform (Frame Inversion, 1/4 DUTY, 1/3BIAS)

Output Waveform (Frame Inversion 1/4 Duty 1/2 Bias Drive Scheme)

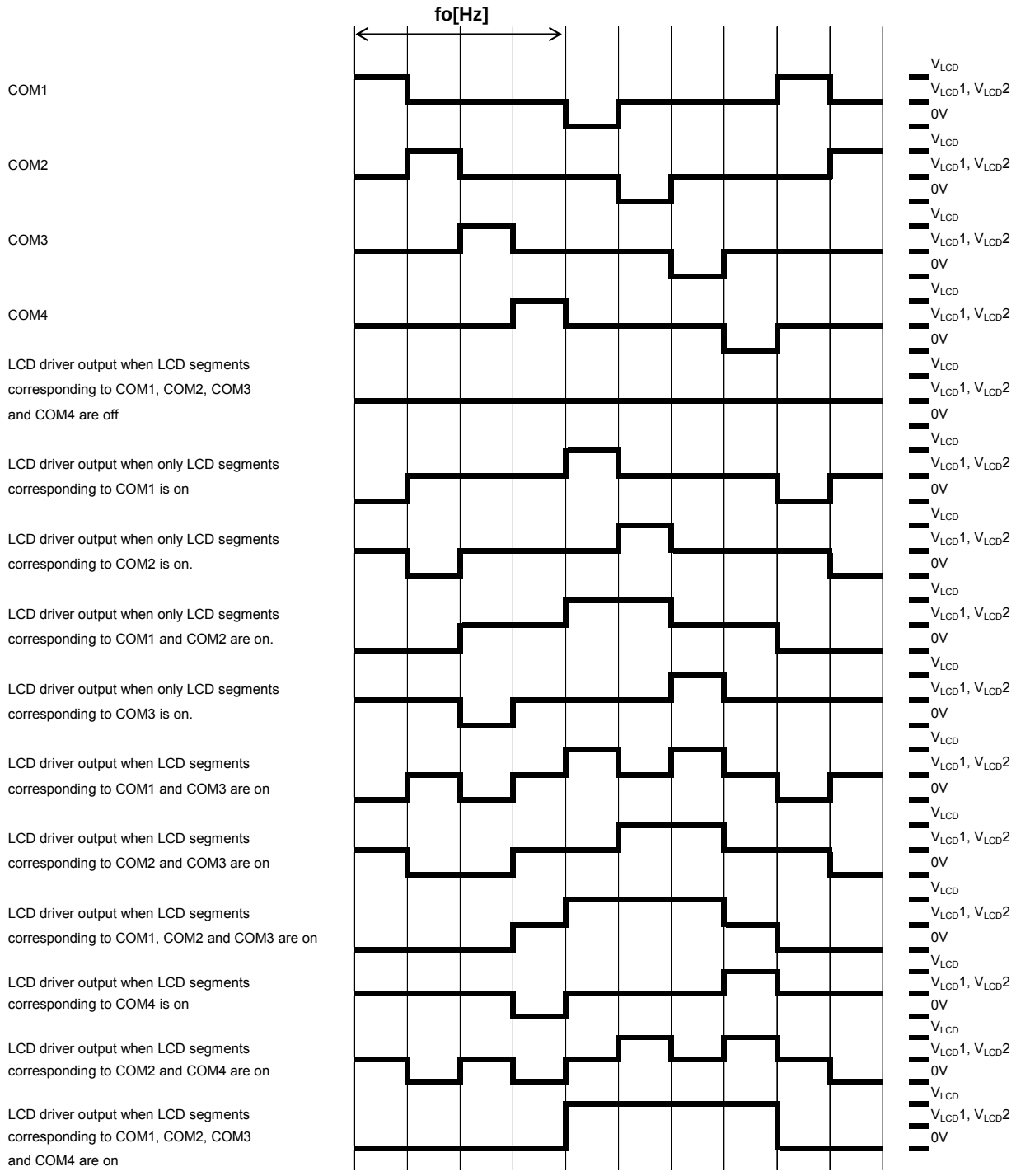


Figure 34. LCD Waveform (Frame Inversion, 1/4 DUTY, 1/2BIAS)

Output Waveform (Frame Inversion 1/3 Duty 1/3 Bias Drive Scheme)

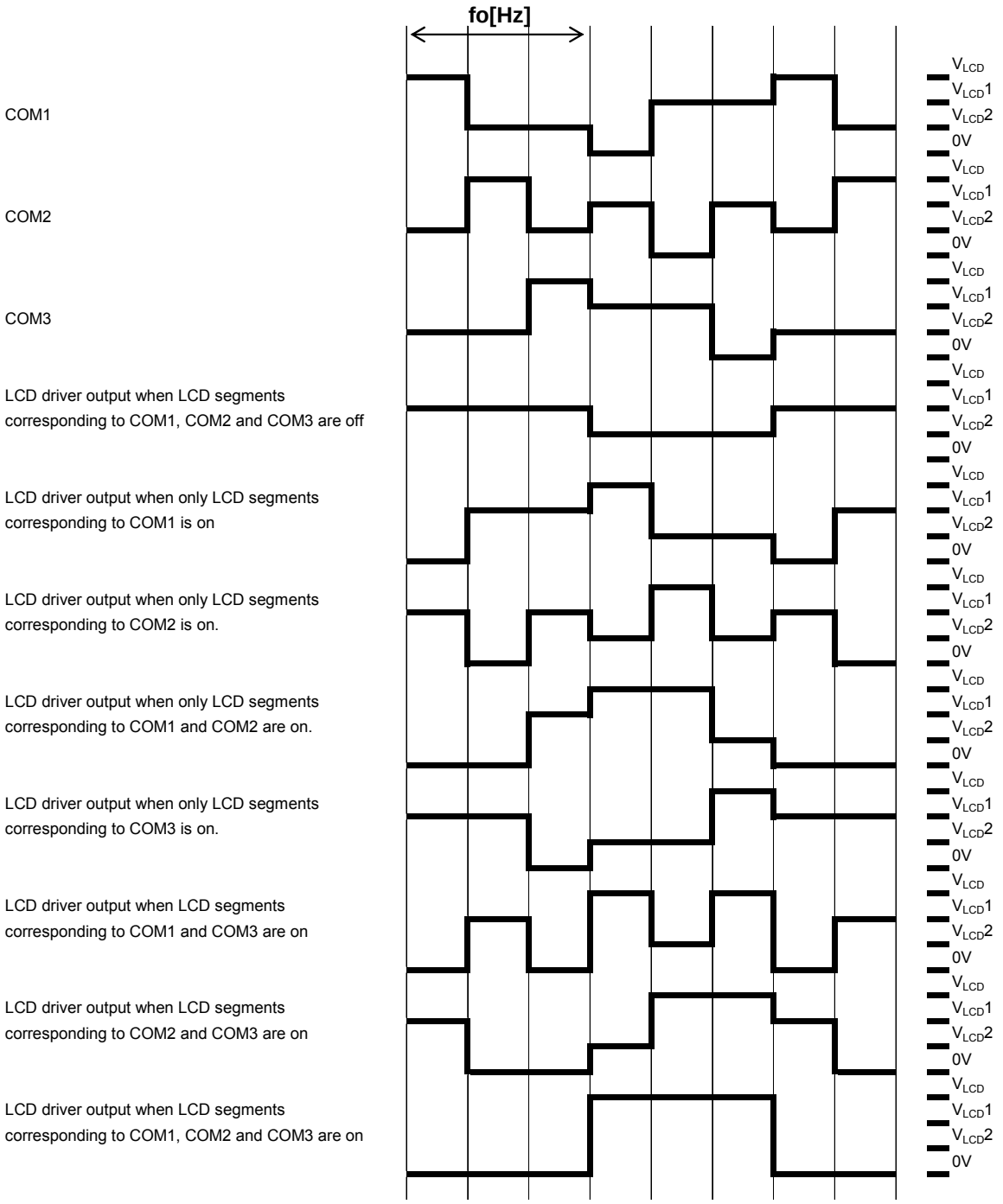


Figure 35. LCD Waveform (Frame Inversion, 1/3 DUTY, 1/3BIAS) (Note29)

(Note29) COM4 function is same as COM1 at 1/3 duty.

Output Waveform (Frame Inversion 1/3 Duty 1/2 Bias Drive Scheme)

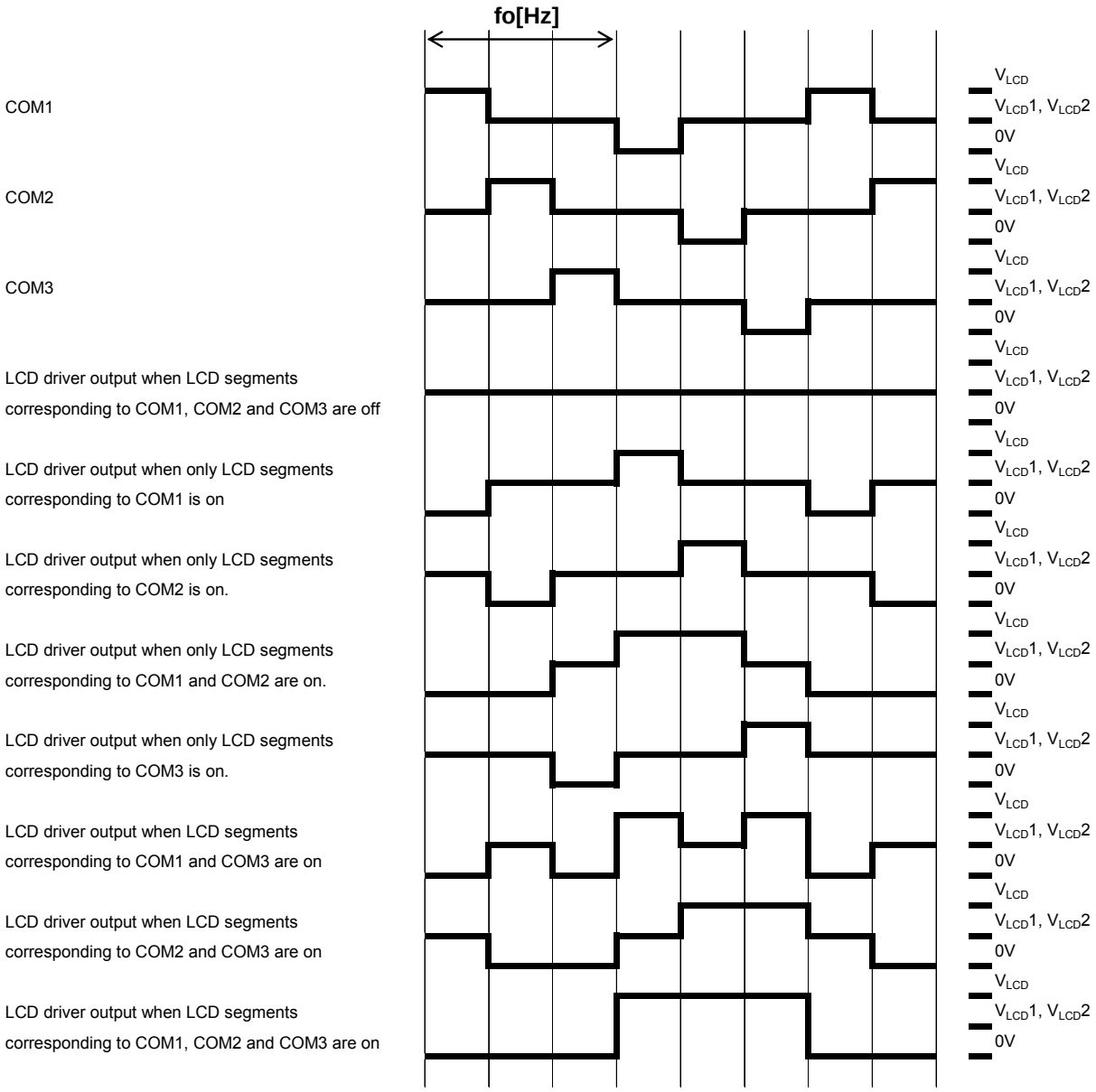


Figure 36. LCD Waveform (Frame Inversion, 1/3 DUTY, 1/2 BIAS) (Note30)

(Note30) COM4 function is same as COM1 at 1/3 duty.

Output Waveform (Frame Inversion 1/2 Duty 1/3 Bias Drive Scheme)

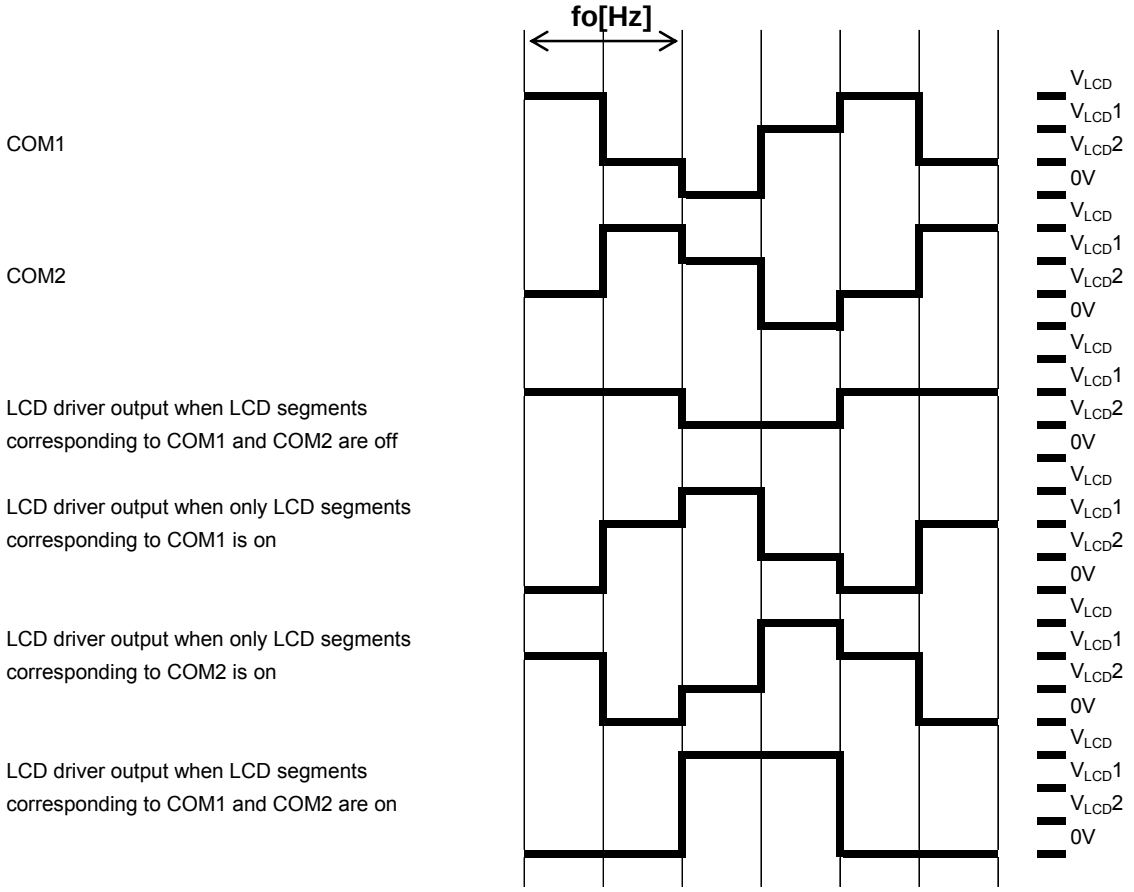


Figure 37. LCD Waveform (Frame Inversion, 1/2 DUTY, 1/3BIAS) (Note31)

(Note31) COM3 function is same as COM1 at 1/2 duty. COM4 function is same as COM2 at 1/2 duty.

Output Waveform (Frame Inversion 1/2 Duty 1/2 Bias Drive Scheme)

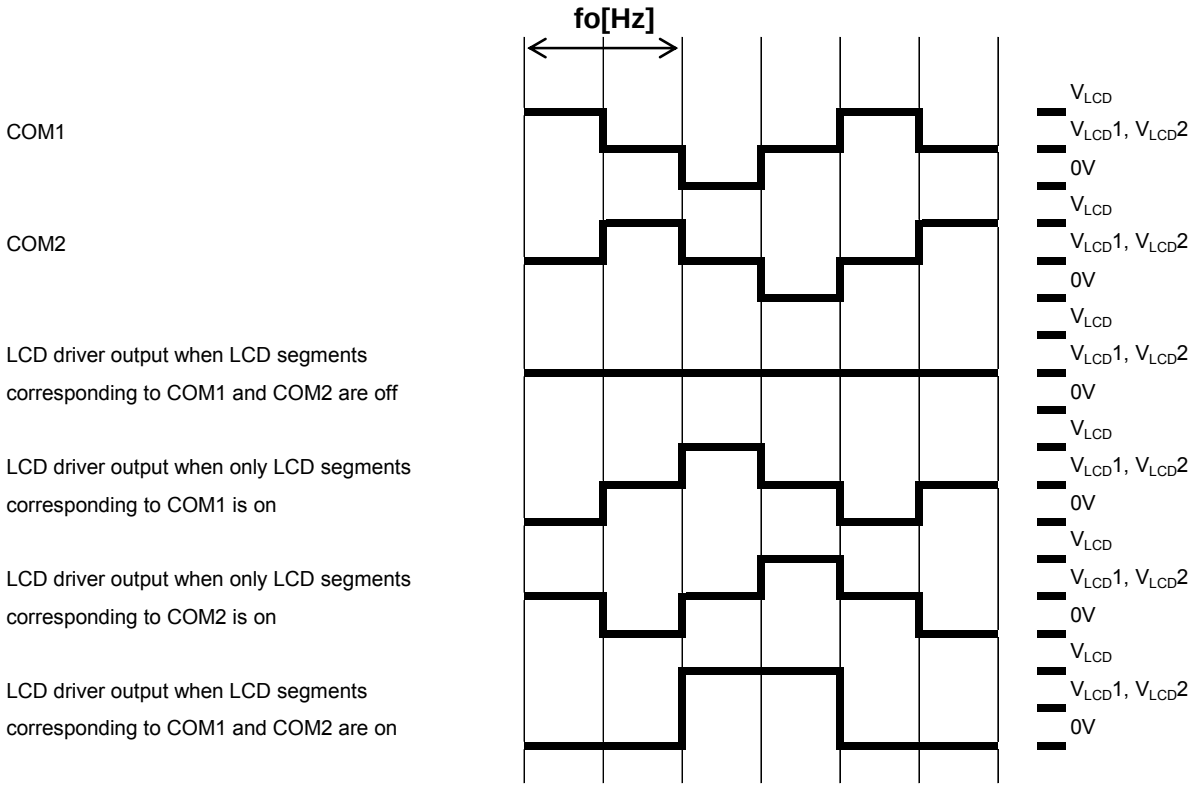


Figure 38. LCD Waveform (Frame Inversion, 1/2 DUTY, 1/2 BIAS) (Note32)

(Note32) COM3 function is same as COM1 at 1/2 duty. COM4 function is same as COM2 at 1/2 duty.

Output Waveform (Frame Inversion 1/1 Duty [Static] Drive Scheme)

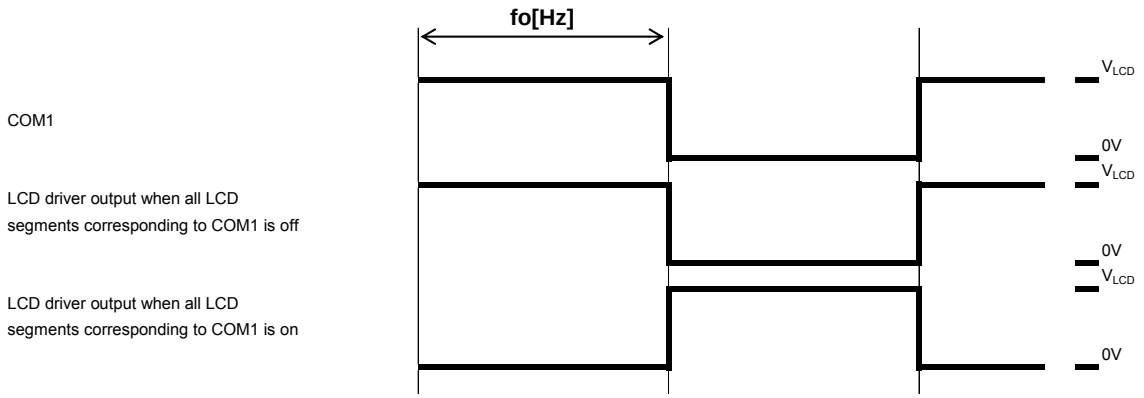


Figure 39. LCD Waveform (Frame Inversion, 1/1 DUTY) (Note33)

(Note33) COM2, COM3 and COM4 function are same as COM1 at 1/1 duty.

INHb Pin and Display Control

Since the IC internal data (1/4-Duty: the display data D1 to D148 and the control data, 1/3-Duty: the display data D1 to D111 and the control data, 1/2-Duty: the display data D1 to D74 and the control data, 1/1-Duty: the display data D1 to D37 and the control data) is undefined when power is first applied, applications should set the INHb pin low at the same time as power is applied to turn off the display (This sets the S1 to S37, COM1 to COM4 to the VSS level.) and during this period send serial data from the controller. The controller should then set the INHb pin high after the data transfer has completed. This procedure prevents meaningless displays at power on.

1. 1/4-Duty

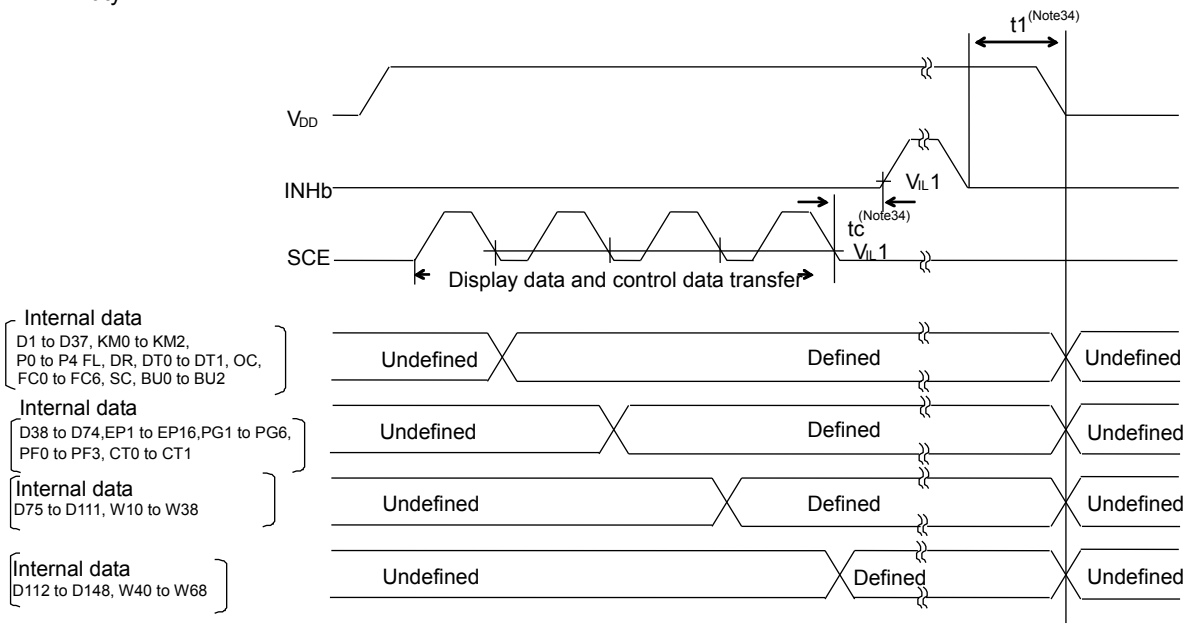


Figure 40. Power ON/OFF and INHb Control Sequence (1/4-Duty)

(Note34) t1≥0, tc: min 10us

2. 1/3-Duty

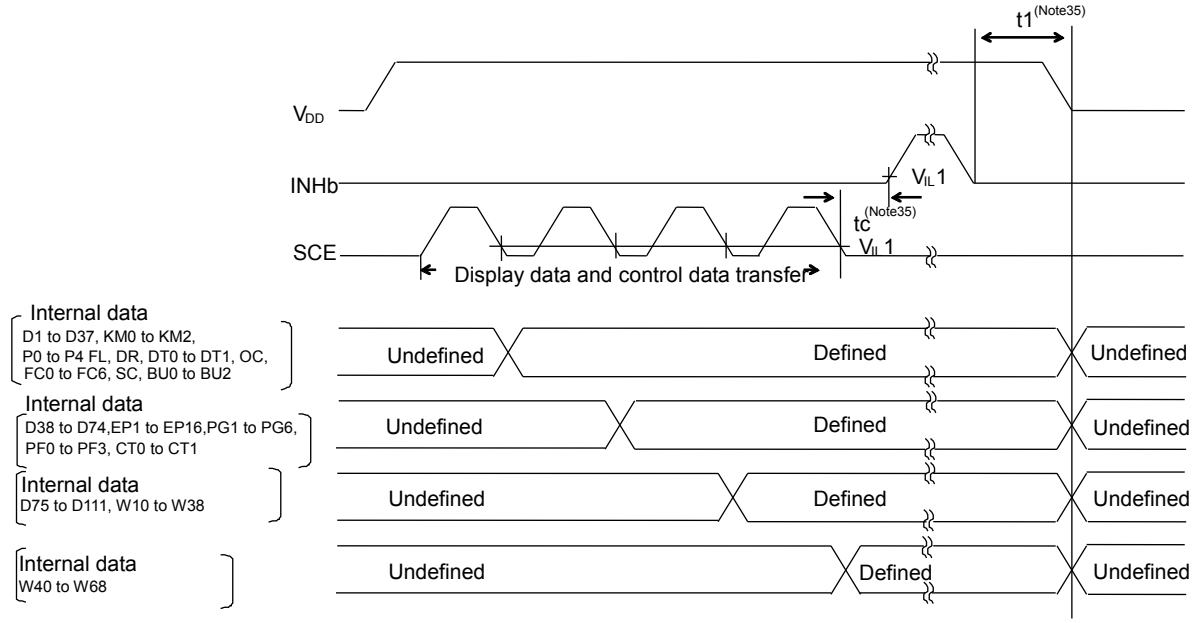


Figure 41. Power ON/OFF and INHb Control Sequence (1/3-Duty)

(Note35) t1≥0, tc: min 10us

3. 1/2-Duty

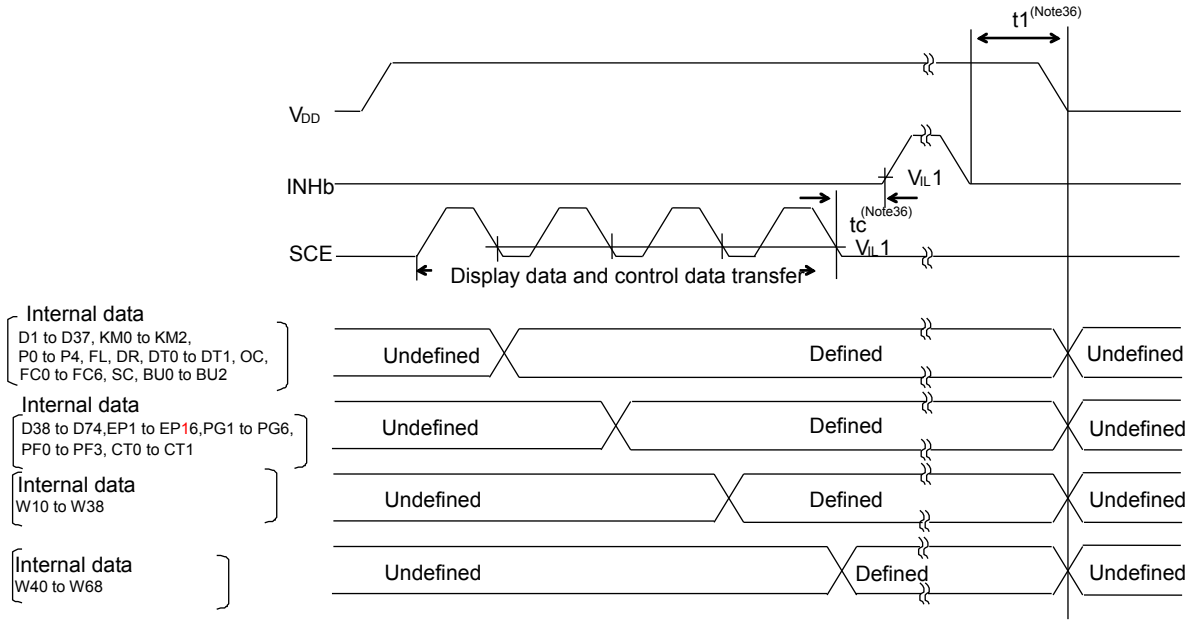


Figure 42. Power ON/OFF and INHb Control Sequence (1/2-Duty)

(Note36) t1≥0, tc: min 10us

4. 1/1-Duty

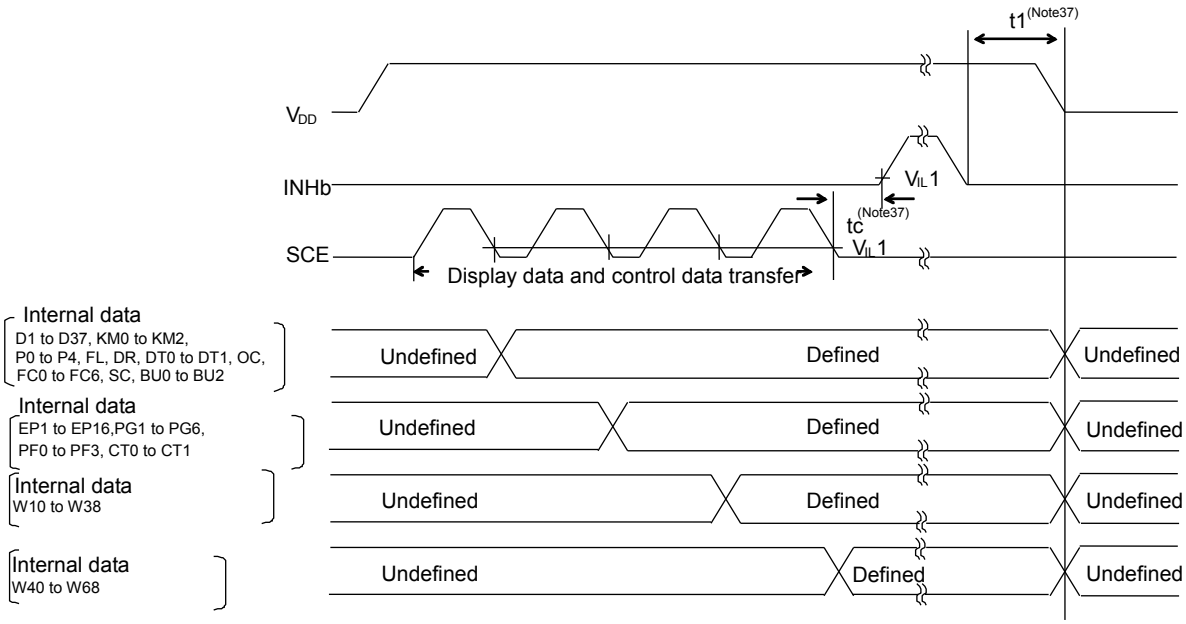


Figure 43. Power ON/OFF and INHb Control Sequence (1/1-Duty)

(Note37) t1≥0, tc: min 10us

Oscillation Stabilization Time

It must be noted that the oscillation of the internal oscillation circuit is unstable for a maximum of 100μs (oscillation stabilization time) after oscillation has started.

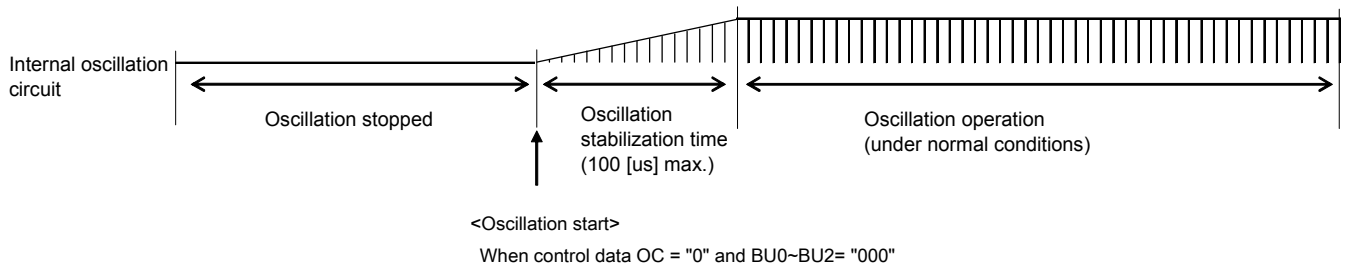


Figure 44. Oscillation Stabilization Time

Voltage Detection Type Reset Circuit (VDET)

The Voltage Detection Type Reset Circuit generates an output signal that resets the system when power is applied for the first time and when the power supply voltage drops (that is, for example, the power supply voltage is less than or equal to the power down detection voltage (VDET = 1.8V typ.). To ensure that this reset function works properly, it is recommended that a capacitor be connected to the power supply line so that both the power supply voltage (VDD) rise time when power is first applied and the power supply voltage (VDD) fall time when the voltage drops are at least 1ms.

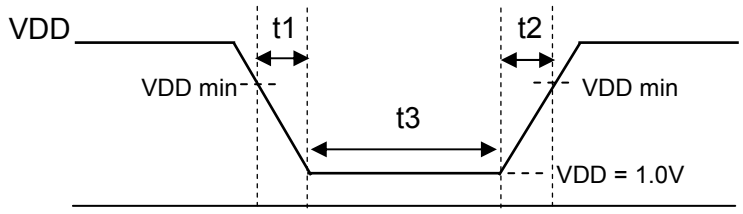


Figure 45. VDET Detection Timing

Power supply voltage VDD rise time: t1 > 1ms
Power supply voltage VDD fall time: t2 > 1ms
Internal reset power supply retain time: t3 > 1ms

RESET CONDITION

When BU97600FV-M and BU97600FUV-M are initialized, the internal status after power supply has been reset as the following table.

Instruction	At Reset Condition
Key Scan mode	[KM0,KM1,KM2]=[1,1,1]:Keyscan no use
S5/P1/G1 to S20/P16/G16 pin	[P0,P1,P2,P3,P4]=[0,0,0,0,0]:all segment output
Inversion mode	FL=0:Line Inversion
LCD bias	DR=0:1/3 bias
LCD duty	[DT0,DT1]=[1,1]:1/4 duty
DISPLAY frequency	[FC0,FC1,FC2,FC3,FC4,FC5,FC6]=[0,0,0,0,0,0,0]:fosc/12000
Display clock mode	OC=0:Internal oscillator
LCD display	SC=1:OFF
Power mode	[BU0, BU1, BU2]=[1,1,1]:Power saving mode
PWM/GPO output	PGx=0:PWM output(x=1～6)
External PWM	[EP1,EP2,EP3,EP4,EP5,EP6,EP7,EP8,EP9,EP10,EP11,EP12,EP13,EP14,EP16] =[0,0,0,0,0,0,0,0,0,0,0,0,0,0,0]: External PWM OFF
PWM frequency	[PF0,PF1,PF2,PF3]=[0,0,0,0]: fosc /4096
PWM duty	[Wn0～Wn8]=[0,0,0,0,0,0,0,0,0]:0/256)xTp (n=1～6,Tp=1/fp)
Display Contrast setting	[CT0,CT1,CT2,CT3]=[0,0,0,0]:VLCD Level is 1.00*VDD

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

13. Data transmission

To refrain from data transmission is strongly recommended while power supply is rising up or falling down to prevent from the occurrence of disturbances on transmission and reception.

Ordering Information

B U 9 7 6 0 0 x x x - ME 2

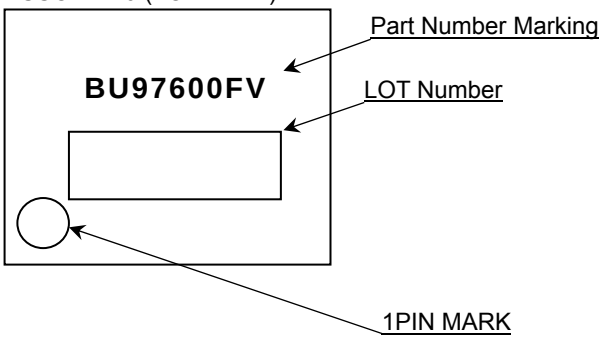
Part Number

Package
FV : SSOP-B40
FUV : TSSOP-C48V

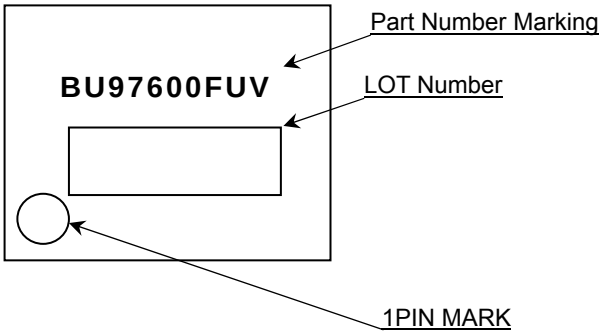
Product Rank
M: for Automotive
Packaging Specification
E2: Embossed tape and reel
(SSOP-B40 / TSSOP-C48V)

Marking Diagram

SSOP-B40 (TOP VIEW)

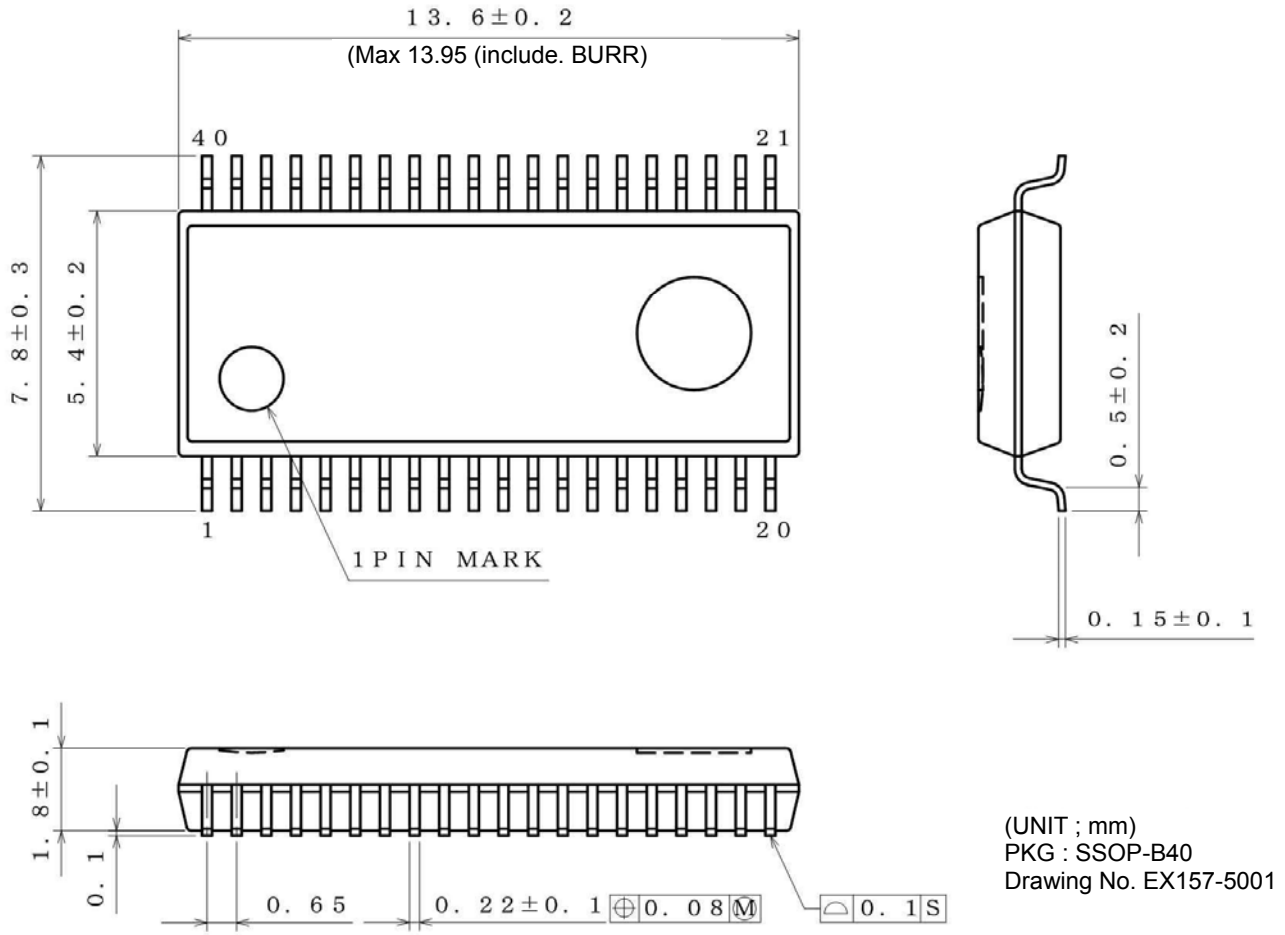


TSSOP-C48V(TOP VIEW)



Physical Dimension, Tape and Reel Information

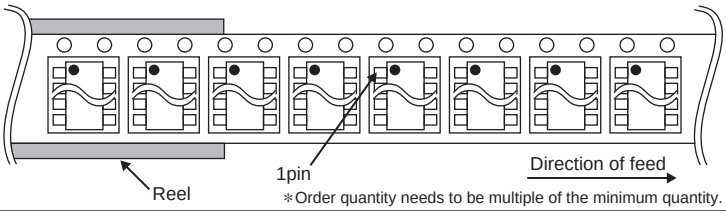
Package Name	SSOP-B40



(UNIT ; mm)
PKG : SSOP-B40
Drawing No. EX157-5001

<Tape and Reel information>

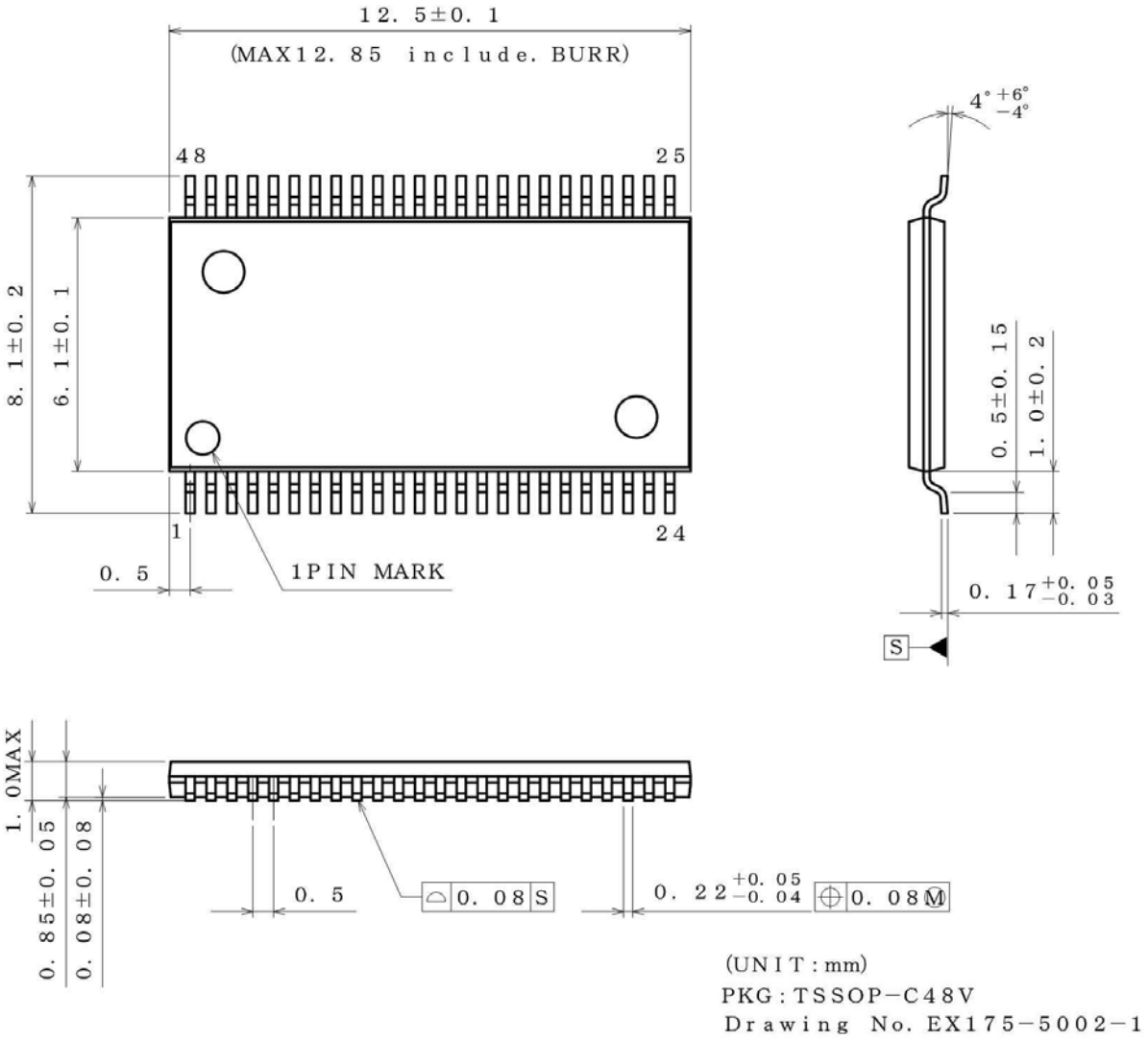
Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

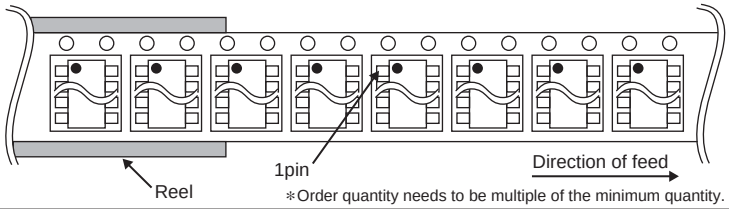
Physical Dimension, Tape and Reel Information

Package Name	TSSOP-C48V



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Version / Revision History

Version	date	description
001	05. Feb. 2015	New Release
002	02. Apr. 2015	Modify INHb Handling when unused of Pin Description in page 7 and page 8.

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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