

Enhanced Multi-touch Capacitive Touch Screen Controller AUR3852

General Description

The AUR3852 is a low-cost high-resolution single chip solution for APA capacitive touch screen. It is an 8-bit single cycle 8051 microcontroller with ICP Interface. The chip includes a 12-bit successive approximation analog-to-digital converter with an I²C interface and multiplexer-switcher circuits for flexible measurement of analog signal from APA panel. An accurate switched-capacitor integrator is built-in and it can auto calibrate the pixel parameters for a wide range of capacitance on the touch screen (0.1pF to 4pF). On-chip capacitor can replace external component. This touch screen controller (TSC) with CMOS integration circuit provides an ideal choice for APA touch panel. The AUR3852 is specified over the temperature range of -40°C to 85°C.

The AUR3852 is available in QFN-6×6-48 and QFN-7×7-56 packages.

Features

- Mutual Capacitive Touch Sensing
- Single Power Supply: 2.8V to 3.6V Operation Voltage
- Supports Low Voltage to 1.8V by Built-in 1.8V to 3.3V Boost Converter
- QFN-6×6-48 Package: Up to 20 Drive Lines and 14 Sense Lines
- QFN-7×7-56 Package: Up to 27 Drive Lines and 15 Sense Lines
- Dedicated Internal Two-wire Serial Control Bus I²C and UART between AUR3852 and Host
- Single-end Integrator with Programmable Gain Control and Offset Control
- Multiplexed Analog Digitization with 12-bit Resolution SAR ADC

Features (Continued)

- Single Cycle 8051 CPU Core, Maximum Operating Clock up to 24MHz from IOSC
2MHz to 24MHz Internal Oscillator (IOSC)
32K-byte Flash ROM
256-byte Internal SRAM and 5888-byte XSRAM
Two 16-bit Timers T0/T1 and One 16-bit ECT Timer T2
One I²C Slave Controller and One I²C Master Controller Shared with the Same Port
 - ◆ With Asynchronous I²C Slave Address Detection Logic Design
- Up to 30 General Purpose GPIO Pins (QFN-56); 25 General Purpose GPIO Pins (QFN-48)
Up to 8 External Interrupt Pins
Up to 2 UART Ports (QFN-56); 1 UART Port (QFN-48)
- ISP/IAP via I²C/UART Port
(With External Clock I/O Pin Definition for UART IAP. Pin Shared with P1.7)
- Operation Temperature Range: -40°C to 85°C
- Package Type: QFN-6×6-48 and QFN-7×7-56
- RoHS Compliance
- Operating Mode:

Mode	Description
Power-down	No scan with power-down mode
Low speed	Lower scan rate when finger is not on panel, IOSC=32kHz
Standard	Higher scan rate when fingers are on panel, IOSC can up to 2MHz to 24MHz

Applications

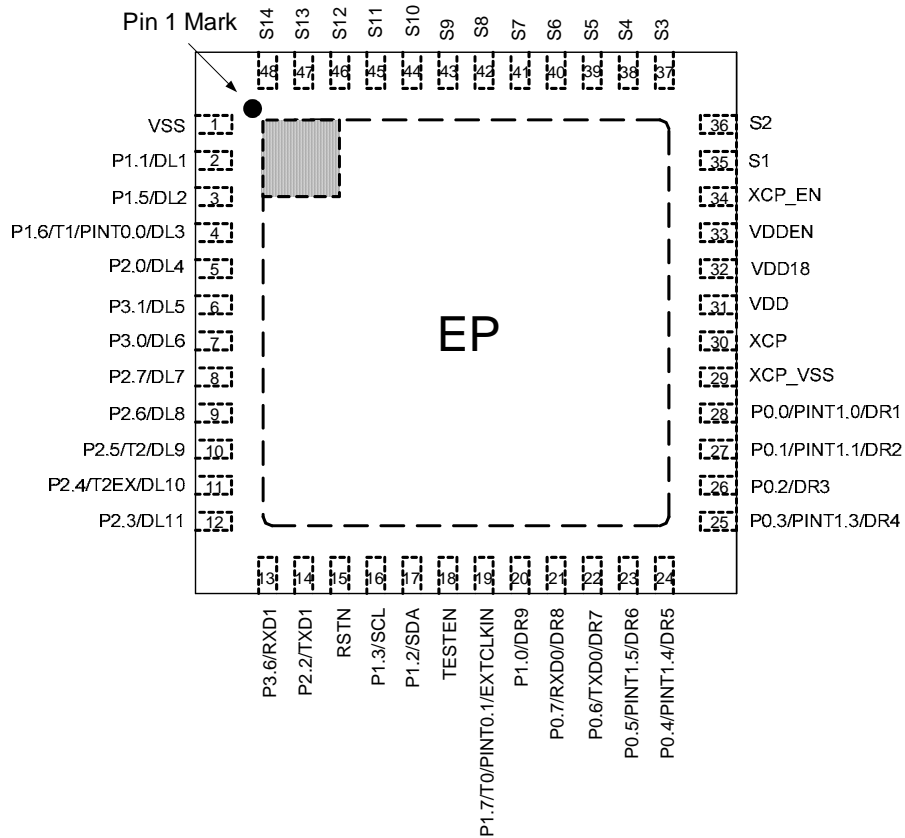
- Mobile Phones
- Personal Digital Assistants
- Smart Hand-held or Gaming Devices



Figure 1. Package Types of AUR3852

Pin Configuration

QT Package
(QFN-6x6-48)



Pin Configuration (Continued)

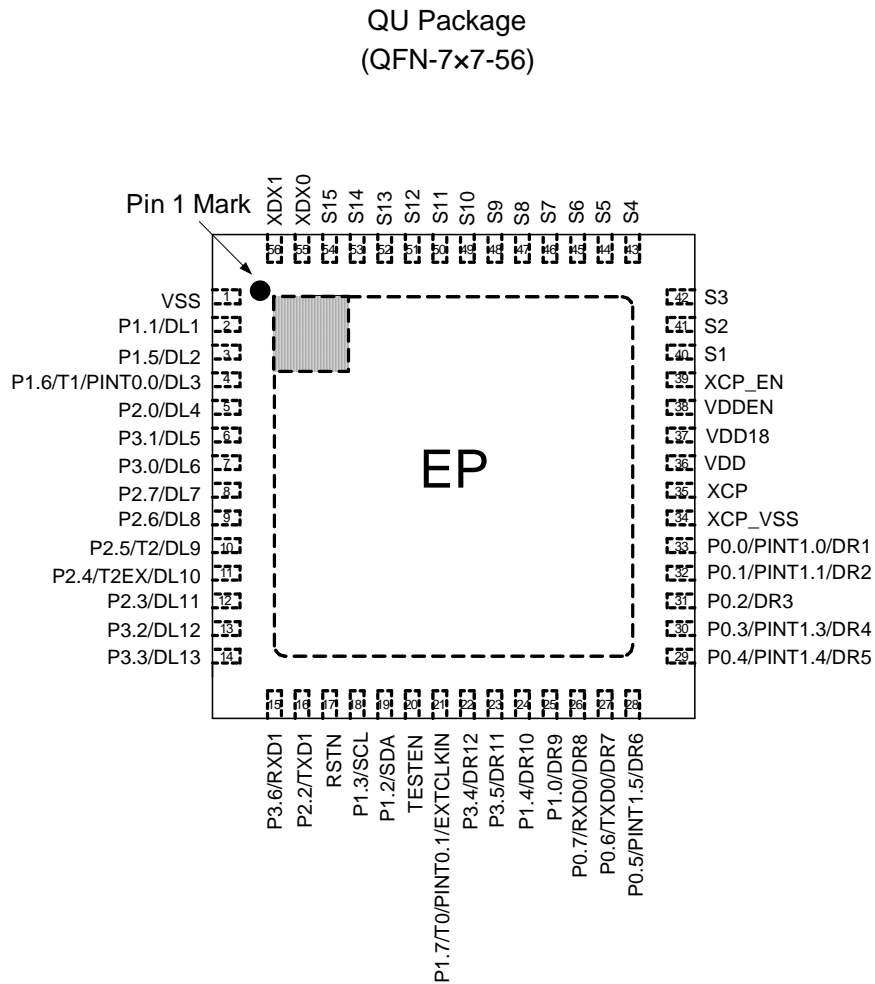


Figure 2. Pin Configuration of AUR3852 (Top View)

**Pin Description**

Pin Number		Pin Name	Pin Type	Pin Function
QFN-6×6-48	QFN-7×7-56			
1	1	VSS	Power	Ground Voltage. 0V
2	2	P1.1	I/O	Port 1.1 GPIO
				8051 P1.1 GPIO
				DL1 Left driving line 1
3	3	P1.5	I/O	Port 1.5 GPIO
				8051 P1.5 GPIO
				DL2 Left driving line 2
4	4	P1.6	I/O	Port 1.6 GPIO
				8051 P1.6 GPIO
				PINT0.0 This pin can also be configured as the expanded INTO interrupt
				T1 Timer 1 Input This pin can also be configured as Timer 1 input
				DL3 Left driving line 3
5	5	P2.0	I/O	Port 2.0 GPIO
				8051 P2.0 GPIO. To allow proper operation as GPIO P2.0 function, crystal oscillator must be disabled by setting XOSCCFG register to 0x00
				DL4 Left driving line 4
6	6	P3.1	I/O	Port 3.1 GPIO
				8051 P3.1 GPIO
				DL5 Left driving line 5
7	7	P3.0	I/O, A	Port 3.0 GPIO
				8051 P3.0 GPIO
				DL6 Left driving line 6



Pin Description (Continued)

Pin Number		Pin Name	Pin Type	Pin Function
QFN-6x6-48	QFN-7x7-56			
8	8	P2.7	I/O	Port 2.7 GPIO
				8051 P2.7 GPIO
				DL7
				Left driving line 7
9	9	P2.6	I/O	Port 2.6 GPIO
				8051 P2.6 GPIO
				DL8
				Left driving line 8
10	10	P2.5	I/O	Port 2.5 GPIO
				8051 P2.5 GPIO
				T2 Timer 2 Input
				This pin can also be configured as Timer 2 input
				DL9
11	11	P2.4	I/O	Port 2.4 GPIO
				8051 P2.4 GPIO
				T2EX Timer 2 Trigger
				This pin can also be configured as T2EX signal for Timer 2. T2EX is the Timer 2 trigger input
				DL10
12	12	P2.3	I/O	Port 2.3 GPIO
				8051 P2.3 GPIO
				DL11
				Left driving line 11
13	15	P3.6	I/O	Port 3.6 GPIO
				8051 P3.6 GPIO
				RXD1
14	16	P2.2	I/O	This pin can also be configured as RXD of UART 1
				Port 2.2 GPIO
				8051 P2.2 GPIO.
				TXD1
				This pin can also be configured as TXD of UART 1
				8051 P2.2 GPIO. To allow proper operation as GPIO P2.2 function, crystal oscillator must be disabled by setting XOSCCFG register to 0x00



Pin Description (Continued)

Pin Number		Pin Name	Pin Type	Pin Function
QFN-6×6-48	QFN-7×7-56			
15, 18	17, 20	RSTN, TESTEN	I	Reset Low Active
				Typically connect a resistor to VDD and a capacitor to VSS
				Low asserted and threshold at $0.5 \times V_{DD}$. When forced low, the chip enters into reset condition
				This pin should not be connected to any level above V_{DD}
16	18	P1.3	I/O	Port 1.3 GPIO
				8051 P1.3 GPIO
				SCL
				This pin can also be configured as the SCL signal of the I ² C master or I ² C slave controller. In I ² C master mode, this pin should be configured as open-drain output. In I ² C slave mode, this pin should be configured as input only
17	19	P1.2	I/O	Port 1.2 GPIO
				8051 P1.2 GPIO
				SDA
				This pin can also be configured as the SDA signal of the I ² C master or I ² C slave controller. In this operation mode, this pin should also be configured as bi-directional I/O with open-drain output
19	21	P1.7	I/O	Port 1.7 GPIO
				8051 P1.7 GPIO
				PINT0.1
				This pin can also be configured as the expanded INTO interrupt
				T0 Timer 0 Input
				This pin can also be configured as Timer 0 input
				External Clock Input
External clock input source				
20	25	P1.0	I/O	Port 1.0 GPIO
				8051 P1.0 GPIO
				DR9
				Right driving line 9
21	26	P0.7	I/O	Port 0.7 GPIO
				8051 P0.7 GPIO
				RXD0
				This pin can also be configured as RXD of UART 0
				DR8
Right driving line 8				



Pin Description (Continued)

Pin Number		Pin Name	Pin Type	Pin Function
QFN-6×6-48	QFN-7×7-56			
22	27	P0.6	I/O	Port 0.6 GPIO
				8051 P0.6 GPIO
				TXD0
				This pin can also be configured as TXD of UART 0
				DR7
				Right driving line 7
23	28	P0.5	I/O	Port 0.5 GPIO
				8051 P0.5 GPIO
				PINT1.5
				This pin can also be configured as the expanded INT1 interrupt
				DR6
				Right driving line 6
24	29	P0.4	I/O	Port 0.4 GPIO
				8051 P0.4 GPIO
				PINT1.4
				This pin can also be configured as the expanded INT1 interrupt
				DR5
				Right driving line 5
25	30	P0.3	I/O	Port 0.3 GPIO
				8051 P0.3 GPIO
				PINT1.3
				This pin can also be configured as the expanded INT1 interrupt
				DR4
				Right driving line 4
26	31	P0.2	I/O	Port 0.2 GPIO
				8051 P0.2 GPIO
				DR3
				Right driving line 3
27	32	P0.1	I/O	Port 0.1 GPIO
				8051 P0.1 GPIO
				PINT1.1
				This pin can also be configured as the expanded INT1 interrupt.
				DR2
				Right driving line 2



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Pin Description (Continued)

Pin Number		Pin Name	Pin Type	Pin Function
QFN-6x6-48	QFN-7x7-56			
28	33	P0.0	I/O	Port 0.0 GPIO
				8051 P0.0 GPIO
				PINT1.0
				This pin can also be configured as the expanded INT1 interrupt
29	34	XCP_VSS	Power	DR1
				Right driving line 1
30	35	XCP	Power	Ground Voltage. 0V
				Boost Ground
31	36	VDD	Power	Supply Voltage. 1.6V to 2.0V
				1.8V boost in
32	37	VDD18	Power	Supply Voltage. 2.8V to 3.6V
				A good decoupling capacitor between VDD and VSS pins is critical for good performance
33	38	VDDE_N	I	Internal Regulator Output. 1.6V to 2.0V
				Typical decoupling capacitors of 0.1μF and 10μF should be connected between VDD18 and VSS
34	39	XCP_EN	I	CPU Power Supply Enable
				Supply voltage enable for 8051 CPU
35	40	S1	I/O, A	1.8V to 3.3V Boost Converter Enable
				3.3V Boost Supply voltage enable for 1.8V power input
36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, -	41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54	S2, S3, S4, S5, S6, S7, S8, S9, S10, S11, S12, S13, S14, S15	I, A	S1
				Sensing line 1
-	13	P3.2	I/O	S2, S3, S4, S5, S6, S7, S8, S9, S10, S11, S12, S13, S14, S15
				Sensing line 2 to 15
-	-	-	-	Port 3.2 GPIO
				8051 P3.2 GPIO
				DL12
				Left driving line 12

**Pin Description (Continued)**

Pin Number		Pin Name	Pin Type	Pin Function
QFN-6×6-48	QFN-7×7-56			
-	14	P3.3	I/O	Port 3.3 GPIO
				8051 P3.3 GPIO
				DL13
				Left driving line 13
-	22	P3.4	I/O	Port 3.4 GPIO
				8051 P3.4 GPIO
				DR12
				Right driving line 12
-	23	P3.5	I/O	Port 3.5 GPIO
				8051 P3.5 GPIO
				DR11
				Right driving line 11
-	24	P1.4	I/O	Port 1.4 GPIO
				8051 P1.4 GPIO
				DR10
				Right driving line 10
-	55,56	XDX0, XDX1	I, A	Driving line 26,27

Functional Block Diagram

AUR3852 I/O Assignment

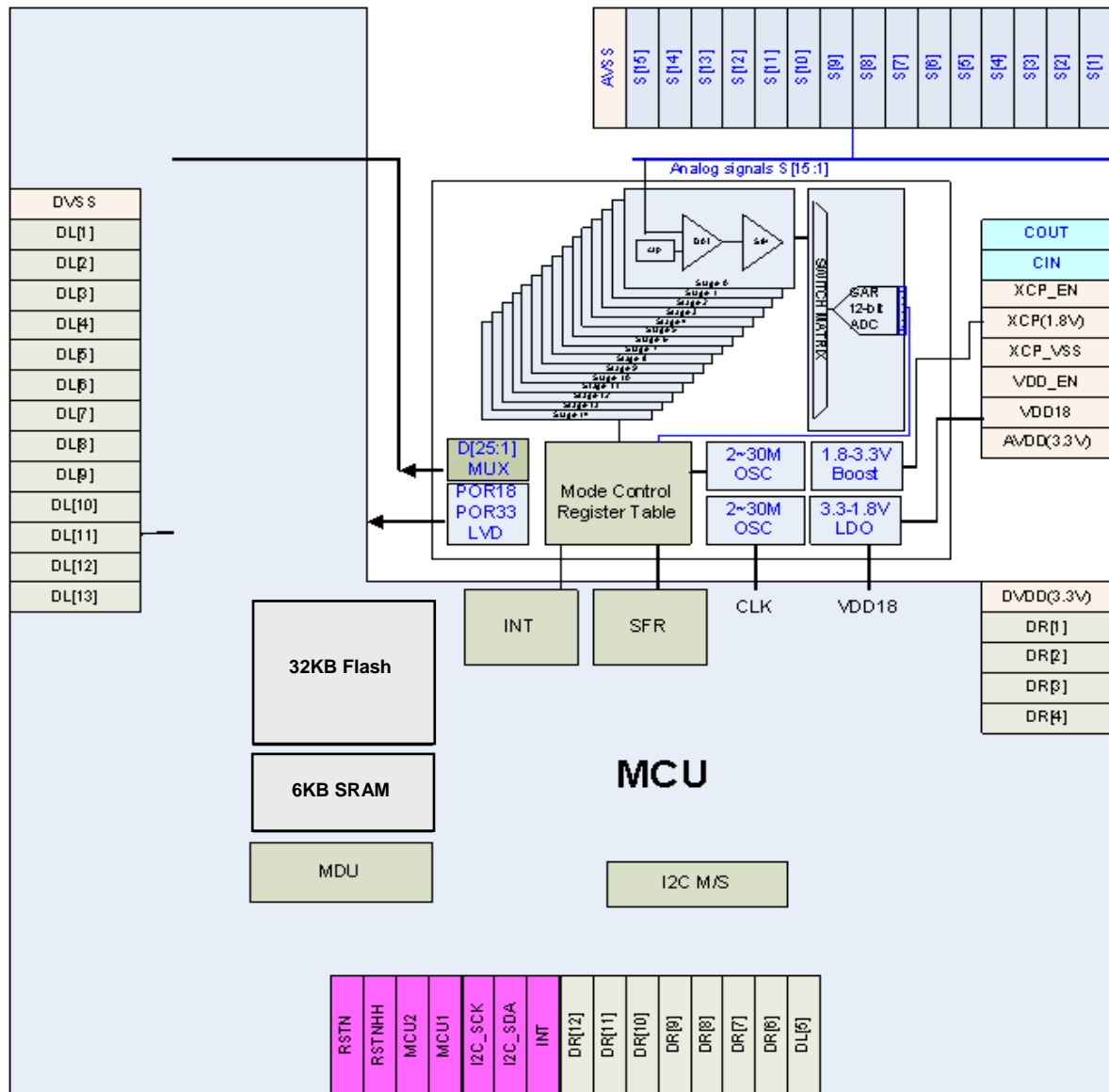
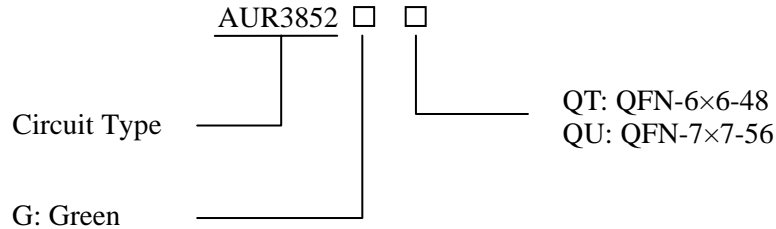


Figure 3. Main AFE I/O Pin Assignment and Whole Chip's Functional Block Diagram

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Ordering Information



Package	Temperature Range	Part Number	Marking ID	Packing Type
QFN-6x6-48	-40 to 85°C	AUR3852GQT	A3852GQT	Tape & Reel
QFN-7x7-56		AUR3852GQU	A3852GQU	Tape & Reel

BCD Semiconductor's Pb-free products, as designated with "G" in the part number, are RoHS compliant and green.

AUR3852 Support 4” to 7” Touch Panel, Listed Below:

PN	TX/RX	Multi-touch	Package	Panel size
AUR3852GQT	20/14	10 point 100Hz	QFN-6x6-48	4” to 5”
AUR3852GQU	27/15	10 point 100Hz	QFN-7x7-56	5” to 7”

Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Value	Unit
Supply Voltage	V _{DD}	2.8 to 3.6	V
Analog Input Voltage (Other pins)		-0.3 to V _{DD} +0.3	V
Logic Input Voltage		-0.3 to V _{DD} +0.3	V
Power Dissipation	P _D	250	mW
Maximum Junction Temperature	T _J	100	°C
Operating Temperature	T _{OP}	-40 to 85	°C
Storage Temperature	T _{STG}	-65 to 150	°C

Note 1: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to “Absolute Maximum Ratings” for extended periods may affect device reliability.



Enhanced Multi-touch Capacitive Touch Screen Controller AUR3852

Electrical Characteristics

DA/AC Characteristics for AFE

T_A=-40°C to 85°C, V_{DD}=3.3V, I²C bus frequency=400kHz, 12-bit mode, unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ADC DC Accuracy						
Resolution					12	Bits
No Missing Codes		Standard/Fast mode	11	12		Bits
Integral Linearity Error	INL	Standard/Fast mode		±3		LSB
Differential Linearity Error	DNL	External V _{REF}		±1.5		LSB
Offset Error					±6	LSB
Gain Error					±4	LSB
Analog Input						
Full-scale Input Span			0		V _{DD}	V
Absolute Input Range			-0.2		V _{DD} +0.2	V
ADC Sampling Dynamics						
Throughput Rate				250		ksps
Reference Input						
Input Voltage Range			1.8		V _{DD}	V
Switched-capacitor Integrator						
Output Voltage Range			0.3		V _{DD} -0.3	V
Integrator Capacitor	C _{INT}			12		pF
Power Supply						
Supply Voltage	V _{DD}	Operating voltage	2.8		3.6	V
Charge Pump Voltage	XCP		1.8		3.6	V
Quiescent Current		Standard mode: IOSC=2MHz to 24MHz		TBD		mA
		Low-speed mode: IOSC=32KHz		TBD		µA
		Power-down mode, V _{DDEEN} =low		3		µA
Temperature Range						
Specified Performance			-40		85	°C
3.3V to 1.8V LDO						
Internal 1.8V Regulator Output	V _{DD18} , 15mA		1.6	1.8	2.0	V
Output Voltage Trimming Level			-2/4/6	0	2/4/6	%
Internal OSC						
Frequency			2		24	MHz
Operating Current		Operating frequency =12MHz		50		µA
Frequency Trimming Level			-10/20/30	0	10/20/30	%
External Clock						
Frequency			2		24	MHz
Operating Current		Operating frequency=12MHz		50		µA

**Enhanced Multi-touch Capacitive Touch Screen Controller****AUR3852****Electrical Characteristics (Continued)****DA/AC Characteristics for 8051 CPU Core, Digital GPIO pins, Digital Peripherals, and IOSC**T_A=-40°C to 85°C, V_{DD}=2.8V to 3.6V, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Current						
Normal Mode Supply Current Using IOSC up to 24MHz	I _{DD} , normal IOSC1		7		mA	2
Normal Mode Supply Current Using IOSC<4MHz	I _{DD} , normal IOSC2		2.5		mA	2
PMM Mode Supply Current Using IOSC up to 24MHz	I _{DD} , PMM IOSC1		2.5		mA	2
PMM Mode Supply Current Using IOSC<4MHz	I _{DD} , PMM IOSC2		0.5		mA	2
Idle Mode Supply Current Using IOSC up to 24MHz	I _{DD} , idle IOSC1		2.5		mA	2
Stop Mode Supply Current Using IOSC Keeps Low, V _{DDEN} =low	I _{DD} , stop		3		μA	2
Digital GPIO Characteristics						
High Level Input Voltage	V _{IH}	2		3.6	V	3
	V _{IH} , SDA/SCL	1.6		3.6	V	3
Low Level Input Voltage	V _{IL}	-0.3		0.8	V	3
	V _{IL} , SDA/SCL	-0.3		0.5	V	3
High Level Output Voltage	V _{OH}	2.4			V	
Low Level Output Voltage	V _{OL}			0.4	V	
High Level Output Current @V _{OH} (min)	I _{OH} (2mA)	3.0	7.8	12.9	mA	
	I _{OH} (4mA)	7.7	15.6	25.8	mA	
Low Level Output Current @V _{OL} (max)	I _{OL} (2mA)	3.4	5.4	7.4	mA	
	I _{OL} (4mA)	6.7	10.7	14.7	mA	
Input Pull Up Resistance	R _{PU}	34		74	kΩ	3
Input Pull Down Resistance	R _{PD}	29		86	kΩ	3
Input Low to High Level, RSTN	V _{IH} , RSTN	1.56		1.71	V	4
Input High to Low Level, RSTN	V _{IL} , RSTN	1.16		1.30	V	4
Output Rise Time	t _{RISE}		5		ns	7
Output Fall Time	t _{FALL}		5		ns	7
Internal 3.3V to 1.8V LDO from AFE						
Internal 1.8V Regulator Output	V _{DD18} , 15mA	1.6	1.8	2.0	V	5
Power On/Off Reset Level	V _{DD18} , Reset	80	85	90	%	6

Note 2: Does not include load current and tested under NOP loop and all peripheral disabled.

Note 3: For Digital I/O only.

Note 4: For RSTN pin only.

Note 5: Supply to internal digital and analog circuit only.

Note 6: This is measured as the percentage of steady state value of V_{DD18}.

Note 7: This is measured with 20pF load and 20% to 80% output level.

Enhanced Multi-touch Capacitive Touch Screen Controller AUR3852

Typical Application

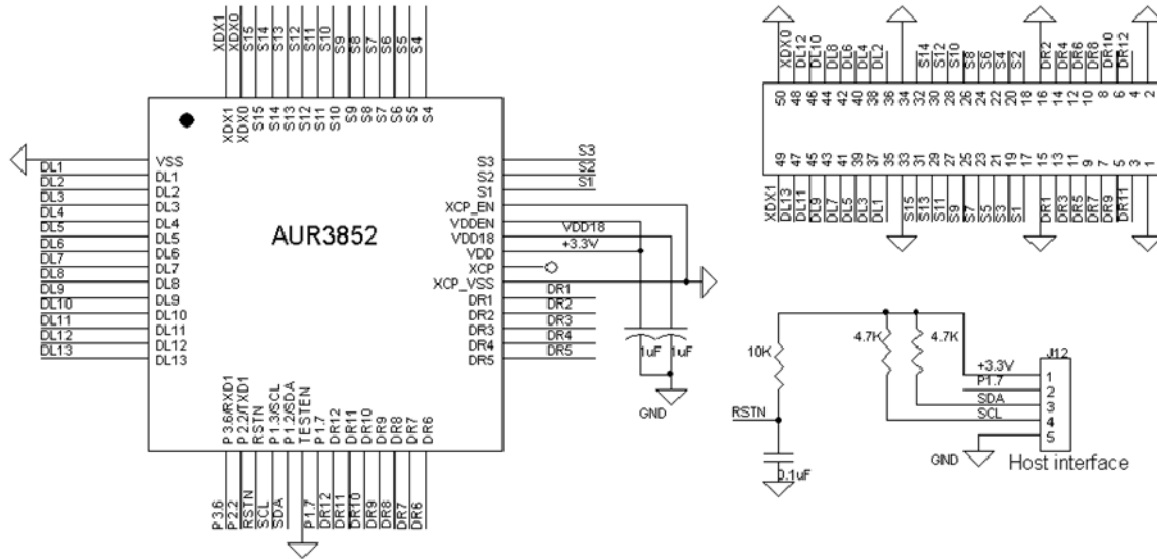
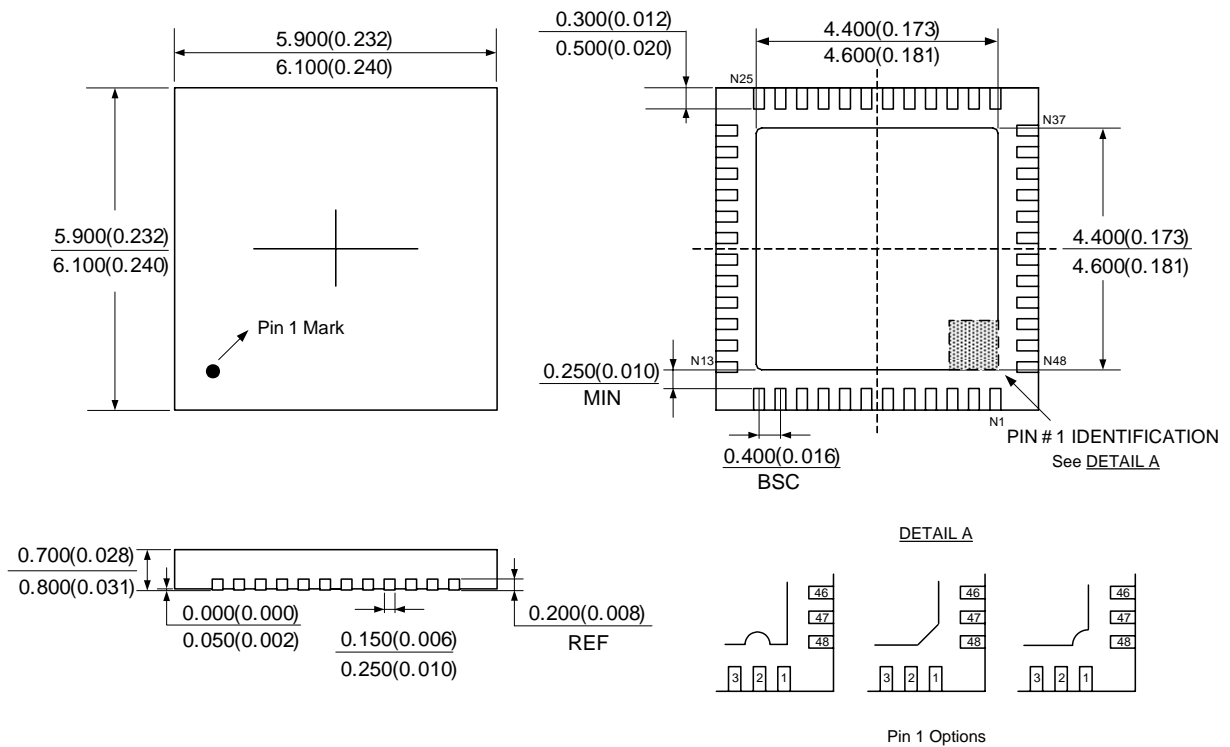


Figure 4. Typical Application of AUR3852 (For QFN-7x7-56 Package)

Mechanical Dimensions

QFN-6x6-48

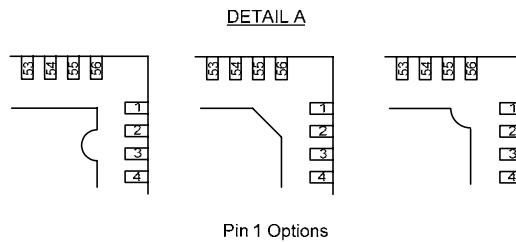
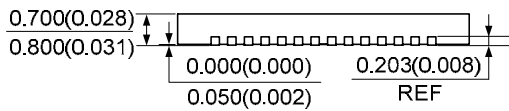
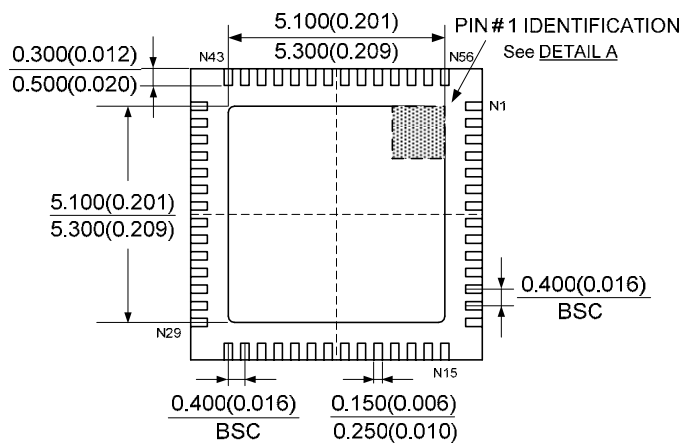
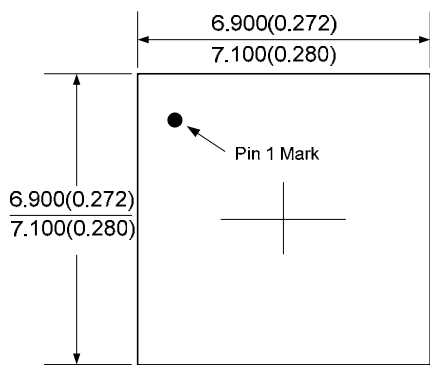
Unit: mm(inch)



Mechanical Dimensions (Continued)

QFN-7x7-56

Unit: mm(inch)





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