



UCD4070B

Preliminary

CMOS IC

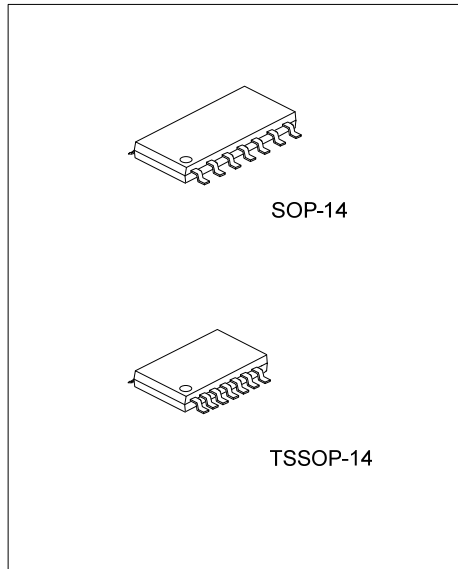
CMOS QUAD EXCLUSIVE-OR GATE

DESCRIPTION

The **UCD4070B** contains four independent 2-input Exclusive-OR gates, they perform the function $Y=A\oplus B$ in positive logic.

FEATURES

- * High-Voltage Types(20V Rating)
- * Quad Exclusive-OR Gate
- * Standardized Symmetrical Output Characteristics
- *100% Tested for Quiescent Current at 20V
- * 5V,10V and 15V Parametric Ratings
- *Maximum input current of 1uA at 18V Over Full Package Temperature Range
 - 100nA at 18V and 25°C
- *Medium Speed Operation
 - t_{PHL} , t_{PLH} =65ns(TYP) at V_{DD} =10V, C_L =50pF

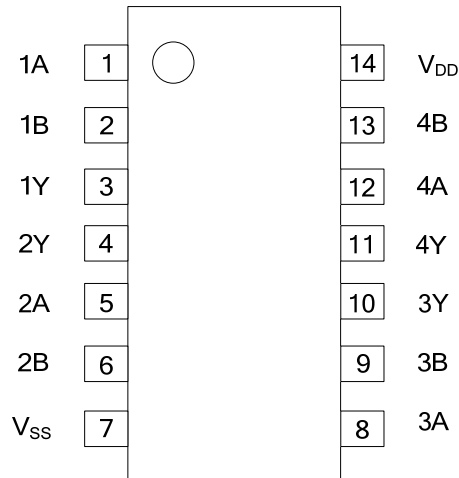


ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
UCD4070BL-S14-R	UCD4070BG-S14-R	SOP-14	Tape Reel
UCD4070BL-S14-T	UCD4070BG-S14-T	SOP-14	Tube
UCD4070BL-P14-R	UCD4070BG-P14-R	TSSOP-14	Tape Reel
UCD4070BL-P14-T	UCD4070BG-P14-T	TSSOP-14	Tube

<p>UCD4070BG-S14-T</p> <p>(1)Packing Type (2)Package Type (3)Halogen Free</p>	<p>(1) T: Tube, R: Tape Reel (2) S14: SOP-14, P14: TSSOP-14 (3) L: Lead Free, G: Halogen Free</p>
---	---

■ PIN CONFIGURATION



■ FUNCTION TABLE (each gate)

INPUT(A)	INPUT(B)	OUTPUT(Y)
H	H	L
H	L	H
L	H	H
L	L	L

■ LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATING (unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	-0.5 ~ 20	V
Input Voltage	$V(nA,nB)$	-0.5 ~ $V_{DD} + 0.5$	V
Operating Temperature	T_{STG}	-65 ~ + 150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{DD}		3		18	V
Operating Temperature	T_{OPR}		-40		125	°C

■ ELECTRICAL CHARACTERISTICS($T_A=25^\circ\text{C}$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Input Voltage	V_{IH}	$V_{DD}= 5V, V_O=0.5V$	3.5			V
		$V_{DD}= 10V, V_O=1.0V$	7.0			
		$V_{DD}= 15V, V_O=1.5V$	11.0			
Low-Level Input Voltage	V_{IL}	$V_{DD}= 5V, V_O=4.5V$			1.5	V
		$V_{DD}= 10V, V_O=9.0V$			3.0	
		$V_{DD}= 15V, V_O=13.5V$			4.0	
High-Level Output Voltage	V_{OH}	$V_{DD}= 5V, \text{No Load}$	4.95	5		V
		$V_{DD}= 10V, \text{No Load}$	9.95	10		
		$V_{DD}= 15V, \text{No Load}$	14.95	15		
Low-Level Output Voltage	V_{OL}	$V_{DD}= 5V, \text{No Load}$		0	0.05	V
		$V_{DD}= 10V, \text{No Load}$		0	0.05	
		$V_{DD}= 15V, \text{No Load}$		0	0.05	
High-Level Output Current (NOTE)	I_{OH}	$V_{DD}= 5V, V_O=4.6V$	-0.51	-1		mA
		$V_{DD}= 5V, V_O=2.5V$	-1.6	-3.2		
		$V_{DD}= 10V, V_O=9.5V$	-1.3	-2.6		
		$V_{DD}= 15V, V_O=13.5V$	-3.4	-6.8		
Low-Level Output Current (NOTE)	I_{OL}	$V_{DD}= 5V, V_O=0.4V$	0.51	1		mA
		$V_{DD}= 10V, V_O=0.5V$	1.3	2.6		
		$V_{DD}= 15V, V_O=1.5V$	3.4	6.8		
Input Leakage Current	$I_{I(LEAK)}$	$V_{DD}= 15V, V_{IN} = V_{DD} \text{ or } GND$			± 0.1	μA
Quiescent Supply Current	I_{DD}	$V_{DD}= 5V, V_{IN} = V_{DD} \text{ or } V_{SS}, I_{OUT} = 0$		0.01	0.25	μA
		$V_{DD}= 10V, V_{IN} = V_{DD} \text{ or } V_{SS}, I_{OUT} = 0$		0.01	0.5	
		$V_{DD}= 15V, V_{IN} = V_{DD} \text{ or } V_{SS}, I_{OUT} = 0$		0.01	1.0	
		$V_{DD}= 20V, V_{IN} = V_{DD} \text{ or } V_{SS}, I_{OUT} = 0$		0.02	5.0	

Note: I_{OL} and I_{OH} are tested one output at a time

■ SWITCHING CHARACTERISTICS

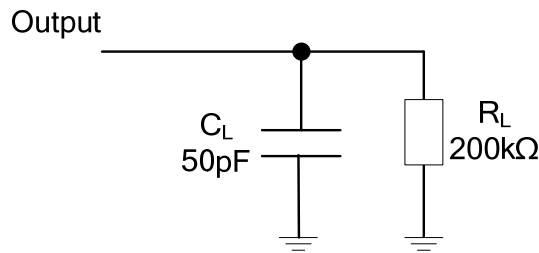
($T_A=25^\circ\text{C}$, Input: $t_R=t_F=20\text{ns}$, $C_L=50\text{pF}$, $R_L=200\text{K}\Omega$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from Input(A or B) to Output(Y)	t_{PLH}	$V_{DD}=5\text{V}$		140	280	ns
		$V_{DD}=10\text{V}$		65	130	
		$V_{DD}=15\text{V}$		50	100	
	t_{PHL}	$V_{DD}=5\text{V}$		140	280	
		$V_{DD}=10\text{V}$		65	130	
		$V_{DD}=15\text{V}$		50	100	
Transition Time	t_{TLH}	$V_{DD}=5\text{V}$		100	200	ns
		$V_{DD}=10\text{V}$		50	100	
	t_{THL}	$V_{DD}=15\text{V}$		40	80	

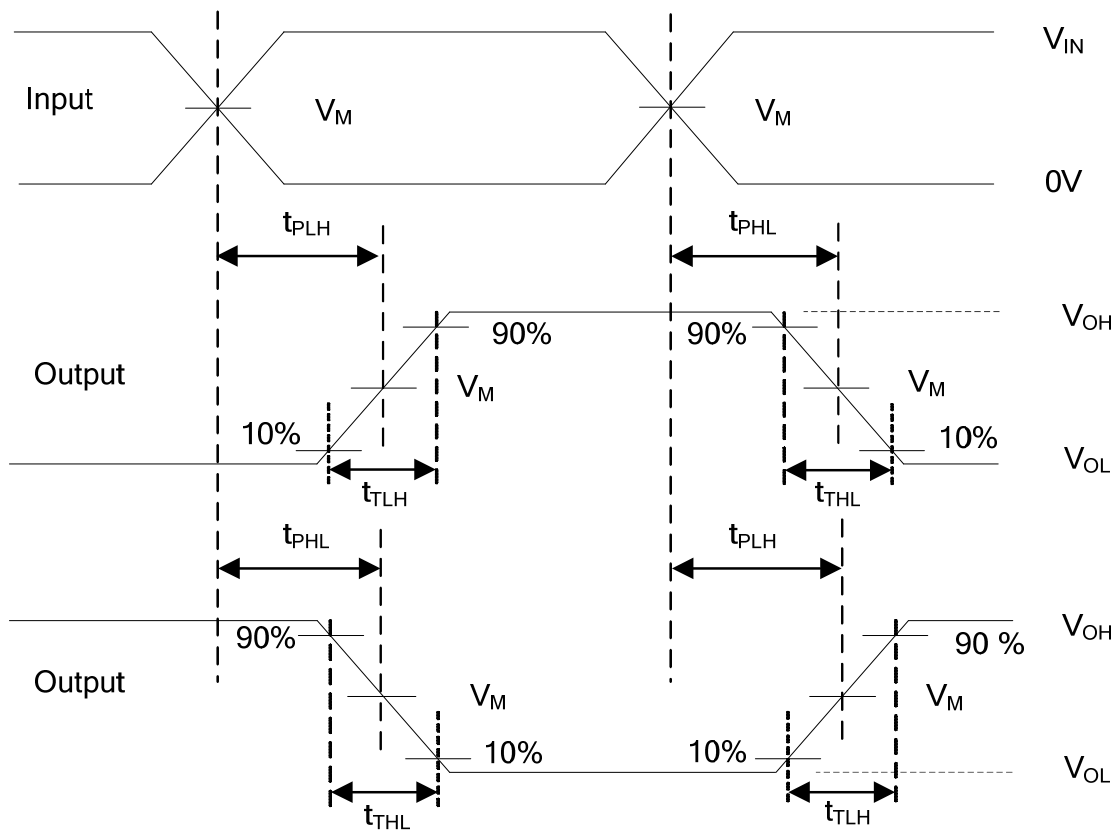
■ OPERATING CHARACTERISTICS($T_A=25^\circ\text{C}$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Average Input Capacitance	C_{IN}	Any Input		5	7.5	pF

■ TEST CIRCUIT AND WAVEFORMS



Definitions for test circuit



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

Note: C_L includes probe and jig capacitance.

UTC assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all UTC products described or contained herein. UTC products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice.