MN101E51/52 Series

8-bit Single-chip Microcontroller

■ Overview

The MN101E series of 8-bit single-chip microcomputers (the memory expansion version of MN101C series) incorporate multiple types of peripheral functions. This chip series is well suited for automotive power window, camera, VCR, MD, TV, CD, LD, printer, telephone, home automation, pager, air conditioner, PPC, fax machine, music instrument and other applications.

This LSI brings to embedded microcomputer applications flexible, optimized hardware configurations and a simple efficient instruction set. MN101EF51A/52A has an internal 32 KB of ROM and 1 KB of RAM. Peripheral functions include 5 (MN101EF52A: 4) external interrupts, 20 (MN101EF52A: 18) internal interrupts including NMI, 8 timer counters, 3 (MN101EF52A: 2) types of serial interfaces, A/D converter, 2 types of watchdog timer and buzzer output (MN101EF52A: no buzzer). The system configuration is suitable for system control microcontroller such as camera, timer selector for VCR, CD player, or minicomponent.

With 5 oscillation systems (high-speed (internal frequency: 20 MHz), high-speed (crystal/ceramic frequency: max. 10 MHz) / low-speed (internal frequency: 30 kHz), low-speed (crystal/ceramic frequency: 32.768 kHz) and PLL: frequency multiplier of high frequency) contained on the chip, the system clock can be switched to high-speed frequency input (NORMAL mode), PLL input (PLL mode), or to low-speed frequency input (SLOW mode). The system clock is generated by dividing the oscillation clock or PLL clock. The best operation clock for the system can be selected by switching its frequency ratio by programming. High speed mode has the normal mode which is based on the clock dividing fpll, (fpll is generated by original oscillation and PLL), by 2 (fpll/2), and the double speed mode which is based on the clock not dividing fpll.

A machine cycle (minimum instruction execution time) in the normal mode is 200 ns when the original oscillation fosc is 10 MHz (PLL is not used). A machine cycle in the double speed mode, in which the CPU operates on the same clock as the external clock, is 100 ns when fosc is 10 MHz. A machine cycle in the PLL mode is 50 ns (maximum).

■ Product Summary

This datasheet describes the following model.

Model	ROM Size	RAM Size	Classification	Package
MN101EF51A	32 KB	1 KB	Flash EEPROM version	QFP044-P-1010F TQFP048-P-0707B
MN101EF52A				TQFP032-P-0707A

Note) DMOD internal pull-up resistor is in only Flash EEPROM version.
When using In-circuit Emulator, it is necessary to connect the pull-up resistor on the circuit board.

■ Features

- ROM capacity
  32 KB

- RAM capacity
  1 KB

- Package:
  MN101EF51A
    44-Pin QFP (10 mm × 10 mm / 0.8 mm pitch)
    48-Pin TQFP (7 mm × 7 mm / 0.5 mm pitch)
  MN101EF52A
    32-Pin TQFP (7 mm × 7 mm / 0.8mm pitch)

- Machine Cycle:
  High-speed mode
    0.05 µs / 20 MHz (2.7 V to 5.5 V)
    0.125 µs / 8 MHz (1.8 V to 5.5 V)
  Low-speed mode
    62.5 µs / 32 kHz (1.8 V to 5.5 V)

- Clock Gear Circuit:
  Internal system clock speed is changeable by selecting division ratio of oscillation clock. (Divided by 1, 2, 4, 16, 32, 64, 128)

- High-speed Clock (fpll-div) Gear Circuit for peripheral functions:
  Can be selected among "stop", fpll/1, fpll/2, fpll/4, fpll/8, and fpll/16.

- Oscillation Circuit: 4 types
  High-speed (Internal oscillation: frc), High-speed (crystal/ceramic: fosc),
  Low-speed (Internal oscillation: frcs), Low-speed (crystal/ceramic: fx)
    High-speed internal oscillation 20 MHz / 16 MHz (selectable)
    Low-speed internal oscillation 30 kHz

- Clock Multiplication Circuit:
  PLL circuit output clock (fpll) fosc multiplied by 2, 3, 4, 5, 6, 8, 10, 1/2 × frc multiplied by 4, 5 enabled
    * When clock multiplication circuit is not used, fpll = fosc or fpll = frc

- Operation Mode
  NORMAL mode (high-speed mode)
  PLL mode
  SLOW mode (low-speed mode)
  HALT mode
  STOP mode
    and operation clock switching

- Operating Voltage
  1.8 V to 5.5 V

- Operating Ambient Temperature:
  –40°C to +85°C

■ Features (continued)

- Interrupts: 25 sets (MN101EF52A: 22 sets)

<Overrun interrupt>
Non-maskable interrupt (NMI)
<Timer interrupt>
Timer 0 interrupt
Timer 1 interrupt
Timer 2 interrupt
Timer 6 interrupt
Time-base interrupt
Timer 7 interrupt
Timer 7 compare register 2 match interrupt
Timer 9 overflow interrupt
Timer 9 underflow interrupt
Timer 9 compare register 2 match interrupt
<Serial interrupt>
Serial 0 interrupt
Serial 0 UART reception interrupt
Serial 1 interrupt (MN101EF52A does not have this function)
Serial 1 UART reception interrupt (MN101EF52A does not have this function)
Serial 4 interrupt
Serial 4 stop condition interrupt
<A/D interrupt>
A/D conversion interrupt
<Low voltage detection interrupt>
Low voltage detection interrupt
<External interrupt>
IRQ0 : Edge selection, noise filter connectable
IRQ1 : Edge selection, noise filter connectable
IRQ2 : Edge selection, noise filter connectable, both edge interrupt
IRQ3 : Edge selection, noise filter connectable, both edge interrupt
IRQ4 : Edge selection, noise filter connectable, both edge interrupt, key scan interrupt
(MN101EF52A does not have this function)

■ Features (continued)

- Timer Counter: 8 sets

General-purpose 8-bit timer × 3 sets
General-purpose 16-bit timer × 1 sets
Motor control 16-bit timer × 1 set
8-bit free-run timer × 1 set
Time-base timer × 1 set
Baud rate timer × 1 set

Timer 0 (General-purpose 8-bit timer)
Square wave output (Timer pulse output), added pulse (2-bit) type PWM output can be output to large current pin TM0IOB, event count, remote control carrier, simple pulse width measurement
Clock source: fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, fslow, external clock, timer A output

Timer 1 (General-purpose 8-bit timer)
Square wave output (Timer pulse output) can be output to large current pin TM1IOB, event count, 16-bit cascade connection (connected with timer 0)
Clock source: fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, fslow, external clock, timer A output

Timer 2 (General-purpose 8-bit timer)
Square wave output (Timer pulse output), added pulse (2-bit) type PWM output can be output to large current pin TM2IOB, event count, simple pulse width measurement, 24-bit cascade connection (connected with timer 0, 1)
Clock source: fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, fslow, external clock, timer A output

Timer 6 (8-bit free-run timer, time-base timer)
8-bit free-run timer
Clock source: fpll-div, fpll-div/2^{12}, fpll-div/2^{13}, fs, fslow, fslow/2^{12}, fslow/2^{13}
Time-base timer
Interrupt generation cycle
fpll-div/2^{7}, fpll-div/2^{8}, fpll-div/2^{9}, fpll-div/2^{10}, fpll-div/2^{13}, fpll-div/2^{15}, fslow/2^{7}, fslow/2^{8}, fslow/2^{9}, fslow/2^{10}, fslow/2^{13}, fslow/2^{15}

Timer 7 (General-purpose 16-bit timer)
Clock source: fpll-div, fs, external clock, timer A output, timer 6 compare match cycle divided by 1, 2, 4, 16, external clock, timer A output divided by 1, 2, 4, 16
Timer function
Square wave output (Timer pulse output), high-precision PWM output (cycle/duty continuous changeable) can be output to large current pin TM7IOB, event count, input capture function (both edges operable)

Timer 9 (Motor control 16-bit timer)
Clock source: fpll-div, fs, external clock, Timer A output divided by 1, 2, 4, 16
Timer function
Square wave output (Timer pulse output), complementary 3-phase PWM output can be output to large current pin TM9OD0 to 5
Triangle wave and saw tooth wave are supported, dead time insertion available, event count
Pin output control
PWM output control is possible by external interrupt 0 to 4 (IRQ 0 to 4). ("Hi-z", output data fixed)

Timer A (baud rate timer)
Clock output for peripheral functions
Clock source: fpll-div divided by 1, 2, 4, 8, 16, 32, and fs divided by 2, 4

■ Features (continued)

- Watchdog timer

  Software processing error detection cycle is selectable from $fs/2^{16}$, $fs/2^{18}$, $fs/2^{20}$

  System reset is generated by the hardware when software processing error is detected twice

- Watchdog timer2

  Software processing error detection cycle is selectable from $frcs/2^4$, $frcs/2^5$, $frcs/2^6$, $frcs/2^7$, $frcs/2^8$, $frcs/2^9$, $frcs/2^{10}$, $frcs/2^{11}$, $frcs/2^{12}$, $frcs/2^{13}$, $frcs/2^{14}$, $frcs/2^{15}$

  System reset is generated by the hardware when software processing error is detected twice

- Buzzer output (MN101EF51A only)

  Output frequency is selectable from $fpll/2^9$, $fpll/2^{10}$, $fpll/2^{11}$, $fpll/2^{12}$, $fpll/2^{13}$, $fpll/2^{14}$, $fslow/2^3$, $fslow/2^4$

- Remote control carrier output

  Remote control carrier of 1/2 or 1/3 duty cycle can be output based on timer 0

- A/D converter

  10-bit × 12 channels (MN101EF51A)

  10-bit × 8 channels (MN101EF52A)

- Serial Interface: 3 systems

  Serial 0 (Full duplex UART / Synchronous serial interface)

  Synchronous serial interface

  Transfer clock source: fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/64, fs/2, fs/4, Timer 0 to 2, Timer A output divided by 1, 2, 4, 8, 16, External clock

  MSB/LSB can be selected as the first bit to be transferred, arbitrary size of 1 to 8 bits are selectable.

  Continuous transmission, continuous reception, continuous transmission/reception are available.

  Full duplex UART (Baud rate timer: selected from timer 0 to 2, or timer A)

  Parity check, overrun error/framing error are detected

  Transfer bits of 7 to 8 are selectable

  Serial 1 (Full duplex UART / Synchronous serial interface) (MN101EF52A does not have this function)

  Synchronous serial interface

  Transfer clock source: fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/64, fs/2, fs/4, Timer 0 to 2, Timer A output divided by 1, 2, 4, 8, 16, External clock

  MSB/LSB can be selected as the first bit to be transferred, arbitrary size of 1 to 8 bits are selectable.

  Continuous transmission, continuous reception, continuous transmission/reception are available.

  Full duplex UART (Baud rate timer: selected from timer 0 to 2, or timer A)

  Parity check, overrun error/framing error are detected

  Transfer bits of 7 to 8 are selectable

  Serial 4 (Multi master IIC / Synchronous serial interface)

  Synchronous serial interface

  Transfer clock source: fpll-div/2, fpll-div/4, fpll-div/8, fpll-div/32, fs/2, fs/4, Timer 0 to 2, Timer A output divided by 1, 2, 4, 8, 16, External clock

  MSB/LSB can be selected as the first bit to be transferred, arbitrary size of 1 to 8 bits are selectable.

  Continuous transmission, continuous reception, continuous transmission/reception are available.

  Multi master IIC

  7-bit slave address is settable

  General call communication mode is supported

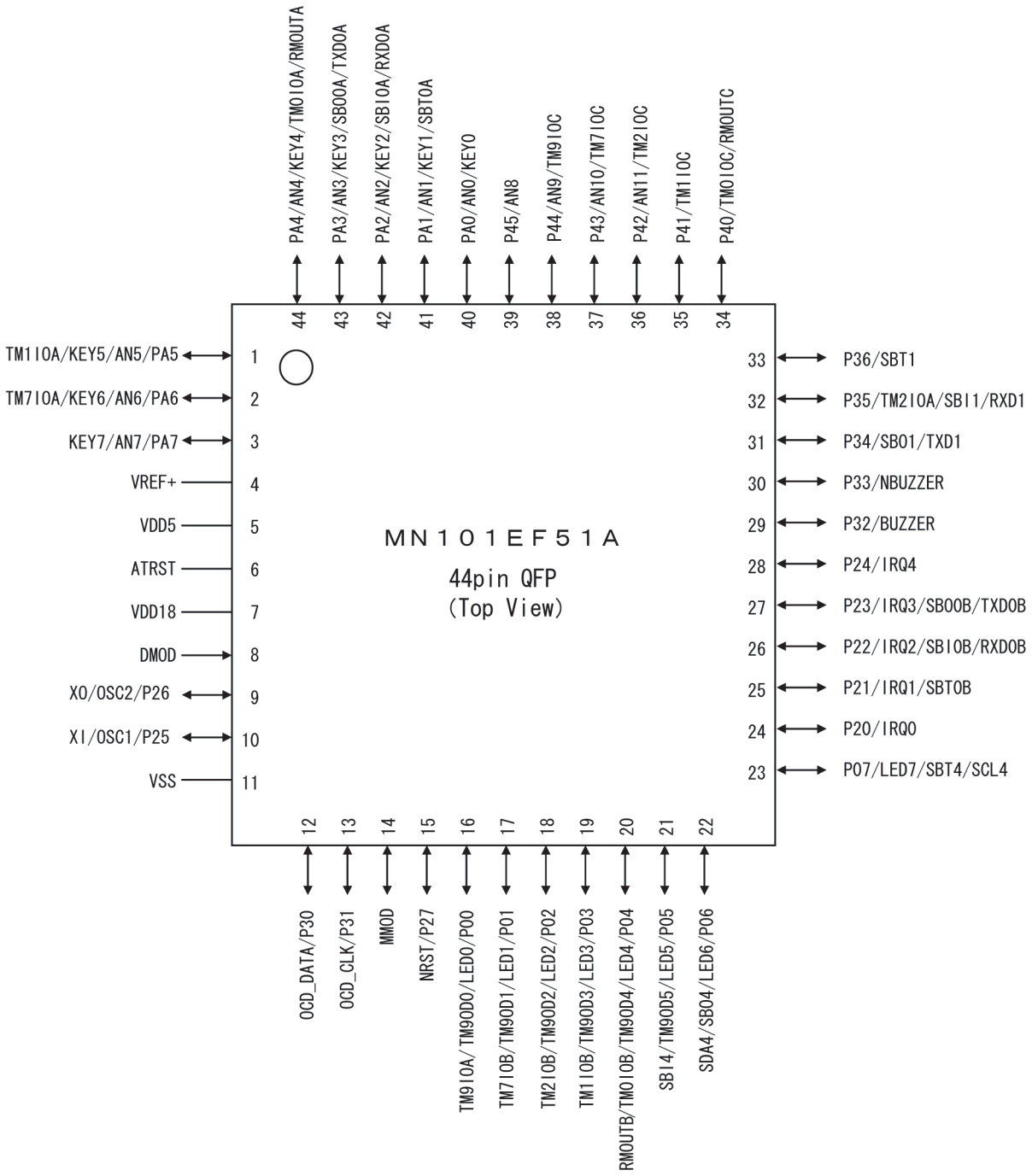
■ Features (continued)

- Auto reset circuit
- Power supply voltage detection circuit
- LED driver: 8 sets
- Ports

Ports	MN101EF51A (pins)	MN101EF52A (pins)
I/O ports	36	24
Serial interface dual ports	12	9
Timer I/O dual ports	15	9
Buzzer output dual ports	2	—
A/D input dual ports	12	8
External interrupt dual ports	5	4
LED (large current) driver dual ports	8	8
High/Low-speed oscillation	2	2
Special function pins	8	8
Operating mode control input pins	3	3
Reset input dual pin	1	1
Analog reference voltage input pin	1	1
Power supply pins	3	3

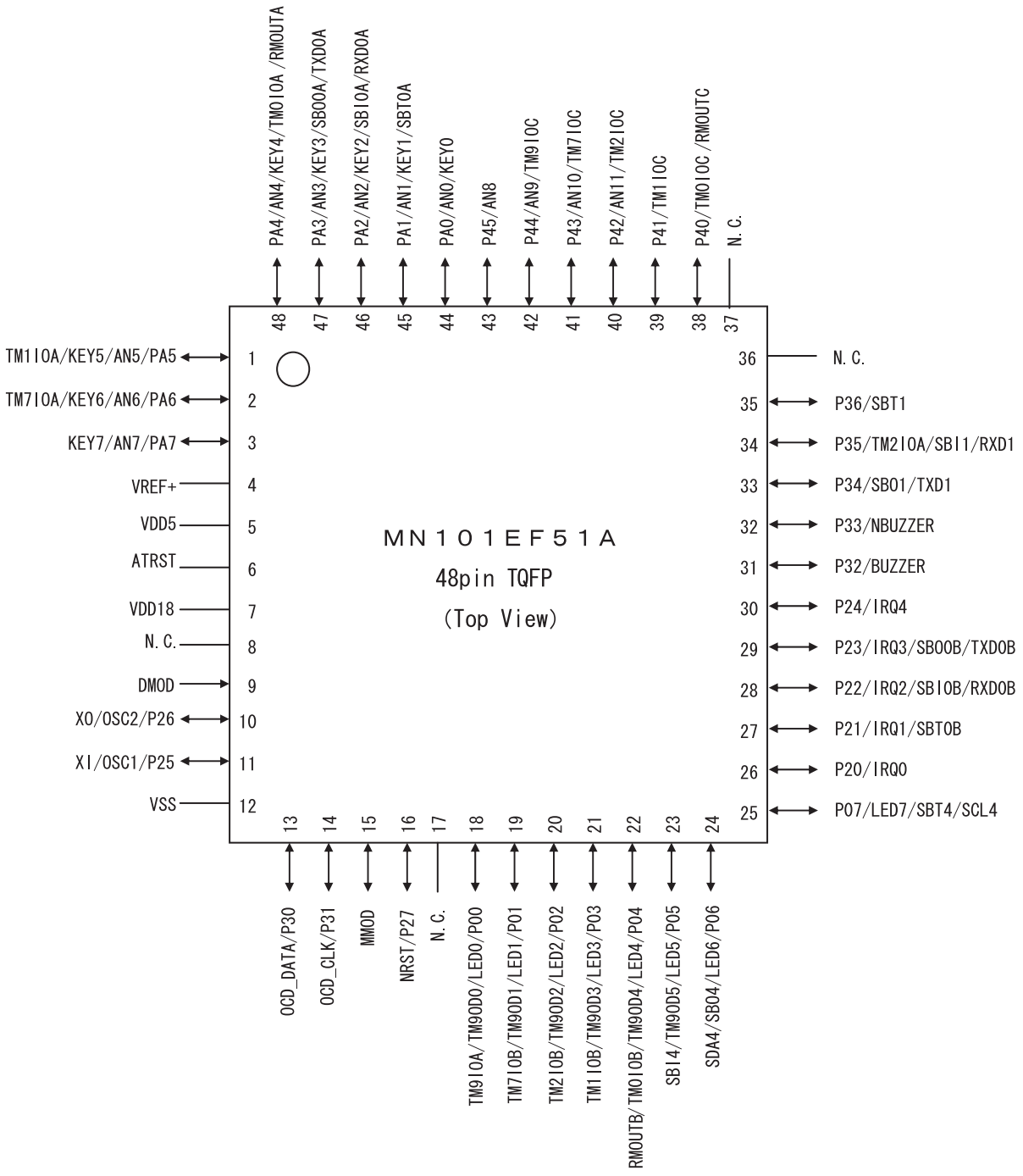
■ Pin Description

• MN101EF51A (QFP044-P-1010F)



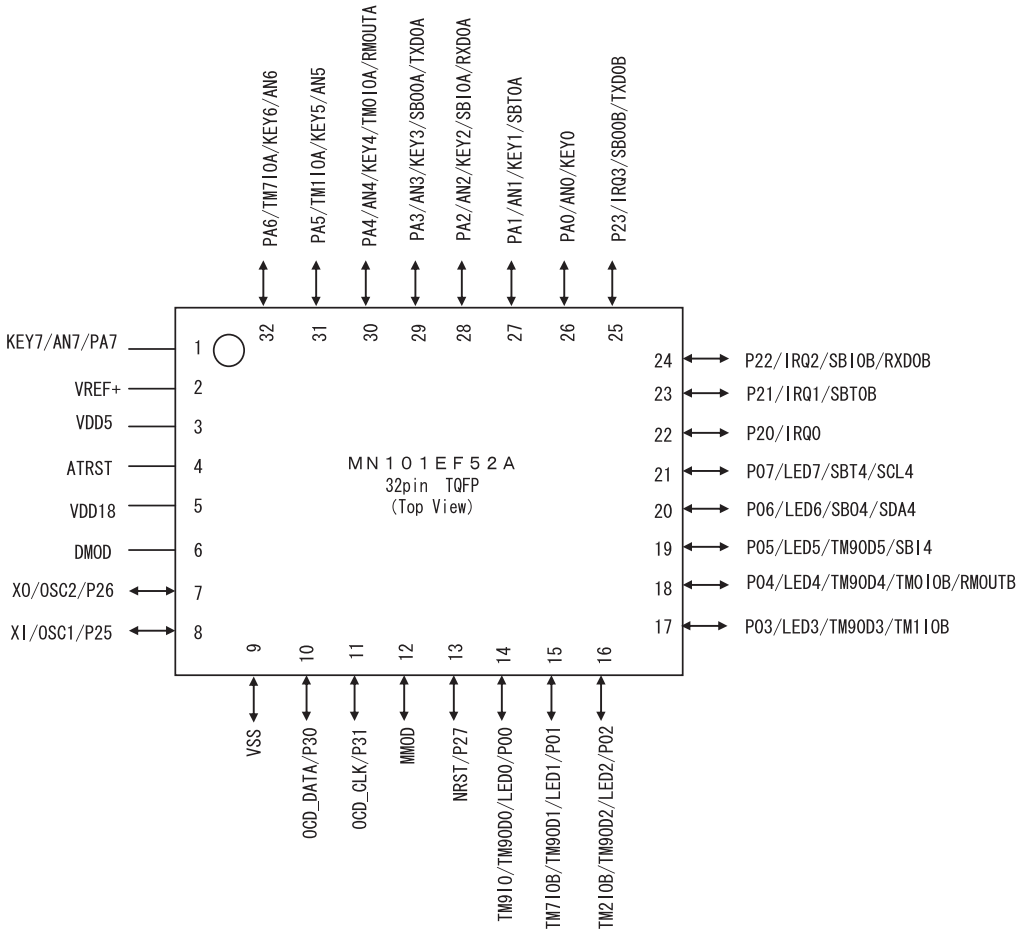
■ Pin Description (continued)

• MN101EF51A (TQFP048-P-0707B)



■ Pin Description (continued)

• MN101EF52A (TQFP032-P-0707A)



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