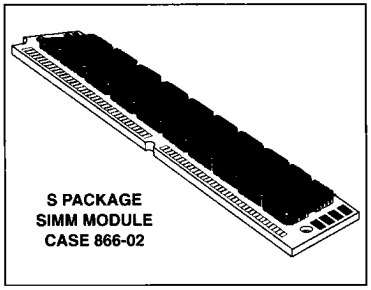
MCM40400

Product Preview

4M x 40 Bit Dynamic Random Access Memory Module

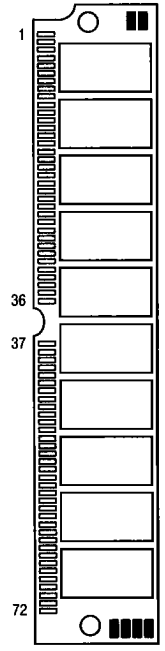
for Error Correction Applications



The MCM40400 is a dynamic random access memory (DRAM) module organized as 4,194,304 x 40 bits. The module is a double-sided 72-lead single-in-line memory module (SIMM) consisting of ten MCM517400 DRAMs housed in J-lead small outline packages (SOJ), mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted under each DRAM. The MCM517400 is a CMOS high-speed dynamic random access memory organized as 4,194,304 four-bit words and fabricated with CMOS silicon-gate process technology.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{RAS}$-Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 2048 Cycle Refresh: MCM40400 = 32 ms (Max)
- Consists of Ten 4M x 4 DRAMs, and Ten 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}): MCM40400-60 = 60 ns (Max)
  MCM40400-70 = 70 ns (Max)
  MCM40400-80 = 80 ns (Max)
- Low Active Power Dissipation: MCM40400-60 = 6.60 W (Max)
  MCM40400-70 = 5.50 W (Max)
  MCM40400-80 = 4.68 W (Max)
- Low Standby Power Dissipation: TTL Levels = 110 mW (Max)
  CMOS Levels= 55 mW (Max)

TOP VIEW



PIN NAMES	
A0 – A10 ..... Address Inputs	DQ0 – DQ39 ..... Data Input/Output
$\overline{CAS0}$ ..... Column Address Strobe	PD1 – PD5 ..... Presence Detect
$\overline{RAS0}$ ..... Row Address Strobe	$\overline{W}$ ..... Read/Write Input
$\overline{X40}$ ..... Configuration Detection	$\overline{OE}$ ..... Output Enable
V_{CC} ..... Power (+ 5 V)	V_{SS} ..... Ground
NC ..... No Connection	

All power supply and ground pins must be connected for proper operation of the device.

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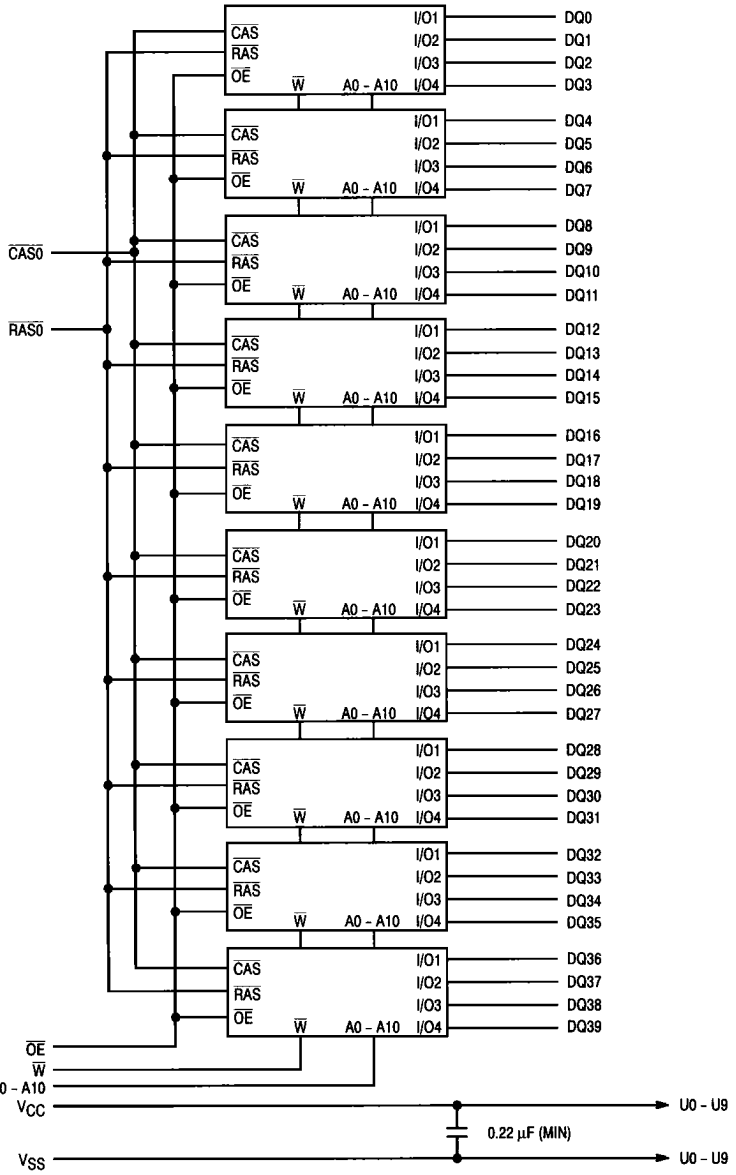
This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

BLOCK DIAGRAM



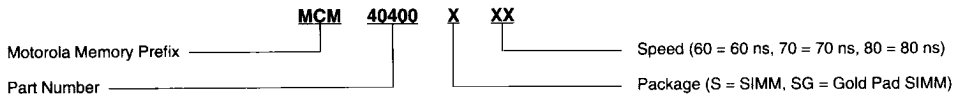
PRESENCE DETECT PIN OUT			
Pin Name	**60 ns**	**70 ns**	**80 ns**
PD1	V_{SS}	V_{SS}	V_{SS}
PD2	NC	NC	NC
PD3	NC	V_{SS}	NC
PD4	NC	NC	V_{SS}
PD5*	V_{SS}	V_{SS}	V_{SS}
$\overline{X40}$	V_{SS}	V_{SS}	V_{SS}

*PD5 tied to V_{SS} through a 2.6 kΩ resistor.

PIN ASSIGNMENTS

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	13	A1	25	DQ13	37	DQ19	49	DQ22	61	DQ33
2	DQ0	14	A2	26	DQ14	38	DQ20	50	DQ23	62	DQ34
3	DQ1	15	A3	27	DQ15	39	V_{SS}	51	DQ24	63	DQ35
4	DQ2	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ25	64	DQ36
5	DQ3	17	A5	29	DQ16	41	A10	53	DQ26	65	DQ37
6	DQ4	18	A6	30	V_{CC}	42	NC	54	DQ27	66	DQ38
7	DQ5	19	$\overline{OE}$	31	A8	43	NC	55	DQ28	67	PD1
8	DQ6	20	DQ8	32	A9	44	$\overline{RAS0}$	56	DQ29	68	PD2
9	DQ7	21	DQ9	33	NC	45	NC	57	DQ30	69	PD3
10	V_{CC}	22	DQ10	34	NC	46	DQ21	58	DQ31	70	PD4
11	PD5	23	DQ11	35	DQ17	47	$\overline{W}$	59	V_{CC}	71	DQ39
12	A0	24	DQ12	36	DQ18	48	$\overline{X40}$	60	DQ32	72	V_{SS}

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM40400S60 MCM40400SG60
MCM40400S70 MCM40400SG70
MCM40400S80 MCM40400SG80

NOTE: For mechanical data, please see Chapter 10.