

# INTELLIGENT INTERACTIVE SYNTHESIZER

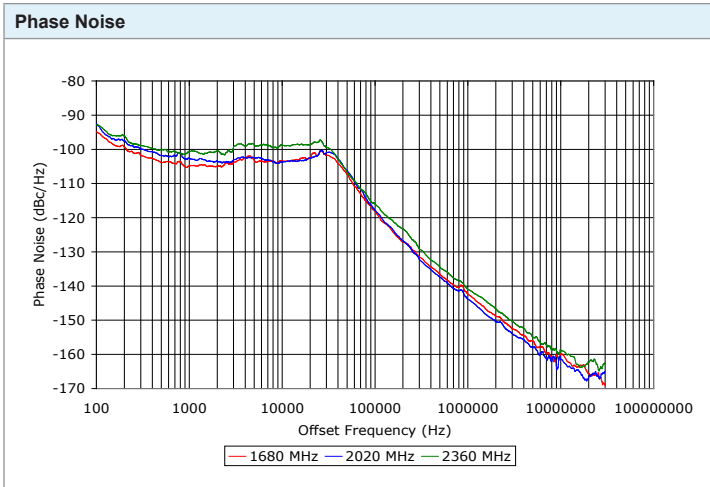
## SURFACE MOUNT MODEL: LFSW168236-100

**OPTIMIZED BANDWIDTH**

**1680 - 2360 MHz**

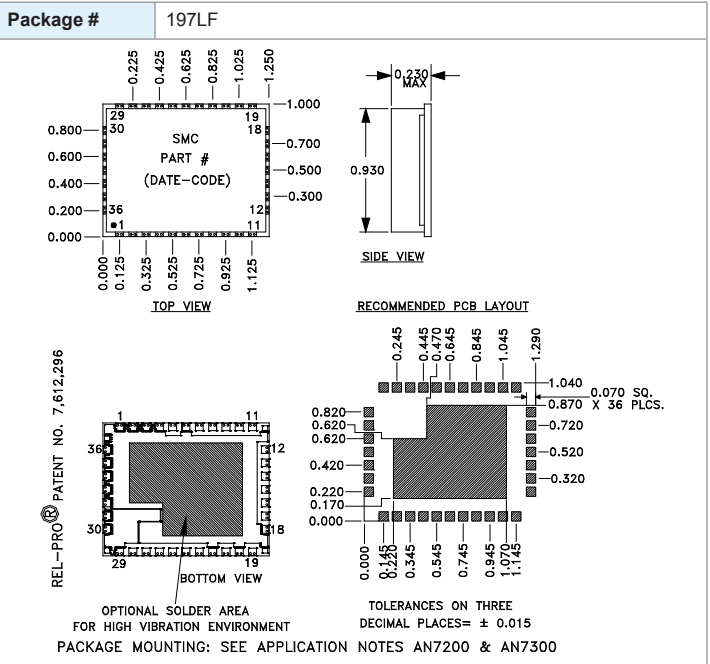
**FEATURES:**

- ▶ Exceptionally Low Phase Noise
- ▶ Interactive Communication
- ▶ Standard Programming Interface
- ▶ Ultra Wide Tuning Range
- ▶ Lead Free - RoHS Compliant
- ▶ Patented REL-PRO® Technology
- ▶ Small Size, Surface Mount
- ▶ Buffered Output



**SPECIFICATIONS (Rev. E 01/25/13)**

Frequency	1680 - 2360 MHz		
Step Size	1000 kHz		
Reference Input Frequency	10 MHz		
Reference Input Voltage	1 V p-p to 3.3 V p-p		
Bias Voltage	Vcc	V (Vdc)	I (mA Max.)
	Digital	+5	45
	VCO	+8	35
	Converter	+8	30
Output Power	+5 dBm (Min.)		
Spurious Suppression	70 dB (Typ.)		
Harmonic Suppression	16 dB (Typ.)		
Settling Time	10 mSec (Typ.) <sup>1</sup>		
Output Impedance	50 Ohms (Nom.)		
Lock Detect Indicator	CMOS 3.3 V		
Typical Phase Noise	Offset	Phase Noise	
	@ 1 kHz	-102 dBc/Hz	
	@ 10 kHz	-102 dBc/Hz	
	@ 100 kHz	-117 dBc/Hz	
Operating Temperature Range	-40 to +85 °C		
Programming	See Application Note: AN7100		
<sup>1</sup> From the rising edge of LE to stable lock detect			



**Absolute Maximum Ratings**

Storage Temp. Range	-55 to +125 °C
Bias Voltage (Digital)	+5.25 V
Bias Voltage (VCO)	+8.5 V
Bias Voltage (Converter)	+10 V
DC Voltage Applied to RF Out	±25 V

**Patent :** <http://www.synergymwave.com/patents>

Port Configuration		
Pin 5 - RF out	Pin 21 - Ref. In	Pin 8,12,14,15,17 - NC
Pin 7 - Lock Detect Out *	Pin 23 - Vcc (Digital)	All Others - Ground
Pin 9 - Data In	Pin 24 - Vtune (Output)	
Pin 10 - Error Flag	Pin 25 - Vcc (VCO)	NC - No Connection
Pin 11 - Clock In	Pin 26 - Vout (Converter) ***	
Pin 13 - VCO (On/Off)****	Pin 27 - Vcc (Tune) ***	
Pin 19 - Latch Enable In	Pin 28 - Vcc (Converter)	

\* High when locked (source/sink 500 uA)  
 \*\*\* Connect externally. Bypassed with a 10uF 35V tantalum capacitor.  
 \*\*\*\* NC if unused.

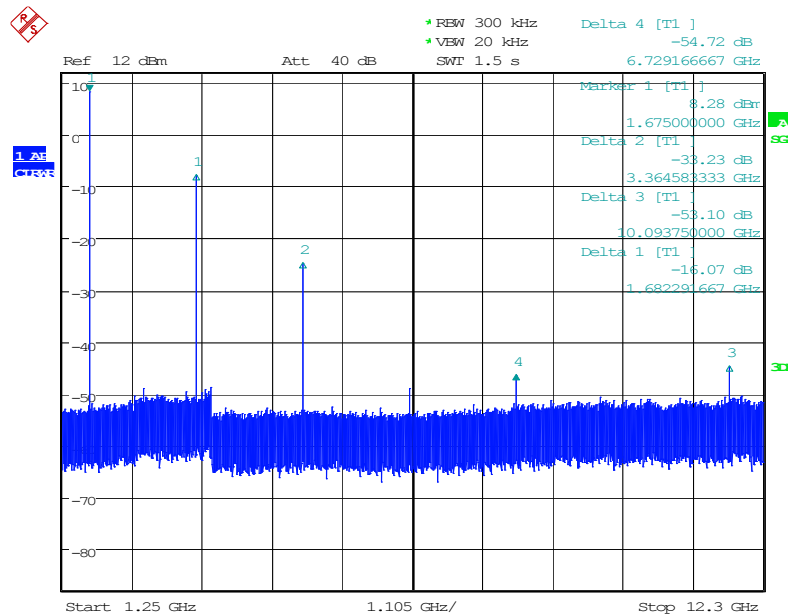
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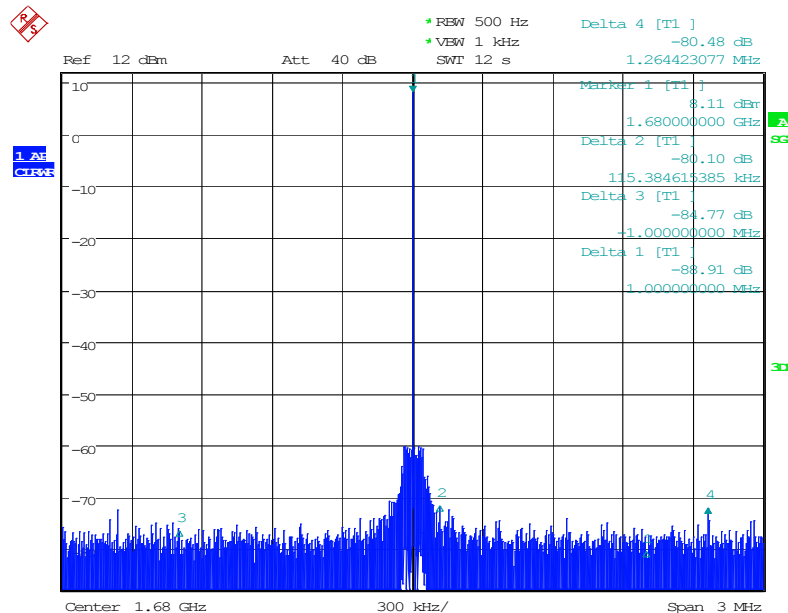
OPTIMIZED BANDWIDTH

1680 - 2360 MHz

### HARMONIC SUPPRESSION



### REFERENCE SIDEBAND SUPPRESSION



PERFORMANCE PLOTS

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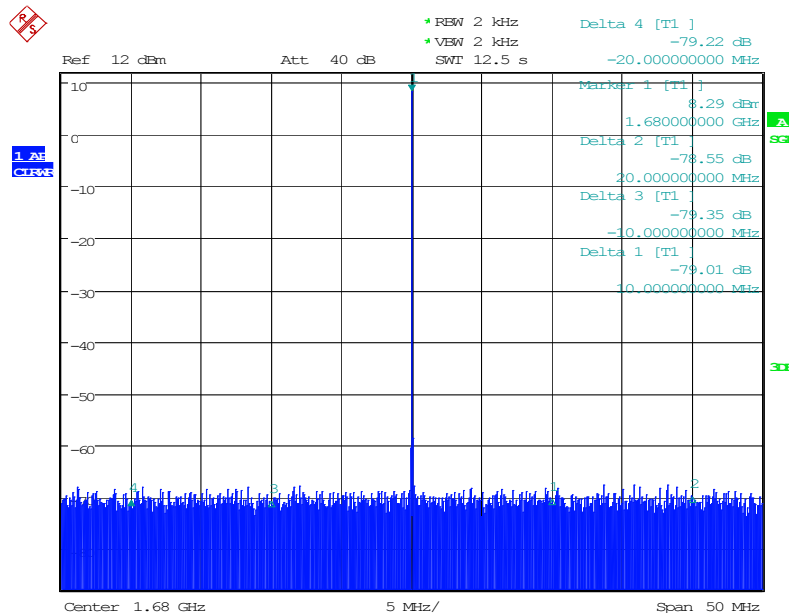
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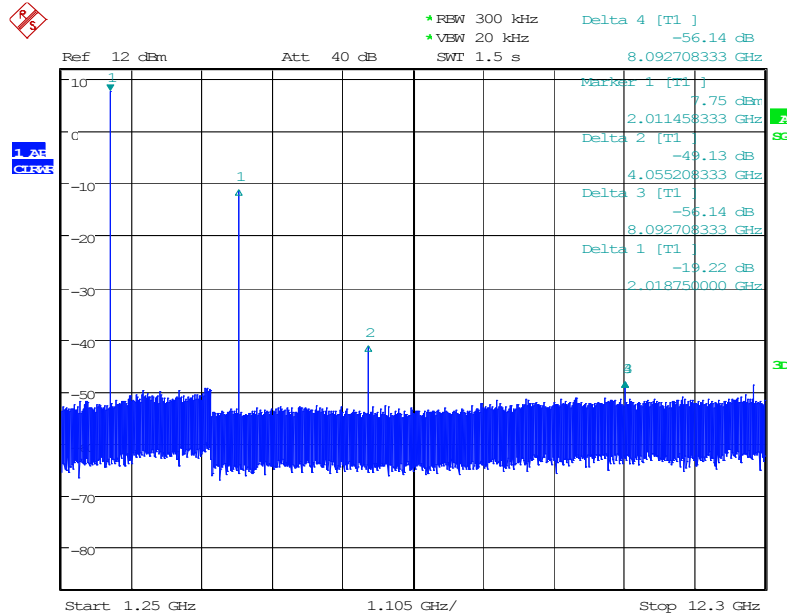
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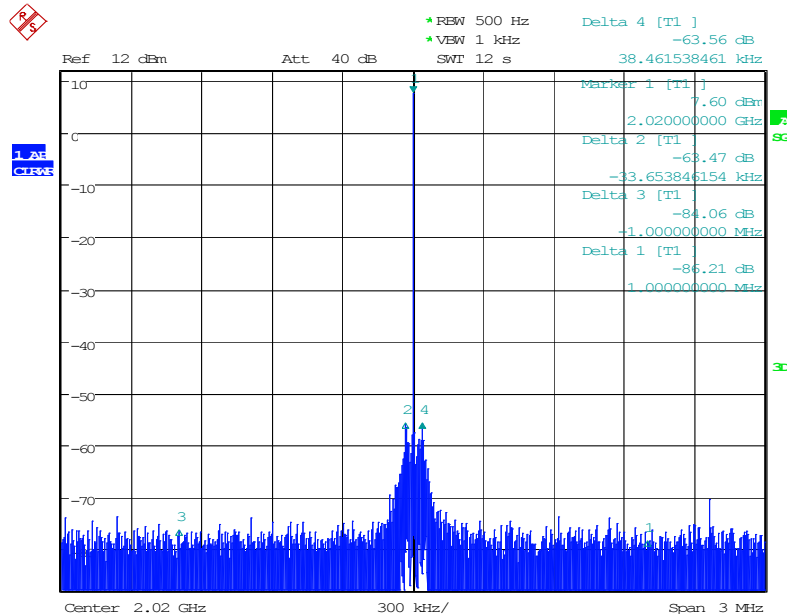
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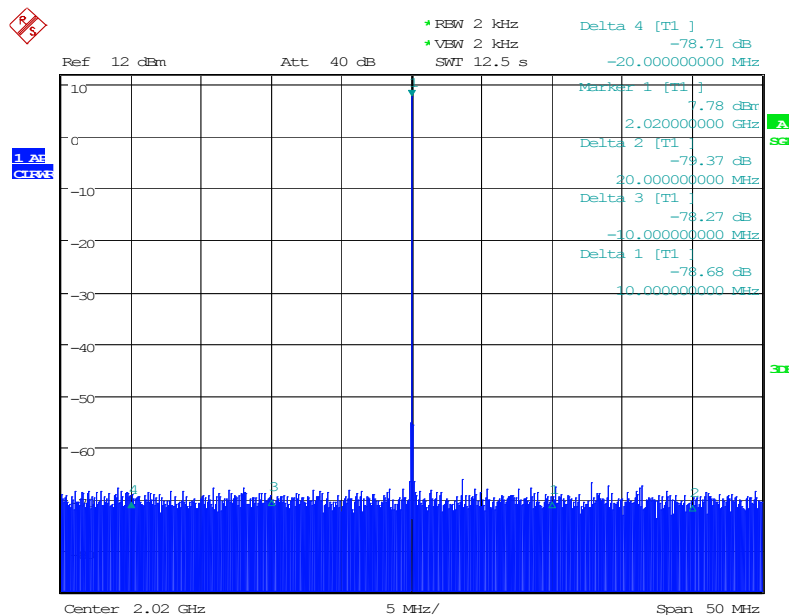
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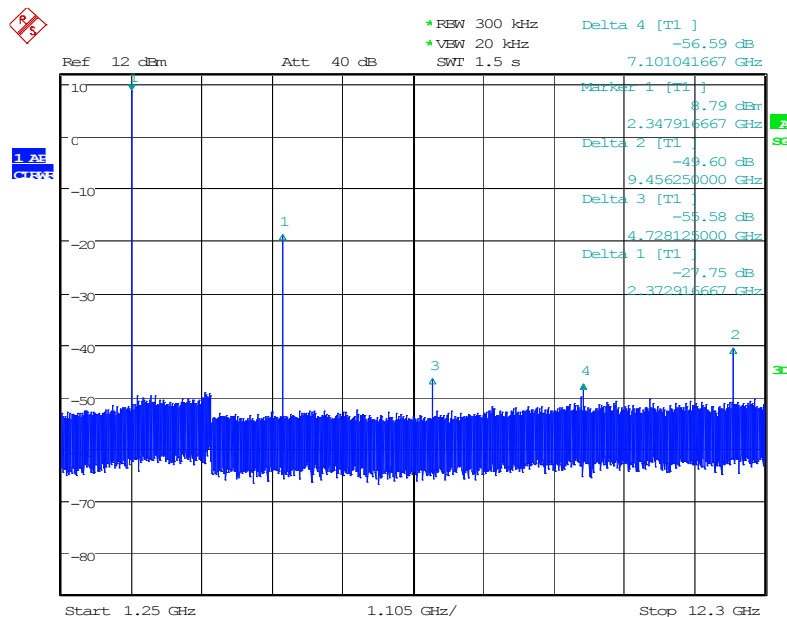
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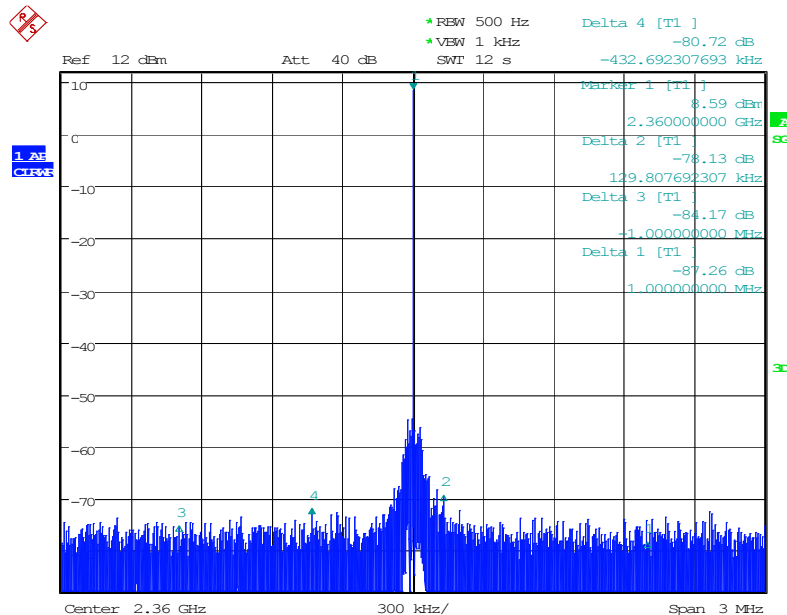
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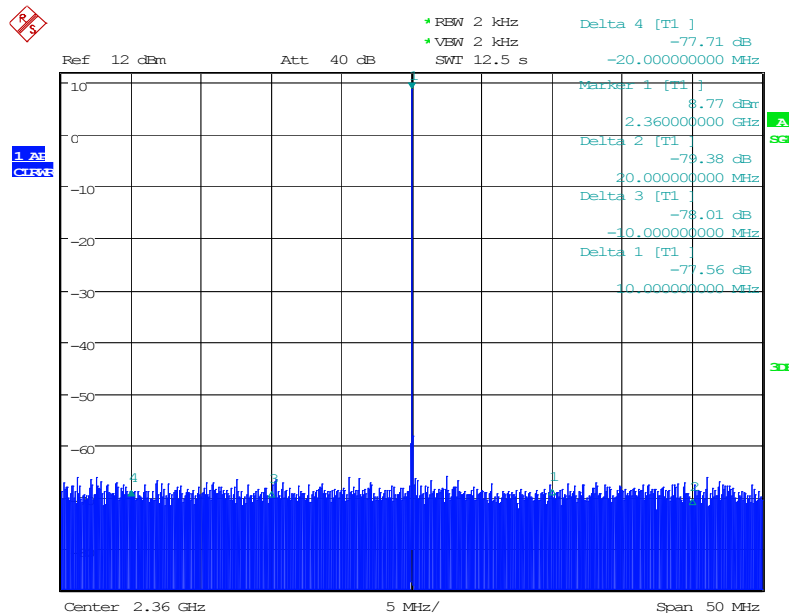
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