

## Supply Voltage Supervisor w/Watchdog Input and Manual Reset

**UM706xS SOP8**  
**UM708xS SOP8**

### General Description

The UM706xS/UM708xS series are cost effective system power supply supervisory circuits designed to monitor the power supplies in digital systems.

The UM706xS provides power-supply monitoring circuitry that generates a reset output during power-up, power-down, and brownout conditions. The reset output remains operational with  $V_{CC}$  as low as 1V. Independent watchdog monitoring circuitry is also provided. This is activated if the watchdog input has not been toggled within 1.6 seconds. In addition, there is a 1.25V threshold detector for power-fail warning, low battery detection, or to monitor an additional power supply. An active low debounced manual reset input is also included.

The UM708xS is the same as the UM706xS, except an active-high reset is substituted for the watchdog timer. All parts are available in a small outline SOP8 package.

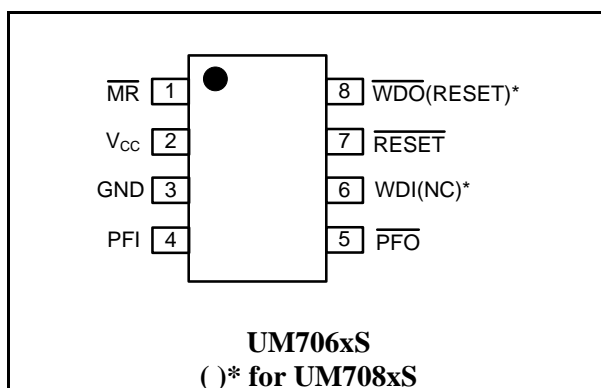
### Applications

- Applications using DSPs, Microcontrollers or Microprocessors
- Programmable Controls
- Computers
- Embedded System
- Industrial Equipments
- Intelligent Instrument
- Wireless Communications Systems

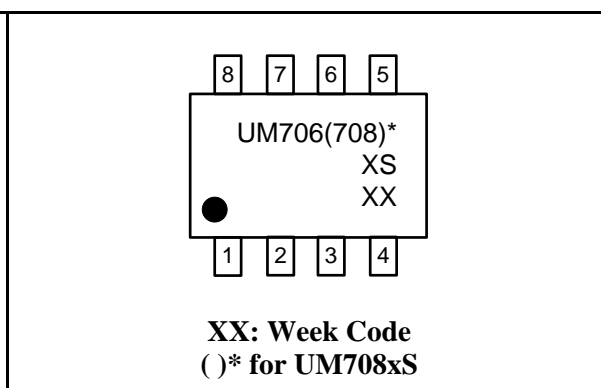
### Features

- Wide Operation Voltage Range of 1V to 5.5V
- Correct Logic Output Guaranteed to  $V_{CC}=1.0V$
- Precision Supply-Voltage Monitor: 2.63V, 2.93V, 3.08V, 4.38V, 4.63V
- 200ms Reset Pulse Width
- Independent Watchdog Timer-1.6s Timeout (UM706xS)
- Active-high Reset Output (UM708xS)
- Voltage Monitor for Power-Fail or Low-Battery Warning
- Temperature Range: -40 °C to +85 °C
- Supply Current of 80 $\mu$ A (Typ.)

### Pin Configurations



### Top View



## Ordering Information

Part Number	Top Marking	RESET Threshold (V)	Timeout Period (ms)	Package Type
UM706LS	UM706LS	4.63	240	SOP8
UM706MS	UM706MS	4.38	240	
UM706TS	UM706TS	3.08	240	
UM706SS	UM706SS	2.93	240	
UM706RS	UM706RS	2.63	240	
UM708LS	UM708LS	4.63	240	
UM708MS	UM708MS	4.38	240	
UM708TS	UM708TS	3.08	240	
UM708SS	UM708SS	2.93	240	
UM708RS	UM708RS	2.63	240	

## Typical Application Circuit

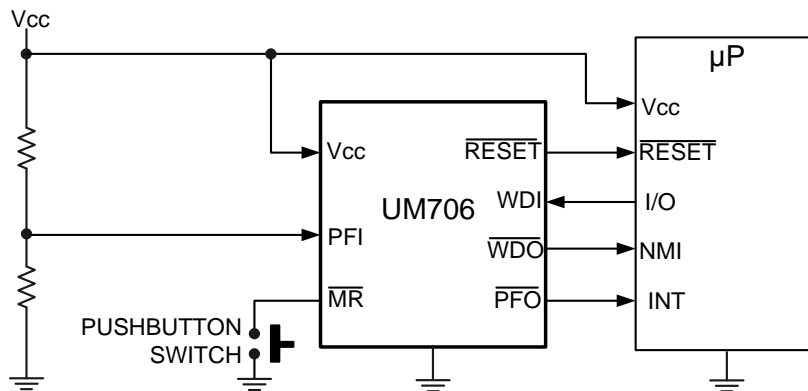


Figure 1. UM706xS Application Circuit

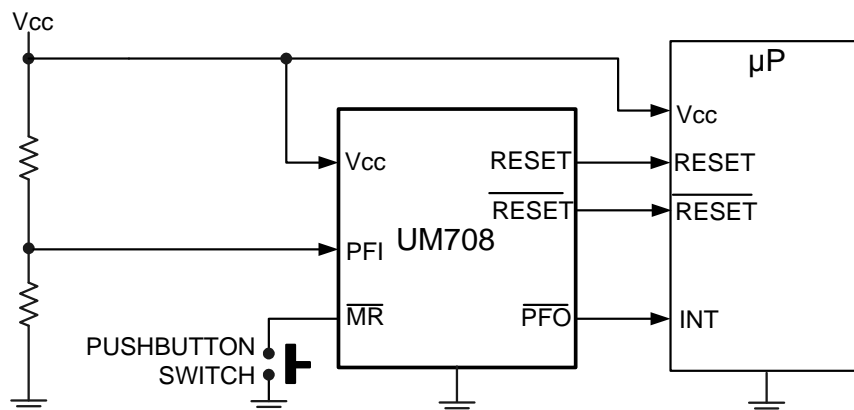


Figure 2. UM708xS Application Circuit

## Pin Description

Pin Number	Pin Name		Function
1	$\overline{\text{MR}}$		Manual-Reset Input triggers a reset pulse when pulled below 0.8V. This active-low input has an internal 250 $\mu$ A pull-up current. It can be driven from a TTL or CMOS logic line as well as shorted to ground with a switch.
2	$V_{\text{CC}}$		Supply Input
3	GND		Ground Reference for all signals.
4	PFI		Power-Fail Voltage Monitor Input. When PFI is less than 1.25V, $\overline{\text{PFO}}$ goes low. Connect PFI to GND or $V_{\text{CC}}$ when not used.
5	$\overline{\text{PFO}}$		Power-Fail Output goes low and sinks current when PFI is less than 1.25V; otherwise $\overline{\text{PFO}}$ stays high.
6	UM706	WDI	Watchdog Input. If WDI remains either high or low for longer than the watchdog timeout period, the $\overline{\text{WDO}}$ goes low. The timer resets with each transition at the WDI input. Either a high-to-low or a low-to-high transition clears the counter. The internal timer is also cleared whenever reset is asserted.
	UM708	NC	No Connect
7	$\overline{\text{RESET}}$		Active-Low Reset Output pulses low for 200ms when triggered, and stays low whenever $V_{\text{CC}}$ is below the reset threshold. It remains low for 200ms after $V_{\text{CC}}$ rises above the reset threshold or $\overline{\text{MR}}$ goes from Low to High.
8	UM706	$\overline{\text{WDO}}$	Watchdog Output pulls low when the internal watchdog timer finishes its 1.6sec count and does not go high again until the watchdog is cleared. $\overline{\text{WDO}}$ also goes low during low-line conditions. Whenever $V_{\text{CC}}$ is below the reset threshold, $\overline{\text{WDO}}$ stays low; however, unlike $\overline{\text{RESET}}$ , $\overline{\text{WDO}}$ does not have a minimum pulse width. As soon as $V_{\text{CC}}$ rises above the reset threshold, $\overline{\text{WDO}}$ goes high with no delay.
	UM708	RESET	Active-High Reset Output is the inverse of $\overline{\text{RESET}}$ . Whenever RESET is high, $\overline{\text{RESET}}$ is low, and vice versa.

## Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply Voltage	-0.3 to +6.0	V
	RESET, $\overline{\text{RESET}}$ (push-pull)	-0.3 to V <sub>CC</sub> +0.3	V
I <sub>CC</sub>	Input Current, V <sub>CC</sub>	20	mA
I <sub>O</sub>	Output Current, RESET, $\overline{\text{RESET}}$	20	mA
	Rate of Rise, V <sub>CC</sub>	100	V/μs
P <sub>D</sub>	Continuous Power Dissipation	471	mW
T <sub>J</sub>	Operating Junction Temperature	-40 to +105	°C
T <sub>STG</sub>	Storage Temperature Range	-65 to +150	°C
	Lead Temperature (soldering, 10s)	300	°C

Note 1: Stresses beyond those listed under “Absolute maximum Ratings” may cause permanent damage to the device.

## Electrical Characteristics

V<sub>CC</sub> = full range, T<sub>A</sub> = -40 °C to +85 °C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25 °C, V<sub>CC</sub> = 5V for L/M versions, V<sub>CC</sub> = 3.3V for T/S versions, and V<sub>CC</sub> = 3V for R version. (Note 2)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit	
V <sub>CC</sub>	V <sub>CC</sub> Range	T <sub>A</sub> =0°C to +70°C	1.0		5.5	V	
		T <sub>A</sub> =-40°C to +85°C	1.2		5.5		
I <sub>CC</sub>	Supply Current	T <sub>A</sub> =-40°C to +85°C		80	150	μA	
V <sub>TH</sub>	Reset Threshold	UM706L/ UM708L	T <sub>A</sub> =+25°C	4.56	4.63	4.70	V
			T <sub>A</sub> =-40°C to +85°C	4.50		4.75	
		UM706M/ UM708M	T <sub>A</sub> =+25°C	4.31	4.38	4.45	
			T <sub>A</sub> =-40°C to +85°C	4.25		4.50	
		UM706T/ UM708T	T <sub>A</sub> =+25°C	3.04	3.08	3.11	
			T <sub>A</sub> =-40°C to +85°C	3.00		3.15	
		UM706S/ UM708S	T <sub>A</sub> =+25°C	2.89	2.93	2.96	
			T <sub>A</sub> =-40°C to +85°C	2.85		3.00	
	Reset Threshold Hysteresis			40		mV	
t <sub>RS</sub>	Reset Pulse Width		140	200	280	ms	

Note 2: Production testing done at T<sub>A</sub> = +25 °C; limits over temperature guaranteed by design only.

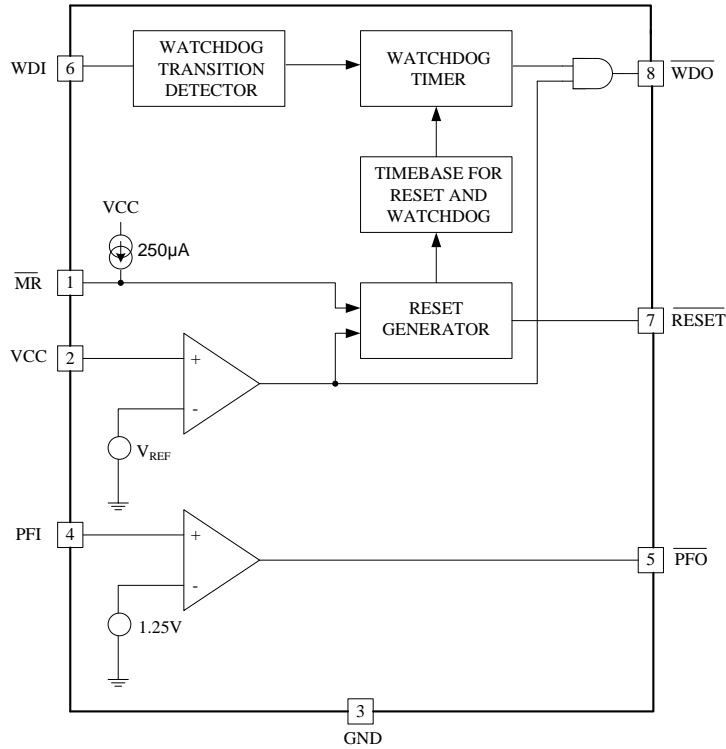
## Electrical Characteristics (Continued)

$V_{CC}$  = full range,  $T_A$  = -40 °C to +85 °C, unless otherwise noted. Typical values are at  $T_A$  = +25 °C,  $V_{CC}$  = 5V for L/M versions,  $V_{CC}$  = 3.3V for T/S versions, and  $V_{CC}$  = 3V for R version. (Note 2)

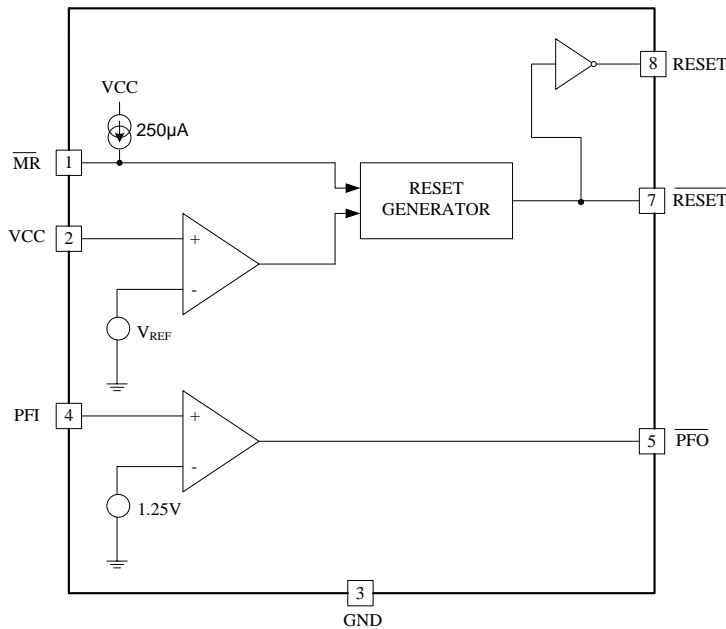
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{OL}$	RESET / $\overline{\text{RESET}}$ Output Voltage Low	$I_{SINK}=1.2\text{mA}$ , (for R/S/T versions)			0.3	V
		$I_{SINK}=3.2\text{mA}$ , (for L/M versions)			0.4	
		$V_{CC} = 1.2\text{V}$ , $I_{SINK} = 100\mu\text{A}$			0.3	
$V_{OH}$	RESET/ $\overline{\text{RESET}}$ Output Voltage High	$I_{SOURCE} = 800\mu\text{A}$	$V_{CC}-1.5$			V
	MR Pull-Up Current	$\overline{\text{MR}}=0\text{V}$	100	250	600	$\mu\text{A}$
$t_{MR}$	$\overline{\text{MR}}$ Pulse Width		150			ns
	MR Input Threshold, Low				0.8	V
	MR Input Threshold, High		2.0			V
$t_{MD}$	$\overline{\text{MR}}$ to Reset Out Delay				250	ns
	PFI Input Threshold	$V_{CC}=5\text{V}$	1.20	1.25	1.30	V
	PFI Input Current		-25	0.01	+25	nA
	$\overline{\text{PFO}}$ Output Voltage	$I_{SOURCE}=800\mu\text{A}$	$V_{CC}-1.5$			V
		$I_{SINK}=3.2\text{mA}$			0.4	
<b>Watchdog function for UM706</b>						
$t_{WD}$	Watchdog Timeout Period		1.0	1.6	2.25	s
$t_{WP}$	WDI Pulse Width	$V_{IL}=0.4\text{V}, V_{IH}=0.8V_{CC}$	50			ns
	WDI Input Threshold Low	$V_{CC}=5\text{V}$			0.8	V
	WDI Input Threshold High	$V_{CC}=5\text{V}$	3.5			V
	WDI Input Current	$\text{WDI}=V_{CC}$		50	150	$\mu\text{A}$
		$\text{WDI}=0\text{V}$	-150	-50		
	WDO Output Voltage High	$I_{SOURCE}=800\mu\text{A}$	$V_{CC}-1.5$			V
	WDO Output Voltage Low	$I_{SINK}=1.2\text{mA}$			0.4	V

Note 2: Production testing done at  $T_A$  = +25 °C; limits over temperature guaranteed by design only.

## Block Diagram



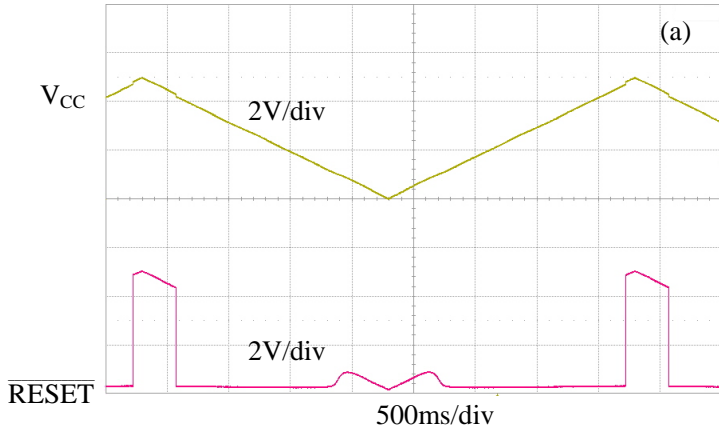
**Figure 3. UM706xS Block Diagram**



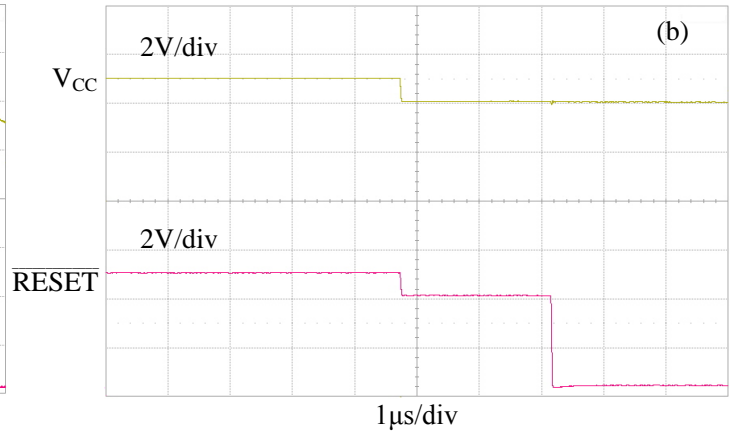
**Figure 4. UM708xS Block Diagram**

## Typical Operating Characteristics

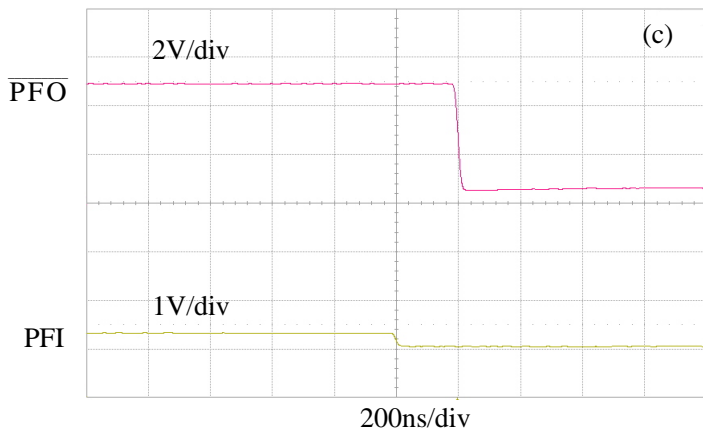
### RESET Output Voltage vs. Supply Voltage



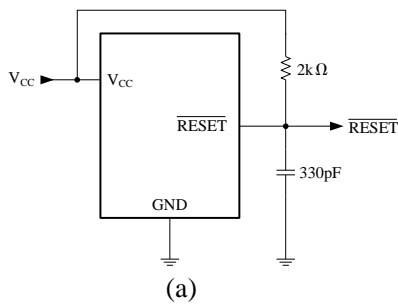
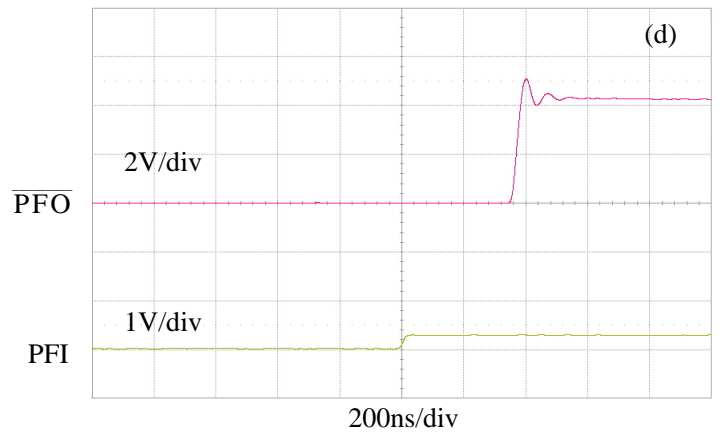
### RESET Response Time



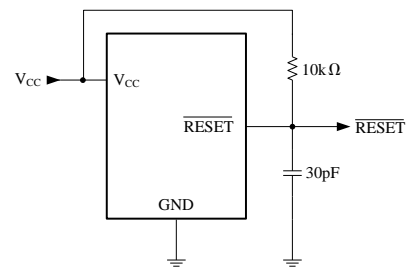
### Power-fail Comparator Assertion Response Time



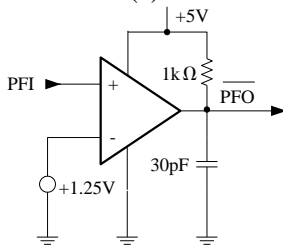
### Power-fail Comparator De-assertion Response Time



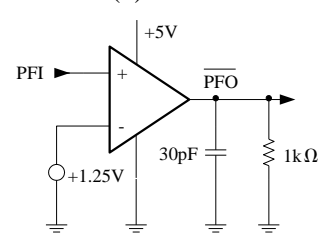
(a)



(b)



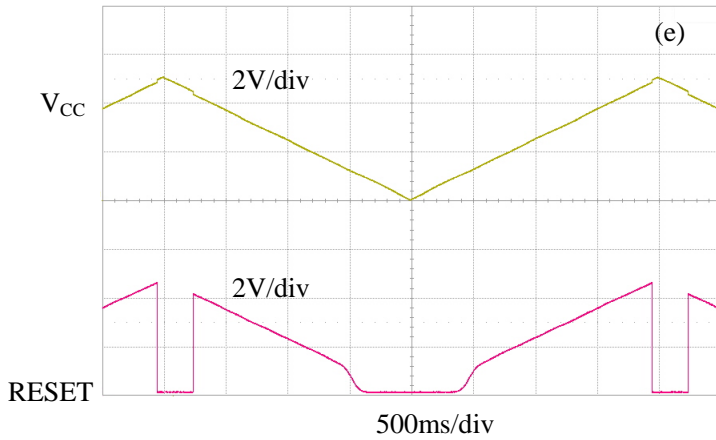
(c)



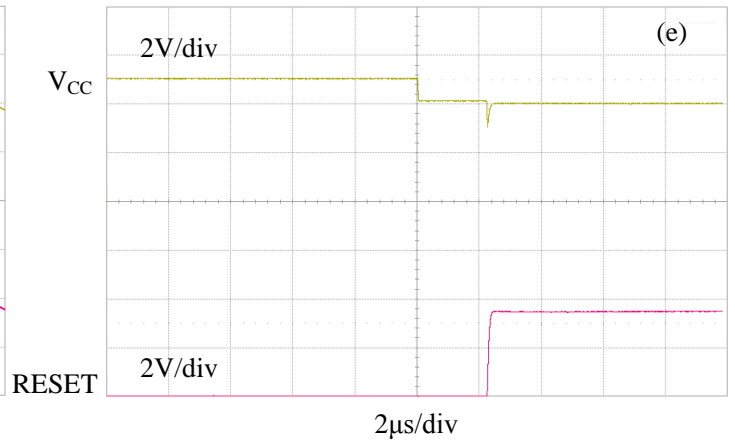
(d)

## Typical Operating Characteristics

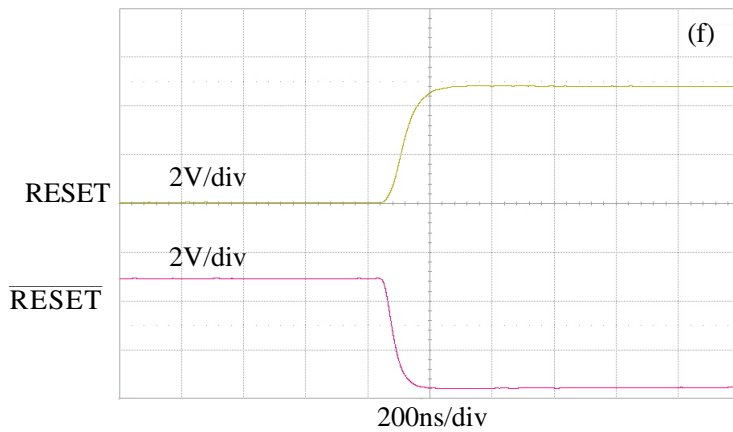
### RESET Output Voltage vs. Supply Voltage



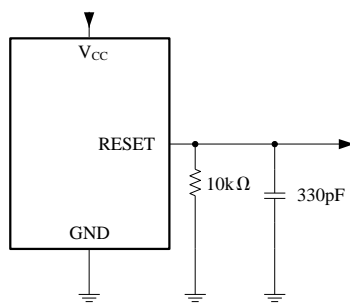
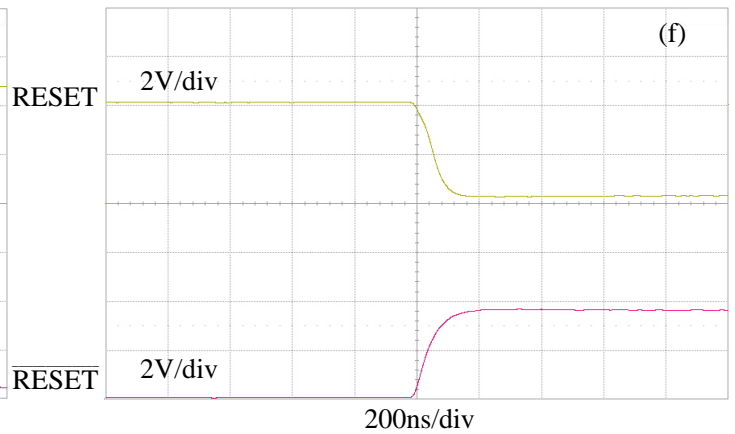
### RESET Response Time



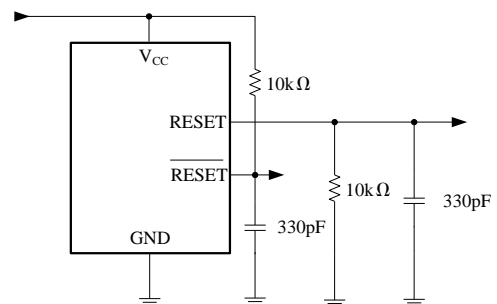
### RESET, $\overline{\text{RESET}}$ Assertion



### RESET, $\overline{\text{RESET}}$ De-assertion



(e)



(f)



## Detailed Description

### Power-Fail Reset

The reset output provides a reset signal to the microprocessor whenever the  $V_{CC}$  input is below the threshold. An internal timer holds the reset output active for 200ms after the voltage on  $V_{CC}$  rises above the threshold. This is intended as a power-on reset signal for the microprocessor. It allows time for both the power supply and the microprocessor to stabilize after power-up. If a power supply brownout or interruption occurs, the reset line is similarly activated and remains active for 200ms after the supply recovers. If another interruption occurs during an active reset period, the reset timeout period continues for an additional 200ms.

The reset output is guaranteed to remain valid with  $V_{CC}$  as low as 1V. This ensures that the microprocessor is held in a stable shutdown condition as the power supply starts up.

The UM706xS provides an active low  $\overline{\text{RESET}}$  signal while the UM708xS provides an active high RESET signal as well as active low  $\overline{\text{RESET}}$  signal.

### Power-Fail Comparator

The power-fail comparator can be used for various purposes because its output and non-inverting input are not internally connected. The inverting input is internally connected to a 1.25V reference.

To build an early-warning circuit for power failure, connect the PFI pin to a voltage divider, choose the voltage divider ratio so that the voltage at PFI falls below 1.25V just before the regulator drops out. Use  $\overline{\text{PFO}}$  to interrupt the  $\mu\text{P}$  so it can prepare for an orderly power-down.

### Manual Reset

The Manual-Reset input ( $\overline{\text{MR}}$ ) allows reset to be triggered by a pushbutton switch. The switch is effectively debounced by the 140ms minimum reset pulse width.  $\overline{\text{MR}}$  is TTL/CMOS logic compatible, so it can be driven by an external logic line. If unused,  $\overline{\text{MR}}$  input can be tied high or left floating.

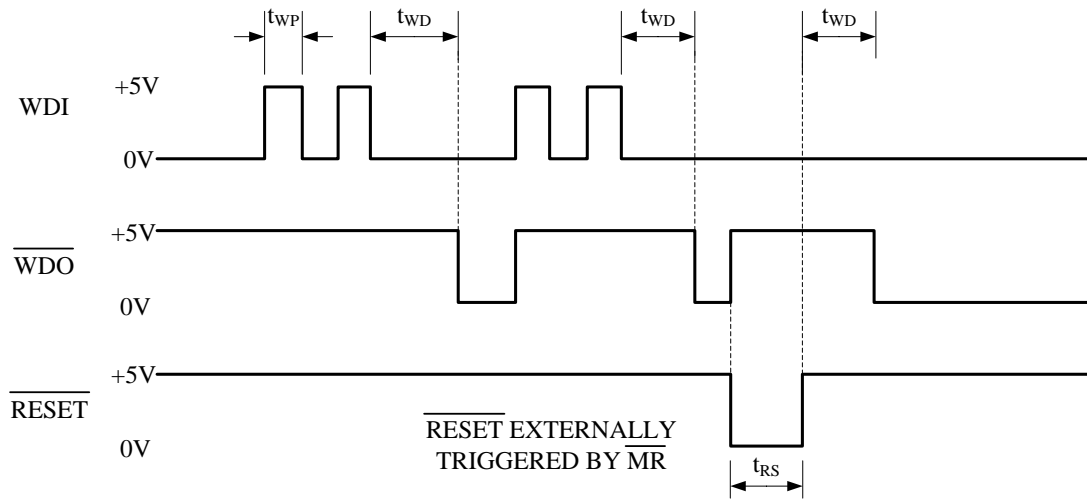
### Watchdog Timer

The UM706xS watchdog timer circuit is used to monitor the activity of the microprocessor to check that it is not stalled in an indefinite loop. An output line on the processor is used to toggle the watchdog input (WDI). If this line is not toggled within 1.6sec,  $\overline{\text{WDO}}$  goes low.  $\overline{\text{WDO}}$  is connected to the non-maskable interrupt input (NMI) of a  $\mu\text{P}$ . Therefore, if the watchdog timer times out, an interrupt is generated. The interrupt service routine is used to rectify the problem.

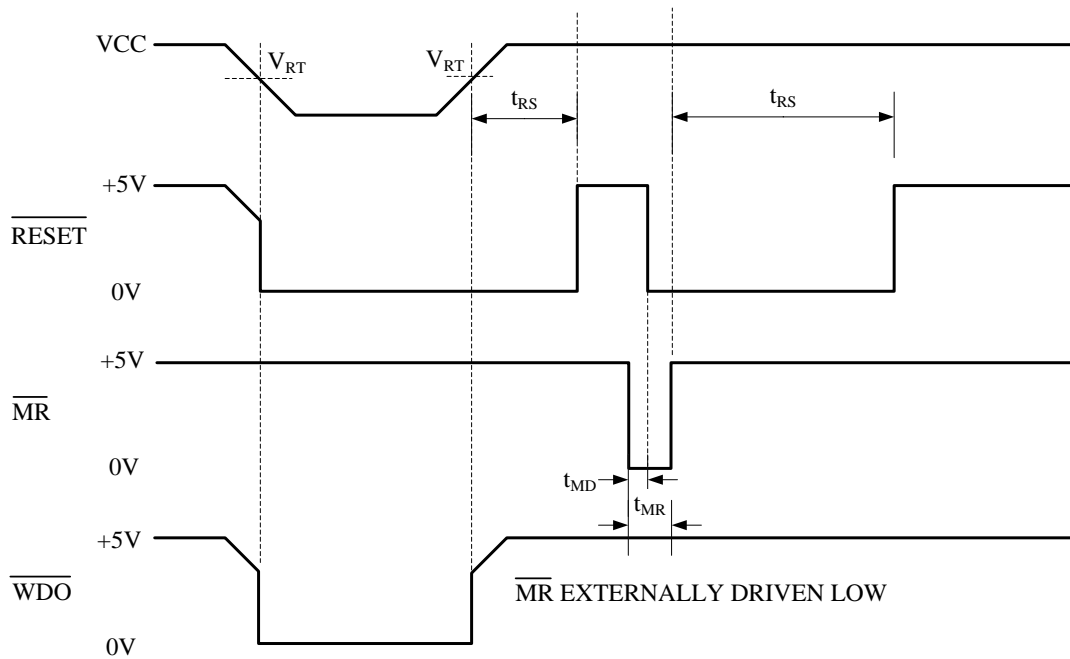
The watchdog timer is cleared either by a high-to-low or by a low-to-high transition on WDI.

Pulses as narrow as 50ns are detected. The timer is also cleared by  $\overline{\text{RESET}}/\overline{\text{RESET}}$  going active. Therefore, the watchdog timeout period begins after reset goes inactive.

When  $V_{CC}$  falls below the reset threshold,  $\overline{\text{WDO}}$  is forced low whether or not the watchdog timer has timed out. Normally, this generates an interrupt, but it is overridden by  $\overline{\text{RESET}}/\overline{\text{RESET}}$  going active.



**Figure 5. Watchdog and Reset Timing**



**Figure 6. Reset, Manual Reset and Watchdog Timing**

## Applications Information

### Valid $\overline{\text{RESET}}$ below 1V $V_{CC}$

The UM706xS/UM708xS are guaranteed to provide a valid reset level with  $V_{CC}$  as low as 1V. When  $V_{CC}$  falls below 1V, the internal transistor does not have sufficient drive to hold it on so the voltage on  $\overline{\text{RESET}}$  is no longer held at 0V. If a pull-down resistor is added to the  $\overline{\text{RESET}}$  pin as shown in Figure 7, any stray charge or leakage current will be drained to ground, holding  $\overline{\text{RESET}}$  low. Resistor value (R1) is not critical. It should be about 100k $\Omega$ , large enough not to load  $\overline{\text{RESET}}$  and small enough to pull  $\overline{\text{RESET}}$  to ground.

### Monitoring Additional Supply Levels

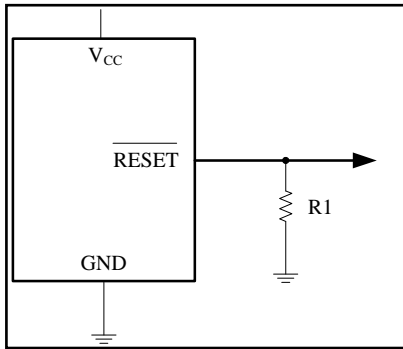
It is possible to use the power-fail comparator to monitor a second supply as shown in figure 8. The two sensing resistors, R1 and R2, are selected such that the voltage on PFI drops below 1.25V at the minimum acceptable input supply. The  $\overline{\text{PFO}}$  output can be connected to the  $\overline{\text{MR}}$  input so that a reset is generated when the supply drops out of tolerance. In this case, if either supply drops out of tolerance, a reset is generated.

### Monitoring a Negative Voltage

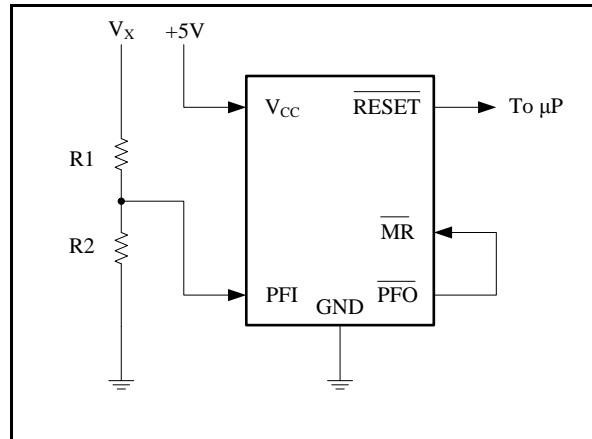
The power-fail comparator can also monitor a negative supply rail (Figure 9). When the negative rail is good (a negative voltage of large magnitude),  $\overline{\text{PFO}}$  is low, and when the negative rail is degraded (a negative voltage of lesser magnitude),  $\overline{\text{PFO}}$  is high. By adding the resistors and transistor as shown, a high  $\overline{\text{PFO}}$  triggers reset. As long as  $\overline{\text{PFO}}$  remains high, the UM706xS/UM708xS will keep reset asserted ( $\overline{\text{RESET}}$  = low, RESET = high). Note that this circuit's accuracy depends on the PFI threshold tolerance, the  $V_{CC}$  line, and the resistors.

### Microprocessor with Bidirectional Reset

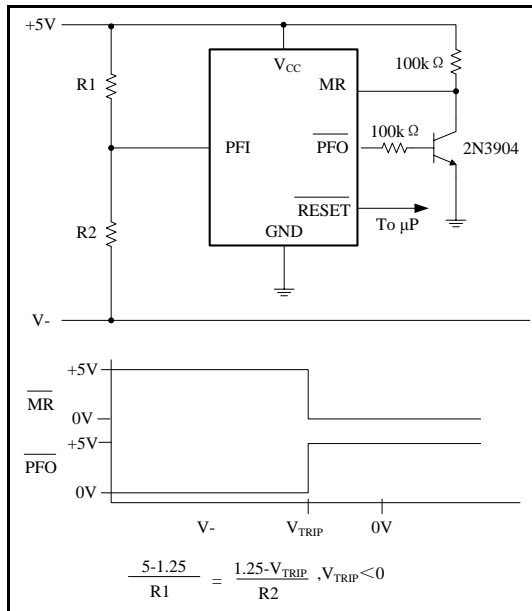
To prevent contention for microprocessors with a bidirectional reset line, a current limiting resistor is to be inserted between the  $\overline{\text{RESET}}$  output pin and the microprocessor reset pin. This limits the current to a safe level if there are conflicting output reset levels. A suitable resistor value is 4.7k $\Omega$ . If the reset output is required for other uses, it should be buffered as shown in figure 10.



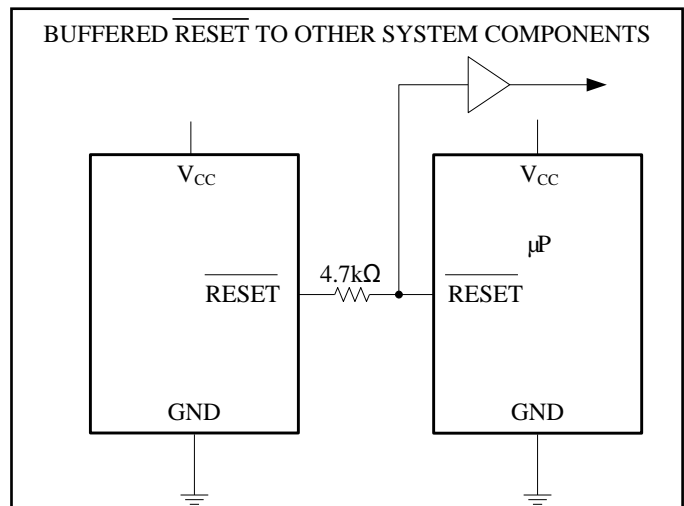
**Figure 7. Reset Valid to Ground Circuit**



**Figure 8. Monitoring an Additional Supply V<sub>x</sub>**



**Figure 9. Monitoring a Negative Voltage**

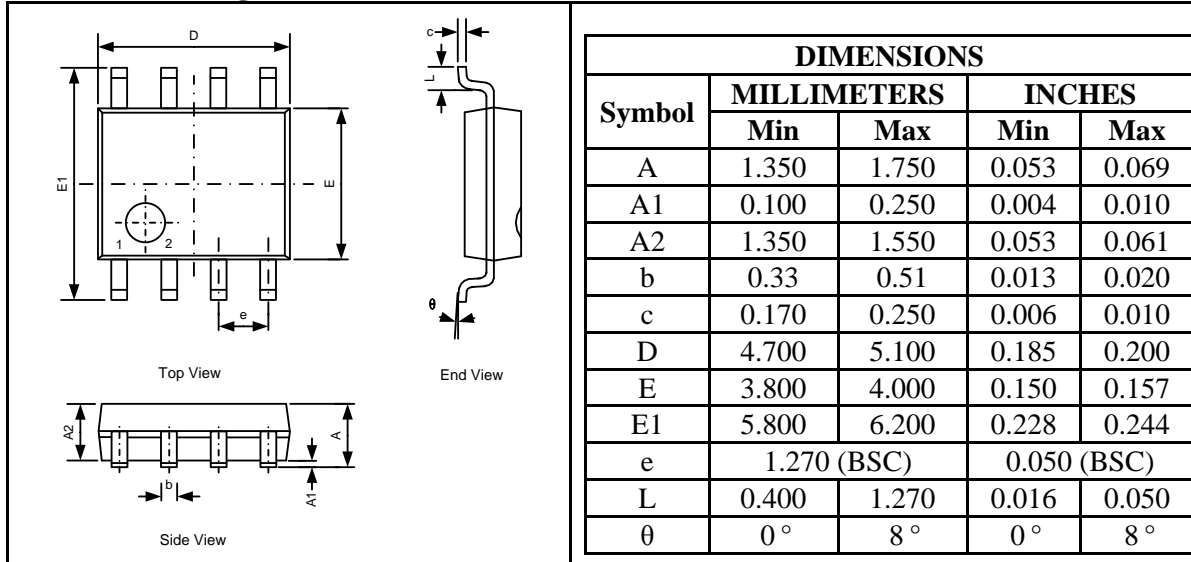


**Figure 10. Bidirectional Reset I/O**

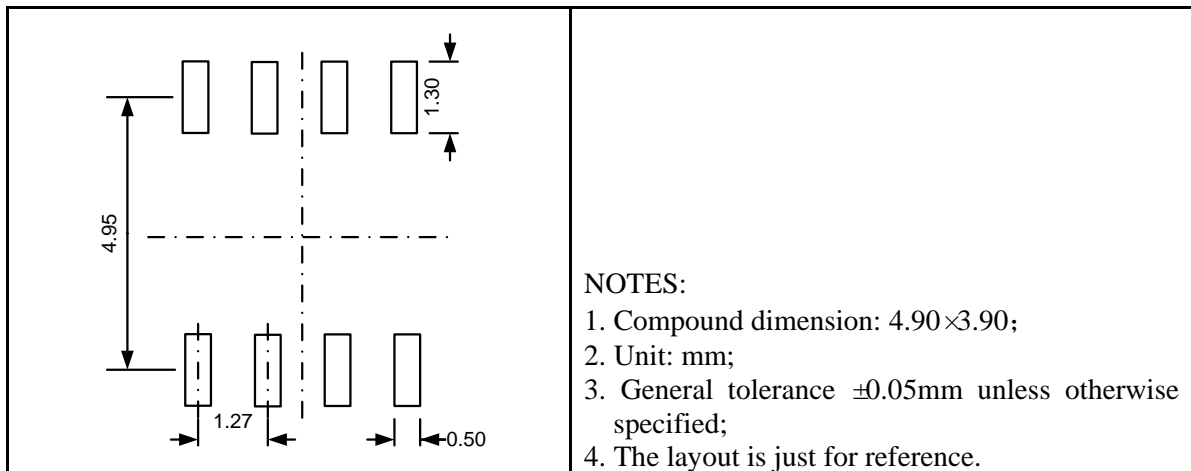
## Package Information

### UM706xS SOP8

#### Outline Drawing



#### Land Pattern

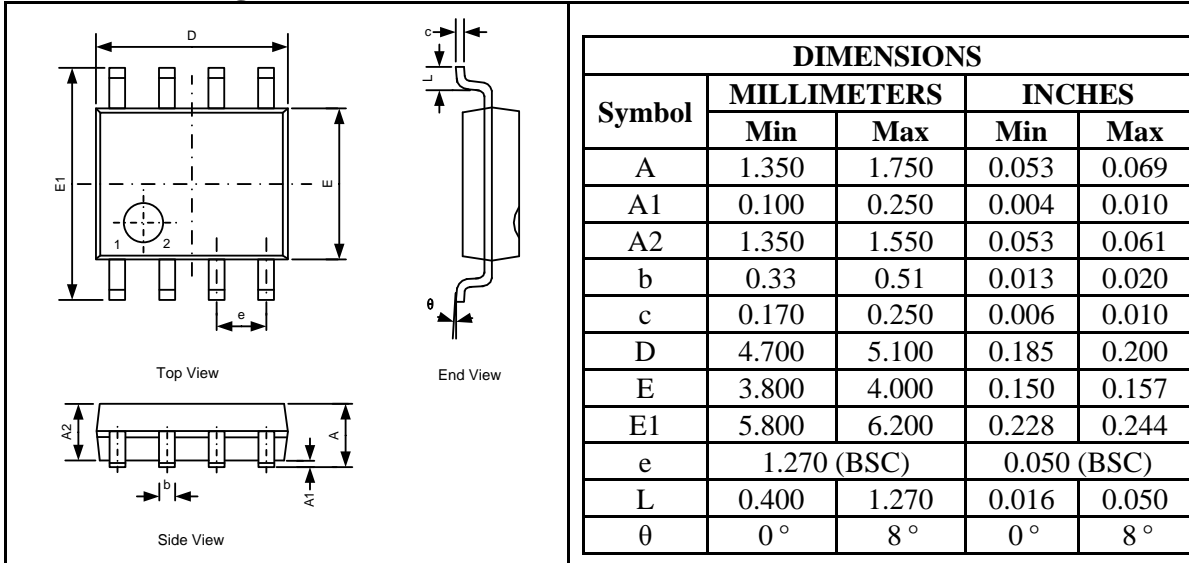


#### Tape and Reel Orientation

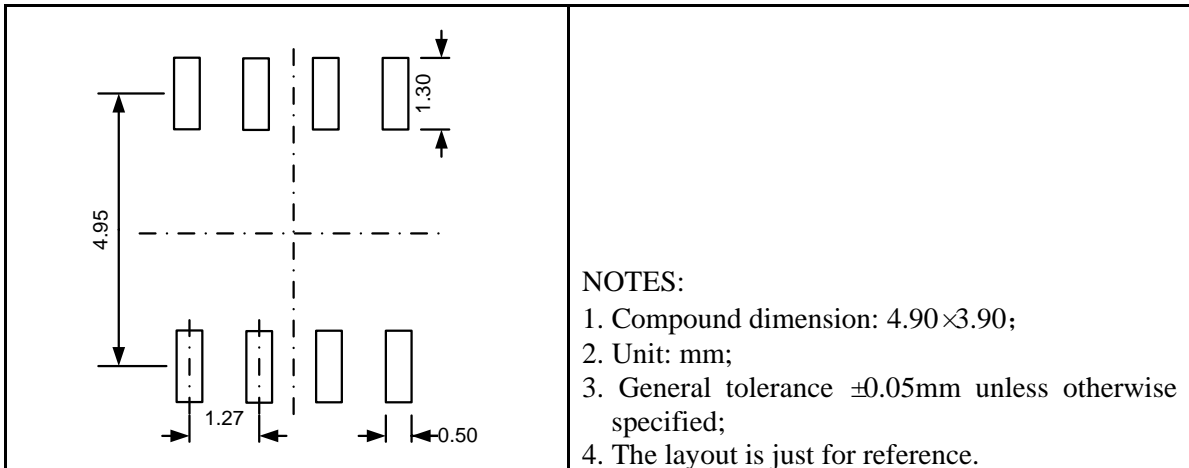


## UM708xS SOP8

### Outline Drawing



### Land Pattern



### Tape and Reel Orientation



## IMPORTANT NOTICE

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Union Semiconductor, Inc

Add: 2F, No. 3, Lane647 Songtao Road, Shanghai 201203

Tel: 021-51093966

Fax: 021-51026018

Website: [www.union-ic.com](http://www.union-ic.com)