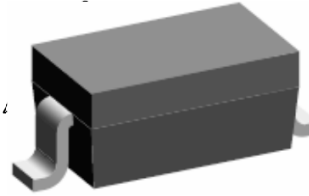


**Small Signal Product**

**Bi-directional TVS Diode Array**

**FEATURES**

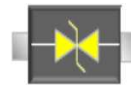
- Meet IEC61000-4-2 (ESD)  $\pm 15\text{kV}$  (air),  $\pm 8\text{kV}$  (contact)
- Meet IEC61000-4-4 (EFT) rating. 40A (5/50ns)
- Protects one Bi-directional I/O line
- Working Voltage : 24V
- Pb free version, RoHS compliant, and Halogen free



**MECHANICAL DATA**

- Case: SOD-323 small outline plastic package
- High temperature soldering guaranteed: 260°C/10s
- Weight: 48 $\pm$ 5 mg (approximately)
- Terminal : Matte tin plated, lead free, solderable per MIL-STD-202, method 208 guaranteed
- Mounting position : Any

**SOD-323**



**APPLICATION**

- Cell Phone Handsets and Accessories
- Notebooks, Desktops, and Servers
- Keypads, Side Keys
- Portable Instrumentation
- Microprocessor Based Equipment
- Peripherals

MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS (T <sub>A</sub> =25°C unless otherwise noted)			
PARAMETER	SYMBOL	VALUE	UNIT
IEC61000-4-2 ESD Voltage		Air model	$\pm 15$
		Contact Model	$\pm 8$
JESD22-A114-B ESD Voltage	V <sub>ESD</sub> (Note 1)	Per Human Body Model	-
ESD Voltage		Machine Model	-
Peak Pulse Power	P <sub>PP</sub> (Note 2)	500	W
Junction Temperature	T <sub>J</sub>	150	°C
Storage Temperature Range	T <sub>STG</sub>	-55 ~ 150	°C

Note 1: Device stressed with ten repetitive ESD pulses, per channel(I/O to GND)

PARAMETER	SYMBOL	VALUE		UNIT
		MIN	MAX	
Reverse Stand-Off Voltage	V <sub>RWM</sub> (Note 1)		24	V
Reverse Breakdown Voltage	I <sub>R</sub> = 1 mA V <sub>(BR)</sub>	26.7		V
Reverse Leakage Current	V <sub>R</sub> = 24 V I <sub>R</sub>		1	μA
Clamping Voltage	I <sub>PP</sub> = 5 A I <sub>PP</sub> = 17 A V <sub>C</sub> (Note 2)		40	V
			52	
Junction Capacitance	V <sub>R</sub> = 0 V , f = 1.0 MHz C <sub>J</sub>	50 (Typ.)		pF

Note 1: Other voltages available upon request

Note 2: Non-repetitive current pulse 8/20μs exponential decay waveform according to IEC61000-4-5

Note 3: Per channel(I/O to GND unless otherwise specified)

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RATINGS AND CHARACTERISTICS CURVES

(TA=25°C unless otherwise noted)

Fig. 1 Admissible Power Dissipation Curve

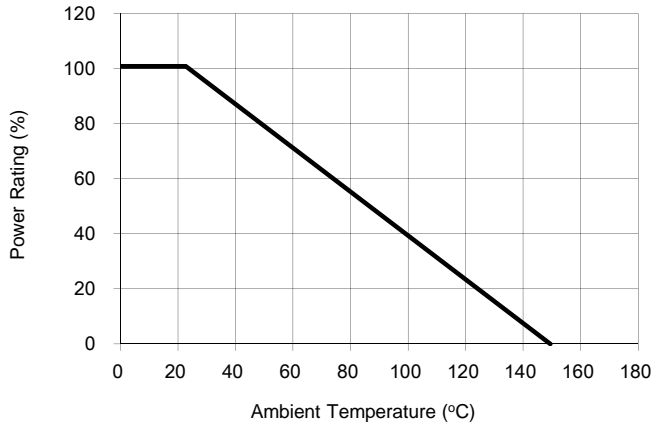


Fig. 2 Pulse Waveform

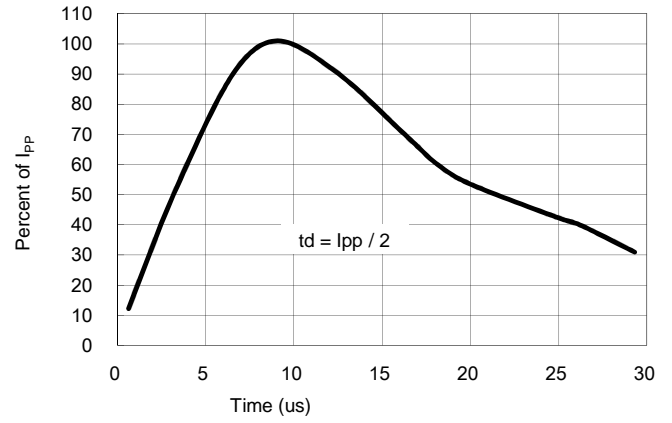


Fig. 3 Clamping Voltage VS. Peak Pulse Current

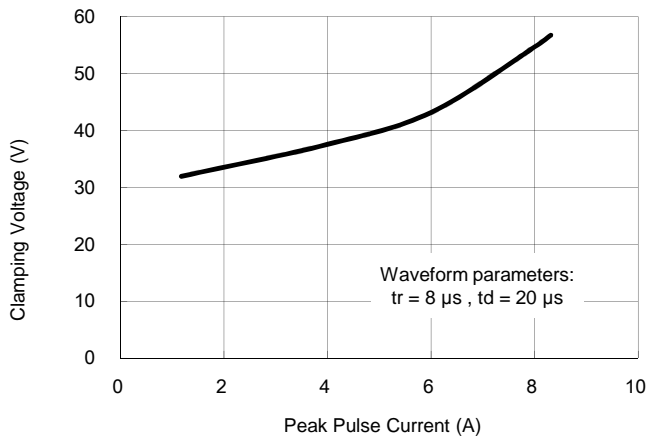


Fig. 4 Typical Junction Capacitance

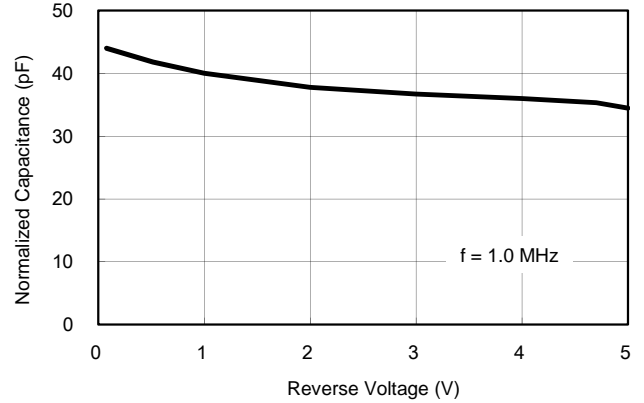
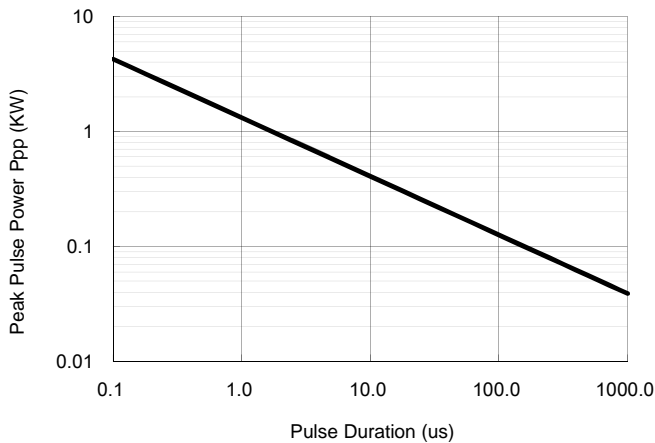


Fig. 5 Non-Repetitive Peak Pulse Power VS. Pulse Time



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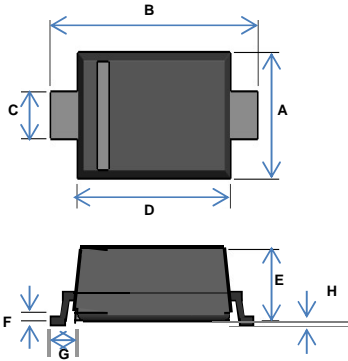
<b>ORDERING INFORMATION</b>						
<b>PART NO.</b>	<b>MANUFACTURE CODE (Note 1)</b>	<b>PACKING CODE</b>	<b>GREEN COMPOUND CODE</b>	<b>PACKAGE</b>	<b>PACKING</b>	<b>MARKING</b>
TESDC24V		RR	G	SOD-323	3K / 7" Reel	2H

Note 1: Indicator of manufacturing site for manufacture special control, if empty means no special control requirement

<b>EXAMPLE</b>					
<b>PREFERRED P/N</b>	<b>PART NO.</b>	<b>MANUFACTURE CODE</b>	<b>PACKING CODE</b>	<b>GREEN COMPOUND CODE</b>	<b>DESCRIPTION</b>
TESDC24V RRG	TESDC24V		RR	G	Green compound
TESDC24V-E0 RRG	TESDC24V	E0	RR	G	Green compound

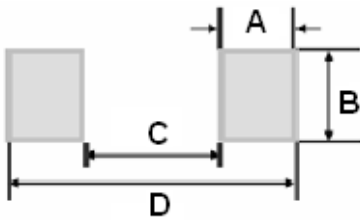
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### DIMENSIONS



DIM.	Unit (mm)		Unit (inch)	
	Min	Max	Min	Max
A	1.15	1.40	0.045	0.055
B	2.30	2.70	0.091	0.106
C	0.25	0.45	0.010	0.018
D	1.60	1.80	0.063	0.071
E	0.80	1.00	0.031	0.039
F	0.05	0.17	0.002	0.007
G	0.475 REF		0.19 REF	
H	-	0.10	-	0.004

### SUGGESTED PAD LAYOUT



DIM.	Unit (mm)		Unit (inch)	
	Typ.		Typ.	
A	0.63		0.025	
B	0.83		0.033	
C	1.60		0.063	
D	2.85		0.112	

### APPLICATION INFORMATION

- Designed to protect one data, I/O, or power supply line
- Designed to protect sensitive electronics from damage or latch-up due to ESD
- Designed to replace multilayer varistors (MLVs) in portable applications
- Features large cross-sectional area junctions for conducting high transient currents
- Offers superior electrical characteristics such as lower clamping voltage and no device degradation when compared to MLVs
- The combination of small size and high ESD surge capability makes them ideal for use in portable applications

### CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Good circuit board layout is critical for the suppression of ESD induced transients

- Place the ESD Protection Diode near the input terminals or connectors to restrict transient coupling
- Minimize the path length between the ESD Protection Diode and the protected line
- Minimize all conductive loops including power and ground loops
- The ESD transient return path to ground should be kept as short as possible
- Never run critical signals near board edges
- Use ground planes whenever possible

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