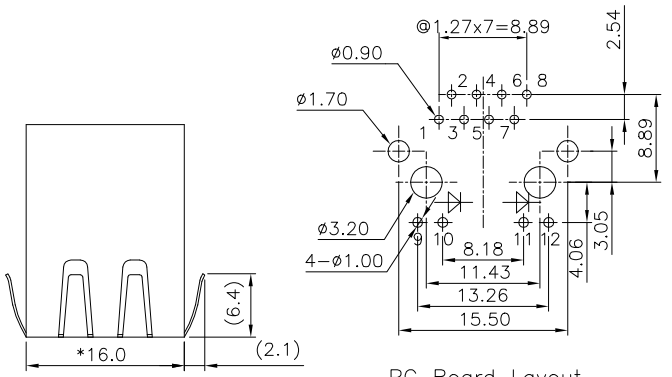
D1RFRD006

		REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	CHKD	
1		DRAWING MODIFICATION	ZJP 06/26/03		
2		ADD P/N	SHJ 09/04/04		
3		ADD P/N	SUNLL 01/04/05		
4		ADD P/N	SUNLL 02/25/05		



PC Board Layout
Component Side Shown

Characteristics Description:

1. RJ45 10/100 Base-Tx Transformer Jack With Transformer/ Impedance Resistor/High Voltage Capacitor.
2. Size Same As RJ-45 Modular Jack To Save PCB Board Space.
3. Reduce EMI Radiation, Improve EMI Performance.
4. Designed For Network Interface Card Application.
5. Designed To Meet IEEE 802.3u Requirement.
6. Designed For 100 Base Transmission over UTP-5 Cable.
7. Operation Temprature Range: 0°c To 70°c

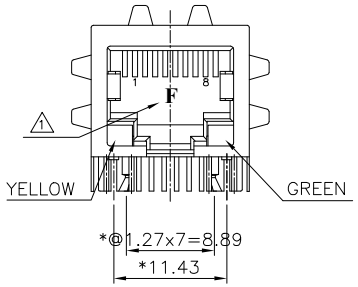
Mechanical:

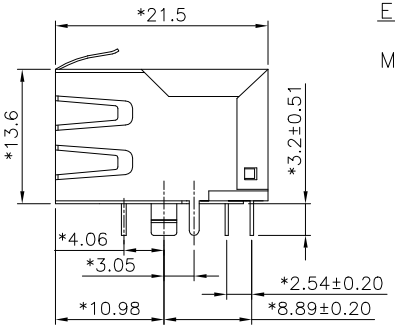
1. Housing Material : Glass Filled Polyester UL94V-0 OR FR52. 3
2. Contact Mateial : Phosphor Bronze t=0.35mm.
3. Plating : 1: Contact Area- Selectine Gold Plating.
   2: Tails-Tin-Lead Over Nickel OR Lead Free. 5
4. Operating Life : 750 Cycles Min.
5. Pcb Retention Pre-Solder : 1 Lb Min.
6. Pcb Retention Post-Solder : 10 Lbs Min.

Environmental:

1. Storage : -40°c To+85°c.

Mates With Modular Plug Conforming To Fcc Part 68, Subpart F.





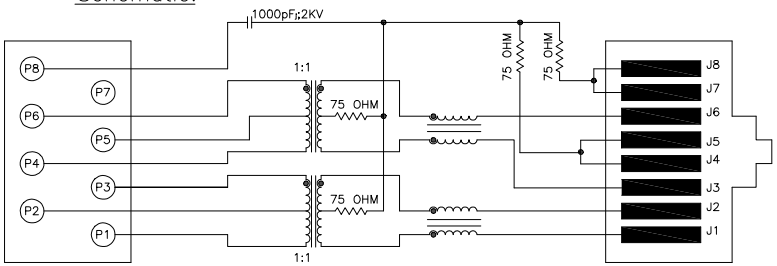
LED SPECIFICATIONS:

	YELLOW	GREEN
- COLOR:		
- FORWARD VOLTAGE(20mA)	2.5V(MAX)	2.5V(MAX)
- FORWARD VOLTAGE(20mA)	2.1V(TYP)	2.2V(TYP)
- POWER DISSIPATION:	105mW	105mW
- WAVE LENGTH:	590nm	565nm
- LUMINOUS INTENSITY(10mA):	2-8MCD	8-32MCD

(W/TIN)Part Number: E5TAB-XP079X
- 2 G-W/SIDE&TOP TABS
- 1-W/O TAB
- 1-3u" 2-6u" 3-15u" 4-30u" 5-50u"
- W/LED W/F 1

(LEAD FREE)Part Number: E5TAB-XXUD1X-L
- 4 G1-W/SIDE&TOP TABS
- 5 16-W/O TAB
- 1-3u" 2-6u" 3-15u" 4-30u" 5-50u"

Schematic:



(TYPICAL FOR EACH PORT)

DETACHED LISTS	MM (INCH)	DFTO xlf	DATE 07/07/01
	TOLERANCES EXCEPT AS NOTED	CHKD SHJ	DATE 2005/2/26
	MM .0 ±0.20 ± .00 ±0.15 ± .000 ±0.075 ±	MFO	DATE
		APPVLLUSHENG	DATE 2005/2/26
	ANGLES ±	MATERIAL :	
	THIRD ANGLE PROJECTION	QT'Y :	
		FINISH :	
		SCALE : 2:1	

FULL RISE ELECTRONIC CO., LTD

TITLE: Transformer LED JACK 1x1

DRAWING NO. GE5T3012 /PART NO. SEE NOTE | SIZE A3 | REV 4 02/25/05

DO NOT SCALE DRAWING | SHEET 1 OF 2

D1RFRD006

4		ADD P/N	SUNLL 02/25/05	

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	CHKD
1		DRAWING MODIFICATION	ZJP 06/26/03	
2		ADD P/N	SHJ 09/04/04	
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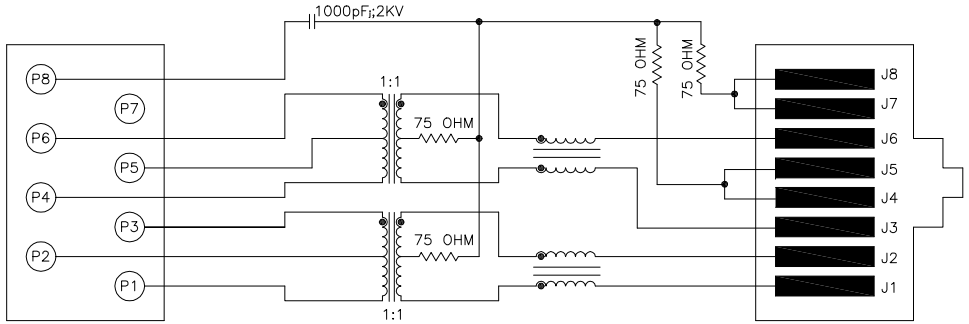

(TYPICAL FOR EACH PORT)

ELECTRICAL SPECIFICATIONS:

1.0 TURNS RATIO (P6–P5–P4):(J6–J3):1CT:1CT±3%
(P3–P2–P1):(J2–J1):1CT:1CT±3%
2.0 INDUCTANCE (P6–P4):350uH MIN @0.1V,100KHz,8mA DC Bias
(P3–P1):350uH MIN @0.1V,100KHz,8mA DC Bias
3.0 LEAKAGE INDUCTANCE P6–P4 (WITH J6 AND J3 SHORT):0.3uH MAX @1MHz
P3–P1 (WITH J2 AND J1 SHORT):0.3uH MAX @1MHz
4.0 INTERWINDING CAPACITANCE (P6,P5,P4) TO (J6,J3):30pf MAX @ 1MHz
(P3,P2,P1) TO (J2,J1) :30pf MAX @ 1MHz
5.0 DC RESISTANCE (J6–J3)=(J2–J1):1.2 ohms MAX
6.0 RETURN LOSS:(P6–P4)=100 OHMS AND (P1–P3)=100 OHM REF.
1MHz TO 30MHz:18dB MIN
60MHz TO 80MHz:12dB MIN
NOTE:100 OHMS CONNECTED TO (J2–J1)OR(J6–J3)
7.0 VOLTAGE WITHSTAND:
(J1,J2) TO (P1,P3):1500VAC
(J3,J6) TO (P4,P6):1500VAC
8.0 INSERTION LOSS:RS=RL=100 OHMS
100KHz TO 100MHz:1.1 dB TYP
9.0 RISE TIME:RS=100 OHMS AND RL=100 OHMS
OUTPUT VOLTAGE=1 V peak:3.0 ns MAX
10.0 CROSS TALK:1MHz TO 100MHz:40 dB TYP
11.0 COMMON TO COMMON MODE ATTENUATION:30MHz TO 100MHz:35 dB TYP
12.0 ISOLATION VOLTAGE @60HZ:1500Vrms(INPUT TO OUTPUT) 60SEC

NOTES:

1.0 PINS WITHOUT ELECTRICAL CONNECTION ARE OMITTED

MM (INCH)		DFTO xlf	DATE 07/07/01
TOLERANCES EXCEPT AS NOTED		CHKD SHJ	DATE 2005/2/26
MM		MFO	DATE
.0 ±0.20	±	APPVL LUSHENG	DATE 2005/2/26
.00 ±0.15	±		
.000 ±0.075	±	MATERIAL :	
ANGLES ±		QT'Y :	
THIRD ANGLE PROJECTION		FINISH :	
DETACHED LISTS		SCALE : 2:1	

FULL RISE ELECTRONIC CO., LTD

TITLE
Transformer LED JACK 1x1

DRAWING NO. GE5T3012
/PART NO. SEE NOTE
SIZE A3
REV 4 02/25/05
DO NOT SCALE DRAWING
SHEET 2 OF 2

8 7 6 5 4 3 2 1
H G F E D C B A