

# ACPL-K34T

## Automotive 2.5 A Peak High Output Current MOSFET Gate Drive Optocoupler with Rail-to-Rail Output Voltage in Stretched SO8



### Data Sheet



Lead (Pb) Free  
RoHS 6 fully compliant

RoHS 6 fully compliant options available;  
-xxxE denotes a lead-free product

#### Description

Avago's 2.5 Amp Automotive R<sup>2</sup>Coupler Gate Drive Optocoupler contains an AlGaAs LED, which is optically coupled to an integrated circuit with a power output stage. The ACPL-K34T features fast propagation delay and tight timing skew, is ideally designed for driving power MOSFETs used in AC-DC and DC-DC converters. The high operating voltage range of the output stage provides the drive voltages required by gate controlled devices. The voltage and high peak output current supplied by this optocoupler make it ideally suited for direct driving power MOSFETs at high frequency for high efficiency conversion.

Avago R<sup>2</sup>Coupler isolation products provide reinforced insulation and reliability that delivers safe signal isolation critical in automotive and high temperature industrial applications.

#### Functional Diagram

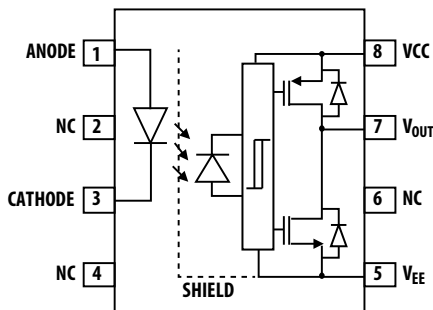


Figure 1. ACPL-K34T Functional Diagram

Note: Minimum 1  $\mu$ F bypass capacitor must be connected between pins V<sub>CC</sub> and V<sub>EE</sub>.

#### Truth Table

LED	V <sub>CC</sub> - V <sub>EE</sub>	V <sub>OUT</sub>
OFF	0 - 20V	LOW
ON	<V <sub>UVLO-</sub>	LOW
ON	>V <sub>UVLO+</sub>	HIGH

#### Features

- Qualified to AEC-Q100 Grade 1 Test Guidelines
- Automotive temperature range: -40 °C to 125 °C
- Peak output current: 2.0 A min.
- Rail-to-rail output voltage
- Propagation delay: 110 ns max.
- Dead time distortion: +50 ns/-40 ns
- LED current input drive with hysteresis
- Common Mode Rejection (CMR): 50 kV/ $\mu$ s min. at V<sub>CM</sub> = 1500 V
- Low supply current allow bootstrap half-bridge topology: I<sub>CC</sub> = 3.9 mA max.
- Under Voltage Lock-Out (UVLO) protection with hysteresis for power MOSFET
- Wide operating V<sub>CC</sub> range: 10 V to 20 V
- Safety Approvals:
  - UL Recognized 5000 V<sub>RMS</sub> for 1 min
  - CSA
  - IEC/EN/DIN EN 60747-5-5 V<sub>IORM</sub> = 1140 V<sub>peak</sub>

#### Applications

- Hybrid Power Train DC/DC Converter
- EV/PHEV Charger
- Automotive Isolated MOSFET Gate Drive
- AC and Brushless DC motor drives

**CAUTION:** It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

## Ordering Information

Part number	Option (RoHS Compliant)	Package	Surface Mount	Tape & Reel	UL 5000 V <sub>rms</sub> / 1 Minute rating	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-K34T	-000E	Stretched	X		X		80 per tube
	-060E	SO-8	X		X	X	80 per tube
	-500E		X	X	X		1000 per reel
	-560E		X	X	X	X	1000 per reel

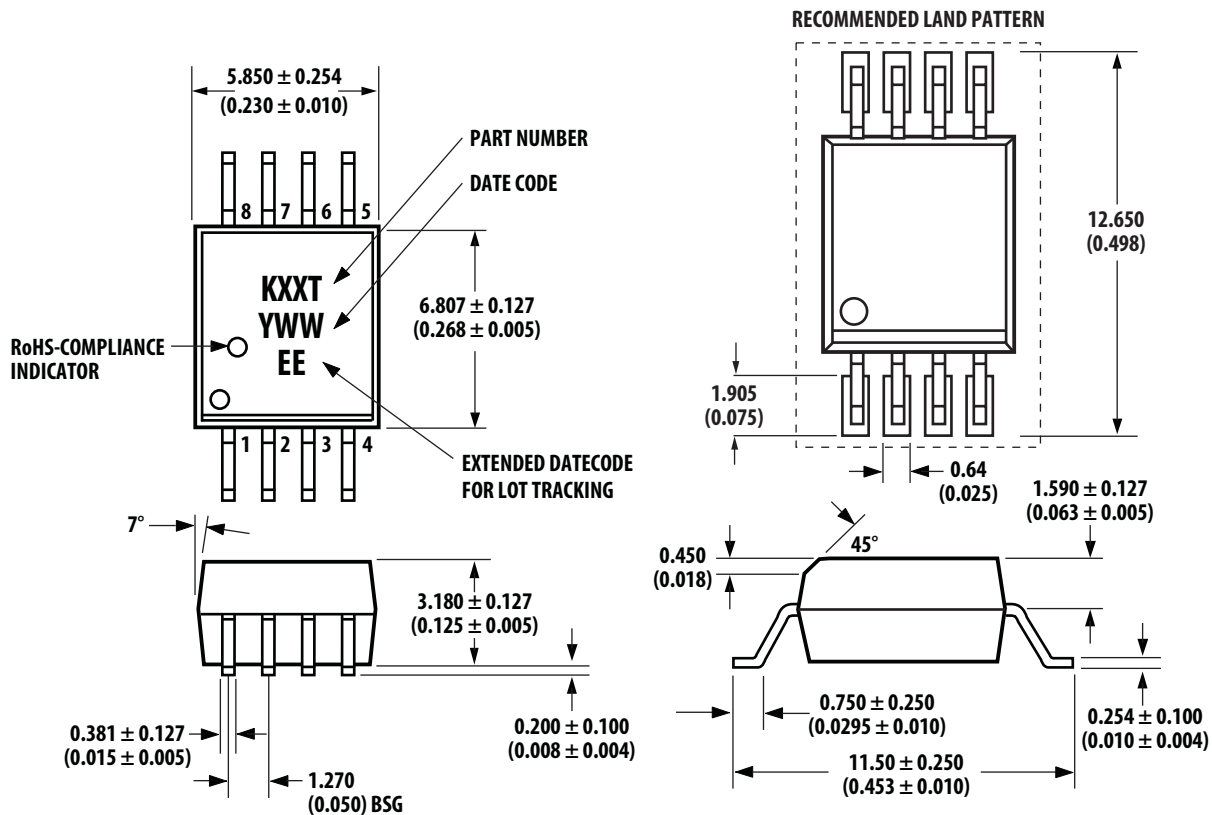
To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

ACPL-K34T-560E to order product of SSO-8 Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

## Package Outline Drawings (Stretched SO8)



## Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision).

Note: Non-halide flux should be used

## Regulatory Information

The ACPL-K34T is approved by the following organizations:

<b>UL</b>	UL 1577, component recognition program up to $V_{ISO} = 5 \text{ kV}_{RMS}$
<b>CSA</b>	CSA Component Acceptance Notice #5.
<b>IEC/EN/DIN EN 60747-5-5</b>	IEC 60747-5-5 EN 60747-5-5 DIN EN 60747-5-5

### IEC/EN/DIN EN 60747-5-5 Insulation Related Characteristic (Option 060 and 560 only)

Description	Symbol	Option 060 and 560	Units
Installation classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage < 600 $V_{rms}$ for rated mains voltage < 1000 $V_{rms}$		I – IV I – III	
Climatic Classification		40/125/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	$V_{IORM}$	1140	$V_{peak}$
Input to Output Test Voltage, Method b $V_{IORM} \times 1.875 = V_{PR}$ , 100% Production Test with $t_m = 1 \text{ sec}$ , Partial discharge < 5 pC	$V_{PR}$	2137	$V_{peak}$
Input to Output Test Voltage, Method a $V_{IORM} \times 1.6 = V_{PR}$ , Type and Sample Test with $t_m = 10 \text{ sec}$ , Partial discharge < 5 pC	$V_{PR}$	1824	$V_{peak}$
Highest Allowable Overvoltage (Transient Overvoltage $t_{ini} = 60 \text{ sec}$ )	$V_{IOTM}$	8000	$V_{peak}$
Safety-limiting values – maximum values allowed in the event of a failure, also see Figure 5.			
Case Temperature	$T_s$	175	$^{\circ}\text{C}$
Input Current	$I_{S, INPUT}$	230	mA
Output Power	$P_{S, OUTPUT}$	600	mW
Insulation Resistance at $T_s$ , $V_{IO} = 500 \text{ V}$	$R_s$	$> 10^9$	$\Omega$

### Insulation and Safety Related Specifications

Parameter	Symbol	ACPL-K34T	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	8	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	8	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group (DIN VDE0109)		IIIa		Material Group (DIN VDE 0109)

## Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	$T_S$	-55	150	°C	
Operating Temperature	$T_A$	-40	125	°C	
IC Junction Temperature	$T_J$		150	°C	3
Average Input Current	$I_{F(AVG)}$		20	mA	
Peak Input Current (50% duty cycle, < 1 ms pulse width)	$I_{F(PEAK)}$		40	mA	
Peak Transient Input Current (<1 $\mu$ s pulse width, 300 pps)	$I_{F(TRAN)}$		1	A	
Reverse Input Voltage	$V_R$		6	V	
“High” Peak Output Current	$I_{OH(PEAK)}$		2.5	A	1
“Low” Peak Output Current	$I_{OL(PEAK)}$		2.5	A	1
Total Output Supply Voltage	$(V_{CC} - V_{EE})$	0	25	V	
Output Voltage	$V_{O(PEAK)}$	-0.5	$V_{CC}$	V	
Output IC Power Dissipation	$P_O$		500	mW	2
Total Power Dissipation	$P_T$		550	mW	3

## Recommended Operating Conditions

Parameter	Symbol	Min	Max.	Units	Note
Operating Temperature	$T_A$	-40	125	°C	
Output Supply Voltage	$(V_{CC} - V_{EE})$	10	20	V	
Input Current (ON)	$I_{F(ON)}$	7	13	mA	
Input Voltage (OFF)	$V_{F(OFF)}$	-5.5	0.8	V	

## Electrical Specifications (DC)

Unless otherwise noted, all Minimum/Maximum specifications are at Recommended Operating Conditions. All typical values are at  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{CC} - V_{EE} = 10\text{ V}$ ,  $V_{EE} = \text{Ground}$ .

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
High Level Peak Output Current	$I_{OH}$		-3.5	-2.0	A	$V_{CC} - V_O = 10\text{ V}$	3	
Low Level Peak Output Current	$I_{OL}$	2.0	4.4		A	$V_O - V_{EE} = 10\text{ V}$	4	
High Output Transistor RDS(ON)	$R_{DS,OH}$		2.2	4.0	$\Omega$	$I_{OH} = -2.0\text{ A}$		4
Low Output Transistor RDS(ON)	$R_{DS,OL}$		1.0	2.0	$\Omega$	$I_{OL} = 2.0\text{ A}$		4
High Level Output Voltage	$V_{OH}$	$V_{CC} - 0.4$	$V_{CC} - 0.2$		V	$I_F = 10\text{ mA}$ , $I_O = -100\text{ mA}$		5, 6
Low Level Output Voltage	$V_{OL}$		0.1	0.25	V	$I_O = 100\text{ mA}$		
High Level Supply Current	$I_{CCH}$		2.5	3.9	mA	$I_F = 10\text{ mA}$		5
Low Level Supply Current	$I_{CCL}$		2.5	3.9	mA	$V_F = 0\text{ V}$		6
Threshold Input Current Low to High	$I_{FLH}$		1.5	4.9	mA	$V_O > 5\text{ V}$		7
Threshold Input Voltage High to Low	$V_{FHL}$	0.8			V			
Input Forward Voltage	$V_F$	1.25	1.5	1.85	V	$I_F = 10\text{ mA}$		7
Temperature Coefficient of Input Forward Voltage	$\Delta V_F / \Delta T_A$		-1.5		mV/°C			
Input Reverse Breakdown Voltage	$BV_R$	6			V	$I_R = 100\text{ }\mu\text{A}$		
Input Capacitance	$C_{IN}$		90		pF	$f = 1\text{ MHz}$ , $V_F = 0\text{ V}$		
UVLO Threshold	$V_{UVLO+}$	8.1	8.6	9.1	V	$V_O > 5\text{ V}$ , $I_F = 10\text{ mA}$		8
	$V_{UVLO-}$	7.1	7.6	8.1				8
UVLO Hysteresis	$UVLO_{HYS}$	0.5	1.0		V			

## Switching Specifications (AC)

Unless otherwise noted, all Minimum/Maximum specifications are at Recommended Operating Conditions. All typical values are at  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{CC} - V_{EE} = 10\text{ V}$ ,  $V_{EE} = \text{Ground}$ .

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to High Output Level	$t_{PLH}$	30	60	110	ns	$V_{CC} = 10\text{ V}$ $R_G = 4.7\Omega$ , $C_L = 10\text{ nF}$	9,12,14	7
Propagation Delay Time to Low Output Level	$t_{PHL}$	30	60	110	ns	$f = 200\text{ kHz}$ , Duty Cycle = 50%	10,12,14	
Pulse Width Distortion ( $t_{PHL} - t_{PLH}$ )	PWD	-40	0	40	ns	$V_{in} = 4.5\text{ V} - 5.5\text{ V}$ , $R_{in} = 350\Omega$	11	8
Dead Time Distortion Caused by Any Two Parts ( $t_{PLH} - t_{PHL}$ )	DTD	-40		50	ns			9
Rise Time	$t_R$		10	30	ns	$V_{CC} = 10\text{ V}$ , $C_L = 1\text{ nF}$ , $f = 200\text{ kHz}$ , Duty Cycle = 50%	13, 14	
Fall Time	$t_F$		10	30	ns	$V_{in} = 4.5\text{ V} - 5.5\text{ V}$ , $R_{in} = 350\Omega$		
Output High Level Common Mode Transient Immunity	$ CM_H $	50	>75		kV/ $\mu\text{s}$	$T_A = 25\text{ }^\circ\text{C}$ , $V_{CC} = 20\text{ V}$ , $V_{CM} = 1500\text{ V}$ , with split resistors	15	10, 11
Output Low Level Common Mode Transient Immunity	$ CM_L $	50	>75		kV/ $\mu\text{s}$			10, 12

## Package Characteristics

Unless otherwise noted, all Minimum/Maximum specifications are at Recommended Operating Conditions. All typical values are at  $T_A = 25\text{ }^\circ\text{C}$ .

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage*	$V_{ISO}$	5000			$V_{RMS}$	$RH < 50\%$ , $t = 1\text{ min}$ , $T_A = 25\text{ }^\circ\text{C}$		13, 14
Input-Output Resistance	$R_{I-O}$		$10^{14}$		$\Omega$	$V_{I-O} = 500\text{ V}_{DC}$		14
Input-Output Capacitance	$C_{I-O}$		0.6		pF	$f = 1\text{ MHz}$		

\* The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to your equipment level safety specification or Avago Technologies Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."

Notes:

1. Maximum pulse width = 100 ns, Duty cycle = 2%.
2. Derate linearly above 110 °C free-air temperature at a rate of 13 mW/°C. Refer to Figure 2 from Output IC Power Dissipation Derating Chart.
3. Total power dissipation is derated linearly above 110 °C free-air temperature at a rate of 13 mW/°C. The maximum LED and IC junction temperature should not exceed 150 °C.
4. Output is source at -2.0 A or 2.0 A with a maximum pulse width of 10  $\mu$ s.
5. In this test  $V_{OH}$  is measured with a DC load current. When driving capacitive loads  $V_{OH}$  will approach  $V_{CC}$  as  $I_{OH}$  approaches zero amps.
6. Maximum pulse width = 1 ms.
7. This load condition approximates the gate load of a 600 V/50 A power MOSFET.
8. Pulse Width Distortion (PWD) is defined as  $t_{PHL} - t_{PLH}$  for any given device.
9. Dead Time Distortion (DTD) is defined as  $t_{PLH} - t_{PHL}$  between any two parts under the same test condition. A negative DTD reduces original system dead time; while a positive DTD increases original system dead time.
10. Pin 2 and Pin 4 must be connected to LED common.
11. Common mode transient immunity in the high state is the maximum tolerable  $dV_{CM}/dt$  of the common mode pulse,  $V_{CM}$ , to assure that the output will remain in the high state, (i.e.,  $V_O > 10$  V).
12. Common mode transient immunity in a low state is the maximum tolerable  $dV_{CM}/dt$  of the common mode pulse,  $V_{CM}$ , to assure that the output will remain in a low state (i.e.,  $V_O < 1.0$  V).
13. In accordance with UL1577, each optocoupler is proof-tested by applying an insulation test voltage  $\geq 6000$   $V_{RMS}$  for 1 second.
14. Device considered a two-terminal device: pins 1, 2, 3 and 4 shorted together and pins 5, 6, 7 and 8 shorted together.

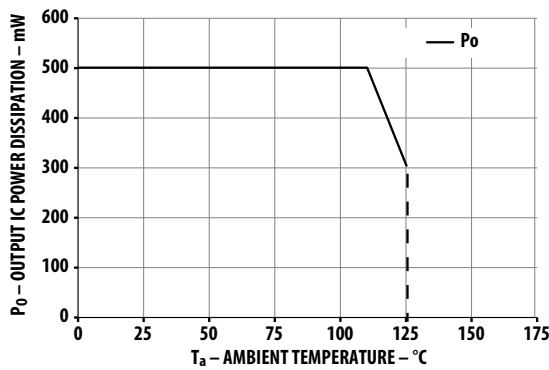


Figure 2. Output IC Power Dissipation Derating Chart

## Typical Performance Plots

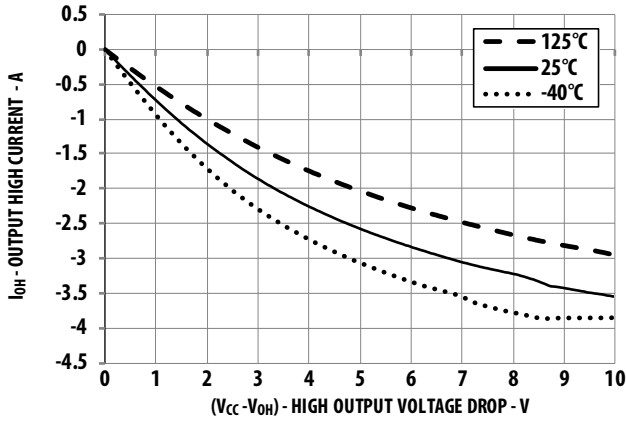


Figure 3.  $I_{OH}$  vs.  $(V_{CC} - V_{OH})$

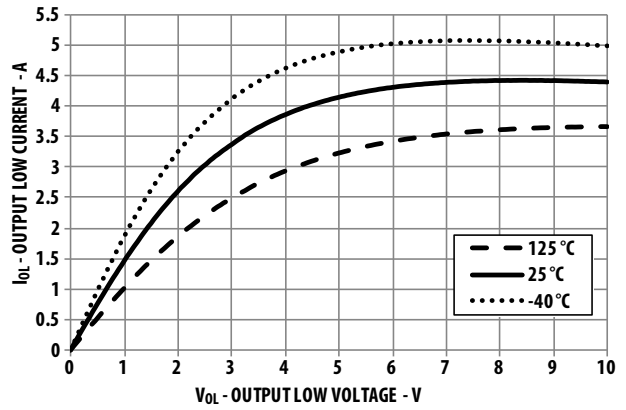


Figure 4.  $I_{OL}$  vs.  $V_{OL}$

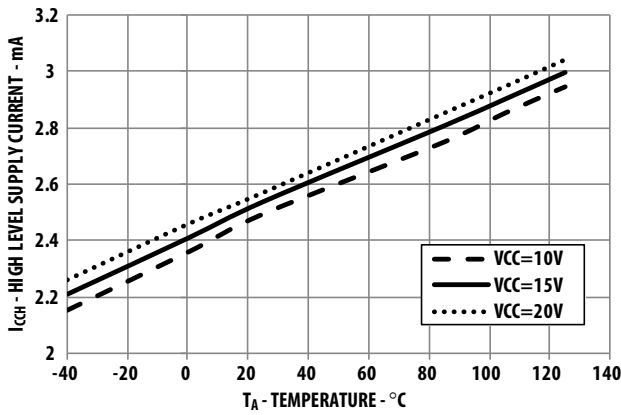


Figure 5.  $I_{CCH}$  vs. Temperature

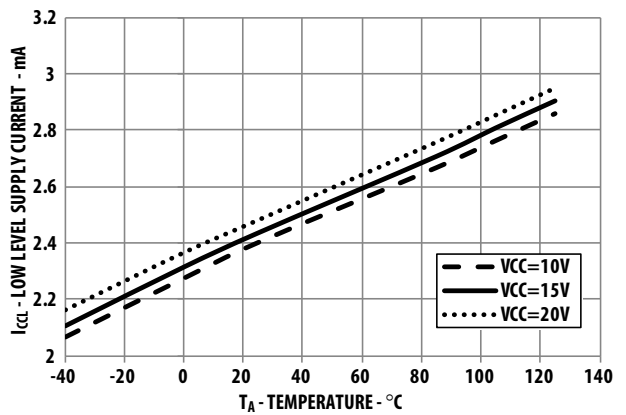


Figure 6.  $I_{CCL}$  vs. Temperature

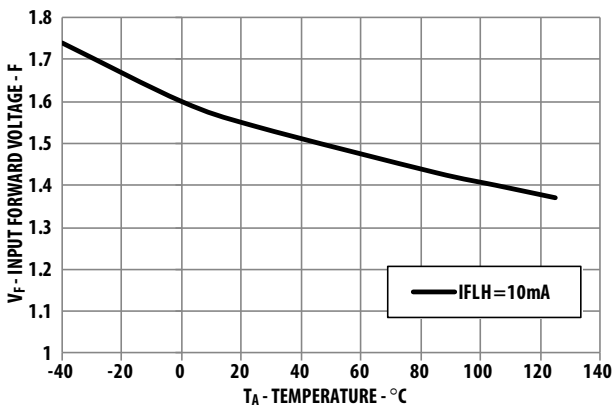


Figure 7.  $V_F$  vs. Temperature

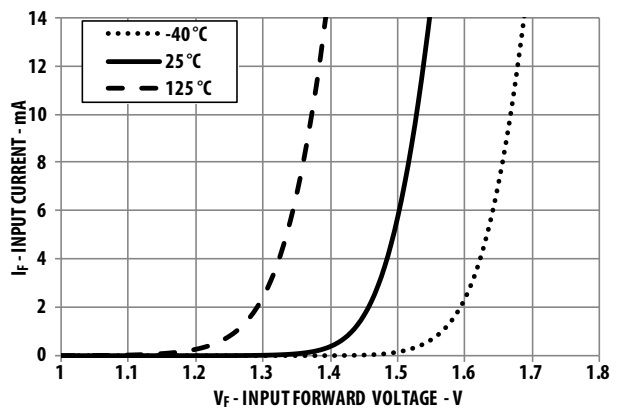


Figure 8.  $I_F$  vs.  $V_F$

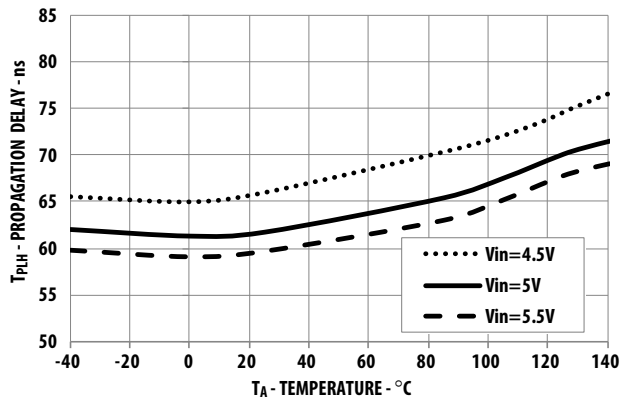


Figure 9.  $t_{pLH}$  vs. Temperature

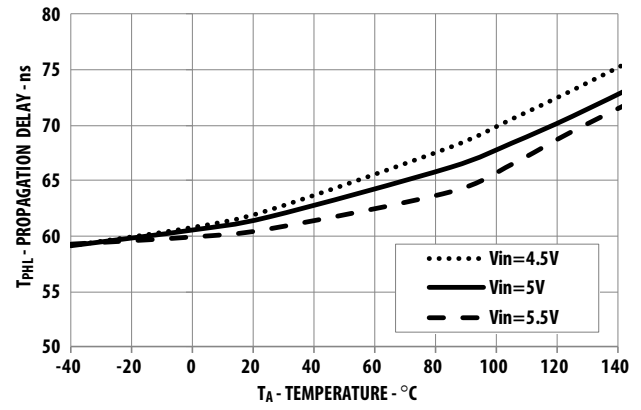


Figure 10.  $t_{pHL}$  vs. Temperature

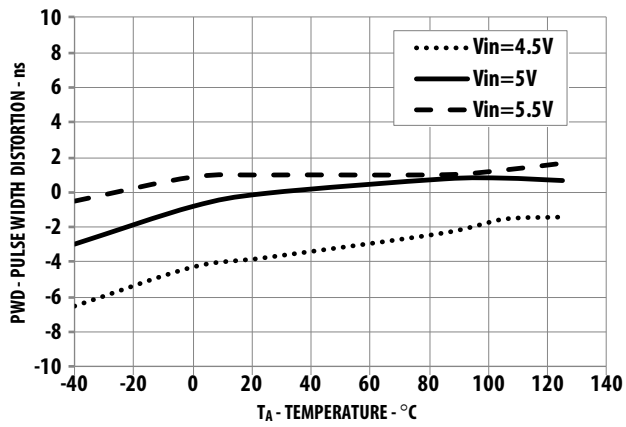


Figure 11. PWD vs. Temperature



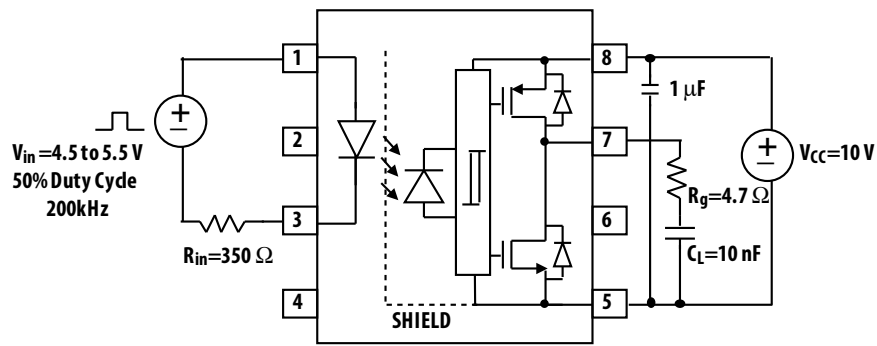


Figure 12.  $t_{PLH}$  and  $t_{PHL}$  test circuit

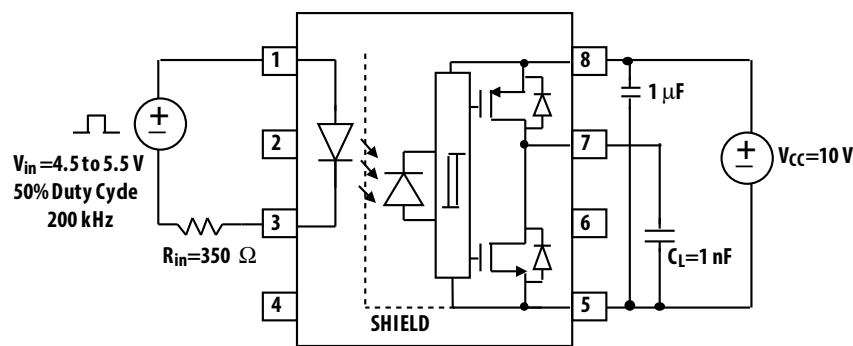


Figure 13.  $t_r$  and  $t_f$  test circuit

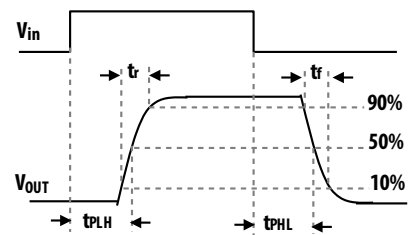


Figure 14.  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_r$  and  $t_f$  reference waveforms

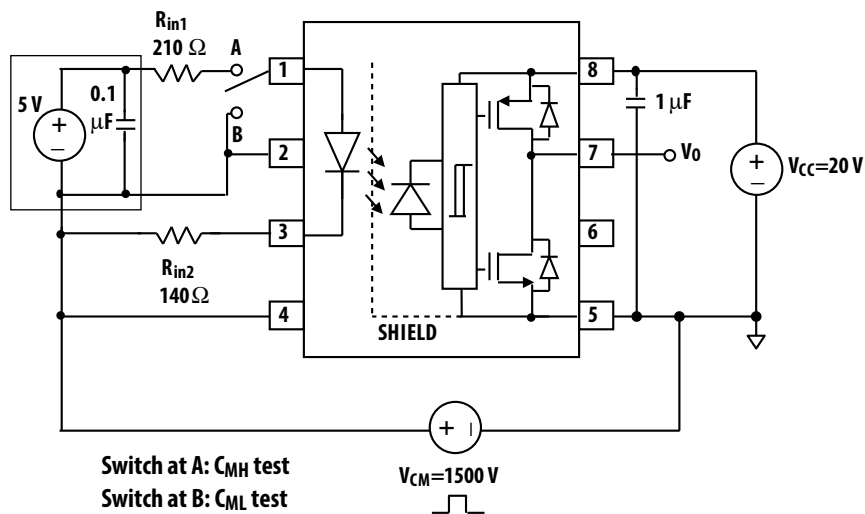


Figure 15. CMR test circuit

## Application Information

### Typical High Speed MOSFET Gate Drive Circuit

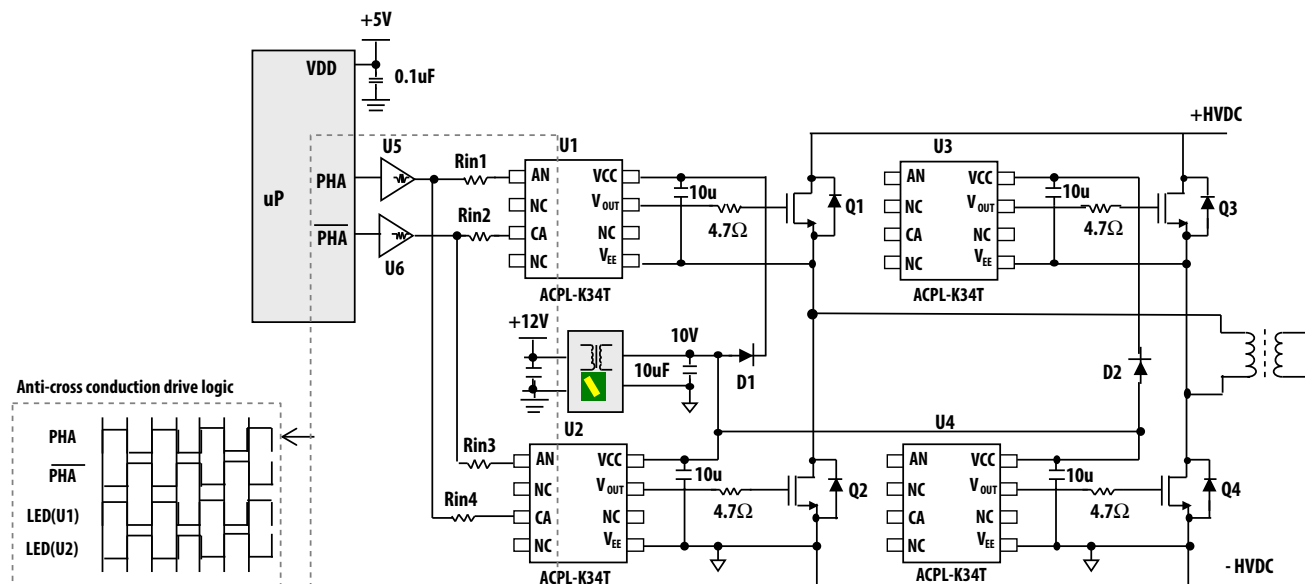


Figure 16. Typical high-speed MOSFET gate drive circuit

### Anti-Cross Conduction Drive

One of the many benefits of using ACPL-K34T is the ease to implement anti-cross conduction drive between the high side and low side gate drivers to prevent shoot through event. This safety interlock drive can be realized by interlocking the output of buffer U5 and U6 to both high and low side gate drivers, as shown in Figure 16. However, due to the propagation delay difference between optocouplers, certain amount of dead time has to be added to ensure sufficient dead time at MOSFET gate. Refer to Dead Time and Propagation Delay section for more details.

### Recommended LED Drive Circuits

Common mode noise exists whenever there is a difference in the ground level of the optocoupler's input control circuitry and output control circuitry. Figure 17 and 18 show recommended LED drive circuits for high common mode rejection (CMR) performance of the optocoupler gate driver. Split limiting resistors are used to balance the impedance at both anode and cathode of the input LED for high common mode noise rejection (see Figure 15).

Open drain and open collector drive circuits showed in Figure 19 are not recommended. During the off state of the MOSFET/transistor, cathode of the input LED sees high impedance and becomes sensitive to noise. In any cases, if designer still prefers to use single MOSFET/transistor drive over the recommended CMOS buffer drive showed in Figure 17 and 18, designer can choose alternative circuits showed in Figure 20; however M1/Q1 in Figure 20 drive circuits will shunt current during LED off state, which result in more power consumption.

### Drive Power

If CMOS buffer is used to drive LED, it is recommended to connect the CMOS buffer at the LED cathode. This is because the sinking capability of the NMOS is usually more than the driving capability of the PMOS in a CMOS buffer.

### Drive Logic

Designer can configure LED drive circuits for non-inverting and inverting logic as recommended in Figure 17 and 18. External power supply,  $V_{DD1}$  has to be connected to the CMOS buffer for the inverting and non-inverting logic to work. If  $V_{DD1}$  supply is lost, LED will be permanently off and output will be at low.

## Bypass and Reservoir Capacitors

Supply bypass capacitors are necessary at the input buffer and ACPL-K34T output supply pin. A ceramic capacitor with the value of 0.1  $\mu\text{F}$  is recommended at the input buffer, which also helps to improve CMR performance. At the output supply pin ( $V_{CC} - V_{EE}$ ), it is recommended to use a 10  $\mu\text{F}$ , low ESR and low ESL capacitor as a charge reservoir to supply instant driving current to MOSFET at  $V_{OUT}$  during switching.

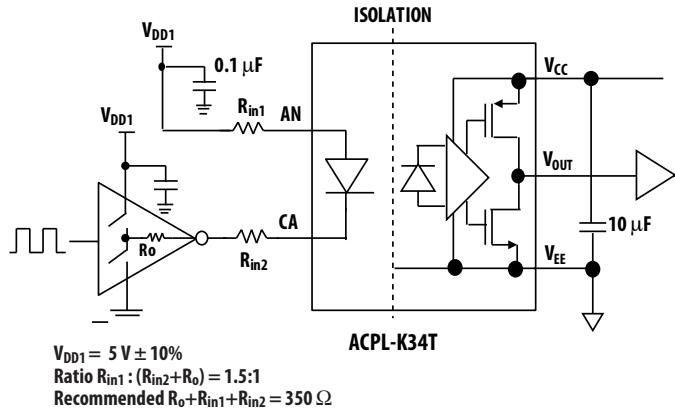


Figure 17. Recommended non-inverting drive circuit

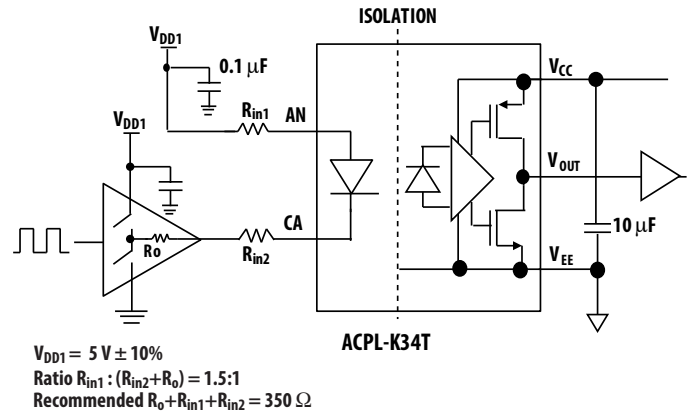


Figure 18. Recommended inverting drive circuit

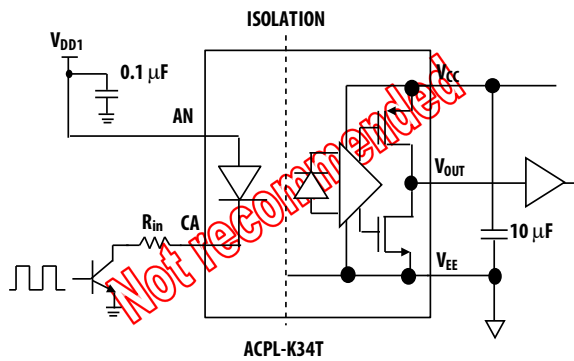


Figure 19(a)

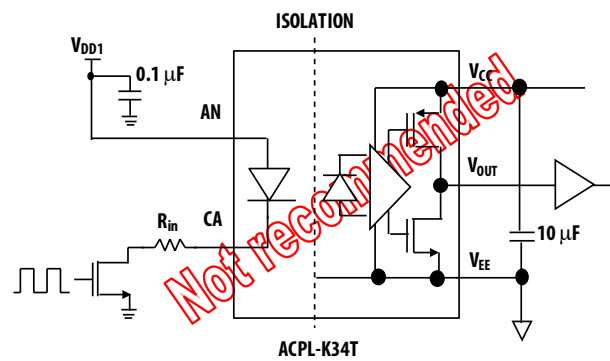


Figure 19(b)

Figure 19(a) and Figure 19(b). Not recommended – Open drain/open collector drive circuit

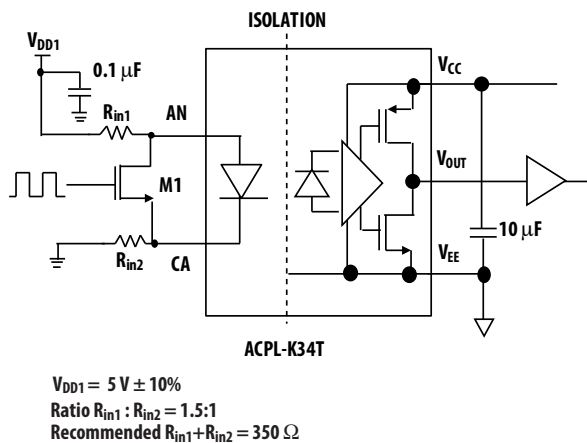


Figure 20(a)

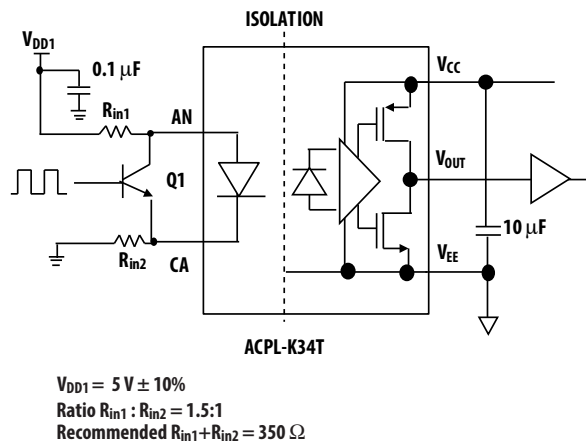


Figure 20(b)

Figure 20(a) and Figure 20(b). Alternative LED drive circuits to replace Figure 19(a) and 19(b)

## Initial Power Up and UVLO Operation

Insufficient gate voltage to MOSFET can increase turn on resistance of MOSFET, resulting in large power loss and MOSFET damage due to high heat dissipation. ACPL-K34T monitors the output power supply constantly. During initial power up, the ACPL-K34T requires maximum 50  $\mu$ s of initial startup time for the internal bias and circuitry to get ready. The gate driver output ( $V_{OUT}$ ) is hold at off state during initial startup time. Thereafter, when the output power supply is lower than under voltage lockout ( $V_{UVLO-}$ ) threshold, gate driver output will shut off to protect MOSFET from low voltage bias. When the output power supply is more than the  $V_{UVLO+}$  threshold,  $V_{OUT}$  is released from low state and it follows the input LED drive signal, as shown in Figure 21.

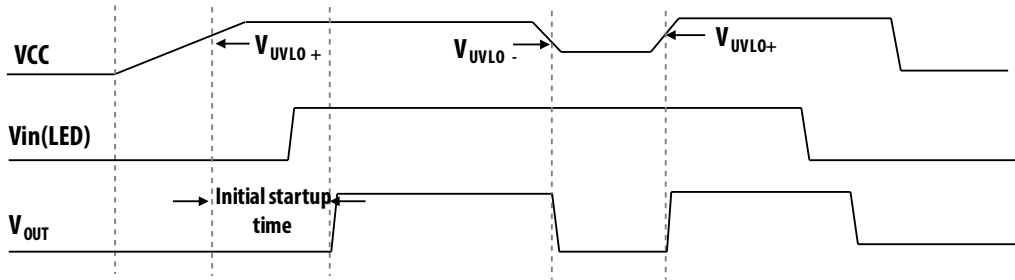


Figure 21. ACPL-K34T initial power-up and UVLO operation

## Dead Time Distortion and Propagation Delay

Dead time is the period of time during which both high side and low side power transistors (shown as Q1 and Q2 in Figure 16) are off. Any overlap in Q1 and Q2 conduction will result in a shoot-through event and large short circuit current will flow through the power devices between the high side and low side power rail.

ACPL-K34T includes a Dead Time Distortion (DTD) specification intended to help designers optimize dead time in a power inverter design. A negative DTD value will decrease the system dead time, and so a negative DTD must be compensated by adding extra dead time to the design. Figure 22a shows that dead time after optocoupler is reduced by negative DTD. On the other hand, a positive DTD will add to the system original dead time, and so a positive DTD will cause dead time redundancy to the system. Figure 22b shows that dead time after optocoupler is increased by positive DTD.

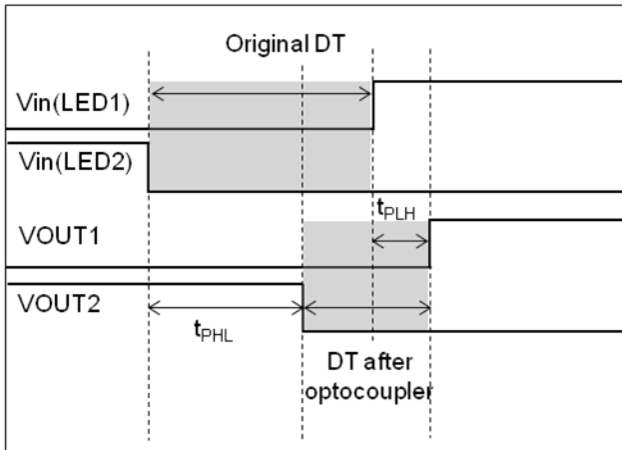


Figure 22a. Negative DTD reduces original DT

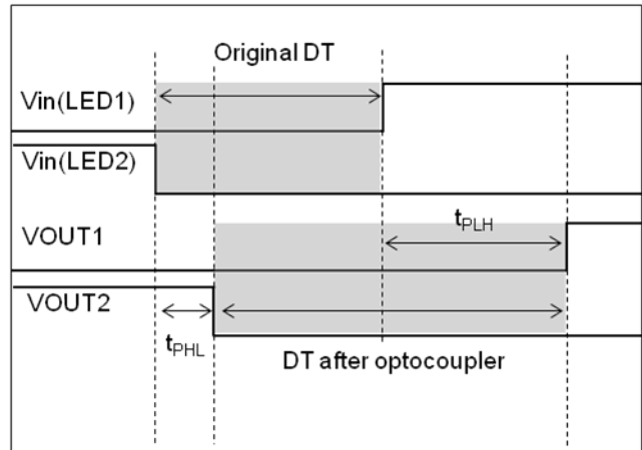


Figure 22b. Positive DTD increased original DT

Figure 22. Dead Time and Propagation Delay Waveforms

To prevent cross-conduction between high side and low side power transistors, minimum dead time (DT MIN) must be introduced to the system. For example, given DTD MIN = -40 ns and DTD MAX = 50 ns, if designers target to have minimum dead time (DT MIN) of 20 ns after the optocoupler, then initial dead time (DT) needed for the system can be calculated as:

$$\begin{aligned}DT &= DT \text{ MIN} - DTD \text{ MIN} \\ &= 20\text{ns} - (-40\text{ns}) \\ &= 60\text{ns}\end{aligned}$$

Maximum dead time (DT MAX) after the optocoupler can be calculated as:

$$\begin{aligned}DT \text{ MAX} &= DT + DTD \text{ MAX} \\ &= 60 \text{ ns} + 50 \text{ ns} \\ &= 110 \text{ ns}\end{aligned}$$

By introducing DT = 60 ns, the overall system dead time can vary from 20 ns to 110 ns due to the optocoupler's DTD.

Note: The propagation delays used to calculate dead time distortion (DTD) are taken at equal temperatures and test conditions since the optocouplers used are typically mounted close to each other and are switching the same type of MOSFETs.

### Thermal Resistance Model for ACPL-K34T

The diagram for measurement is shown in Figure 23. Here, one die is heated first and the temperatures of all the dice are recorded after thermal equilibrium is reached. Then, the second die is heated and all the dice temperatures are recorded. With the known ambient temperature, the die junction temperature and power dissipation, the thermal resistance can be calculated. The thermal resistance calculation can be cast in matrix form. This yields a 2 by 2 matrix for our case of two heat sources.

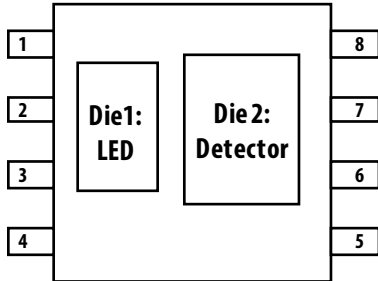


Figure 23. Diagram of ACPL-K34T for measurement

$$\begin{bmatrix} R11 & R12 \\ R21 & R22 \end{bmatrix} \cdot \begin{bmatrix} P1 \\ P2 \end{bmatrix} = \begin{bmatrix} \Delta T1 \\ \Delta T2 \end{bmatrix}$$

R11: Thermal Resistance of Die1 due to heating of Die1 (°C/W)

R12: Thermal Resistance of Die1 due to heating of Die2 (°C/W)

R21: Thermal Resistance of Die2 due to heating of Die1 (°C/W)

R22: Thermal Resistance of Die2 due to heating of Die2 (°C/W)

P1: Power dissipation of Die1 (W)

P2: Power dissipation of Die2 (W)

T1: Junction temperature of Die1 due to heat from all dice (°C)

T2: Junction temperature of Die2 due to heat from all dice (°C)

T<sub>A</sub>: Ambient temperature (°C)

ΔT1: Temperature difference between Die 1 junction and ambient (°C)

ΔT2: Temperature difference between Die2 junction and ambient (°C)

$$T1 = (R11 \times P1 + R12 \times P2) + T_A \text{ -----(1)}$$

$$T2 = (R21 \times P1 + R22 \times P2) + T_A \text{ -----(2)}$$

Measurement is done on both low and high conductivity boards as shown below:

Layout	Measurement data	
	Low conductivity board:	High conductivity board:
	R11=191 °C/W R12=R21= 68.5°C/W R22=77°C/W	R11=155 °C/W R12=R21= 64°C/W R22=41°C/W

Note that the above thermal resistance R11, R12, R21 and R22 can be improved by increasing the ground plane/copper area.

Application and environment design for ACPL-K34T needs to ensure that the junction temperature of the internal IC and LED within the gate drive optocoupler do not exceed 150 °C. The equation (1) and (2) provided above are for the purposes of estimating the junction temperatures. For example:

#### Calculation of LED and output IC power dissipation

$$\begin{aligned} \text{LED power dissipation, } P_E &= I_{F(\text{LED})} (\text{Recommended Max}) * V_{F(\text{LED})} (\text{at } 125 \text{ }^\circ\text{C}) * \text{Duty Cycle} \\ &= 13 \text{ mA} * 1.25 \text{ V} * 50\% \\ &= 8.125 \text{ mW} \end{aligned}$$

$$\begin{aligned} \text{Output IC power dissipation, } P_O &= V_{CC} (\text{Recommended Max}) * I_{CC}(\text{Max}) + P_{HS} + P_{LS} \\ &= 20 \text{ V} * 4 \text{ mA} + 53.3 \text{ mW} + 32 \text{ mW} \\ &= 165.3 \text{ mW} \end{aligned}$$

where PHS = High side switching power dissipation

$$\begin{aligned} &= (V_{CC} * Q_G * f_{PWM}) * R_{DS,OH(\text{MAX})} / (R_{DS,OH(\text{MAX})} + R_{GH}) / 2 \\ &= (20 \text{ V} * 80\text{nC} * 200 \text{ kHz}) * 4\Omega / (4\Omega + 8\Omega) / 2 \\ &= 53.3\text{mW} \end{aligned}$$

PLS = Low side switching power dissipation

$$\begin{aligned} &= (V_{CC} * Q_G * f_{PWM}) * R_{DS,OL(\text{MAX})} / (R_{DS,OL(\text{MAX})} + R_{GL}) / 2 \\ &= (20 \text{ V} * 80 \text{ nC} * 200 \text{ kHz}) * 2\Omega / (2\Omega + 8\Omega) / 2 \\ &= 32 \text{ mW} \end{aligned}$$

$Q_G$  = Gate charge at supply voltage

$f_{PWM}$  = LED switching frequency

$R_{GH}$  = Gate charging resistance

$R_{GL}$  = Gate discharging resistance

Calculation of LED junction temperature and output IC junction temperature at  $T_a=125 \text{ }^\circ\text{C}$ :

LED junction temperature,

$$\begin{aligned} T_1 &= (R_{11} * P_E + R_{12} * P_O) + T_A \\ &= (191^\circ\text{C/W} * 8.125 \text{ mW} + 68.5 \text{ }^\circ\text{C/W} * 165.3 \text{ mW}) + 125 \text{ }^\circ\text{C} \\ &= 138 \text{ }^\circ\text{C} < T_{J(\text{absolute max})} \text{ of } 150 \text{ }^\circ\text{C} \end{aligned}$$

Output IC junction temperature,

$$\begin{aligned} T_2 &= (R_{21} * P_E + R_{22} * P_O) + T_A \\ &= (68.5 \text{ }^\circ\text{C/W} * 8.125 \text{ mW} + 77 \text{ }^\circ\text{C/W} * 165.3 \text{ mW}) + 125 \text{ }^\circ\text{C} \\ &= 138 \text{ }^\circ\text{C} < T_{J(\text{absolute max})} \text{ of } 150 \text{ }^\circ\text{C} \end{aligned}$$

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