



STB24NM60N

N-channel 600 V, 0.168 Ω , 17 A MDmesh™ II Power MOSFET
D²PAK

Features

Order codes	V _{DSS} (@T _{jmax})	R _{DS(on)} max.	I _D
STB24NM60N	650 V	< 0.19 Ω	17 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Application

Switching applications

Description

These N-channel 600 V Power MOSFET devices are made using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a new vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converter.

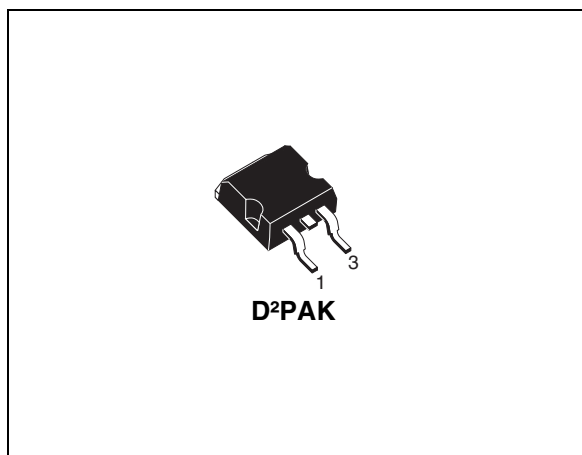


Figure 1. Internal schematic diagram

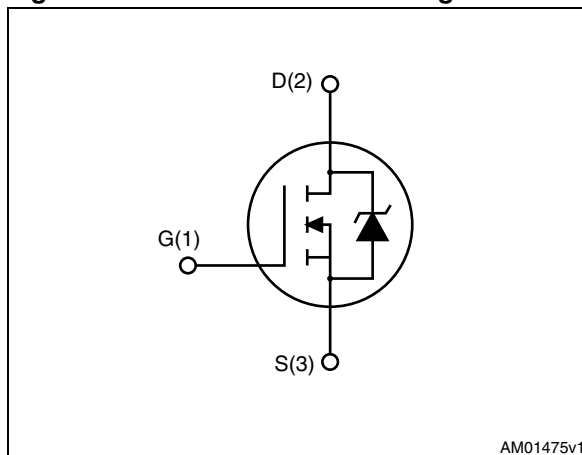


Table 1. Device summary

Order codes	Marking	Package	Packaging
STB24NM60N	24NM60N	D ² PAK	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate- source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	17	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	11	A
$I_{DM}^{(1)}$	Drain current (pulsed)	68	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	125	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. Pulse width limited by safe operating area.

2. $I_{SD} \leq 17\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, peak $V_{DS} \leq V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max.	1	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max.	30	$^\circ\text{C}/\text{W}$

1. When mounted on 1inch² FR-4 board, 2 oz Cu

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max)	6	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AS}$, $V_{DD} = 50\text{ V}$)	300	mJ

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0	600			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = Max rating V _{DS} = Max rating, T _C =125 °C			1 100	μA μA
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	V _{GS} = ± 25 V			100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2	3	4	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10 V, I _D = 8 A		0.168	0.19	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 50 V, f = 1 MHz, V _{GS} = 0	-	1400	-	pF
C _{oss}	Output capacitance			44		pF
C _{rss}	Reverse transfer capacitance			7.4		pF
C _{oss eq.} ⁽¹⁾	Equivalent output capacitance	V _{DS} = 0 to 480 V, V _{GS} = 0	-	190	-	pF
R _g	Gate input resistance	f=1 MHz open drain	-	5	-	Ω
Q _g	Total gate charge	V _{DD} = 480 V, I _D = 17 A, V _{GS} = 10 V <i>(see Figure 15)</i>	-	46	-	nC
Q _{gs}	Gate-source charge			7		nC
Q _{gd}	Gate-drain charge			23		nC

1. C_{o(eff)} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS}.

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 8.5\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 14)	-	11.5	-	ns
$t_{r(v)}$	Voltage rise time			16.5		ns
$t_{d(off)}$	Turn-off-delay time			73		ns
$t_{f(i)}$	Fall time			37		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		-		17	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				68	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 17\text{ A}$, $V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 17\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see Figure 16)	-	340		ns
Q_{rr}	Reverse recovery charge			4.6		μC
I_{RRM}	Reverse recovery current			27		A
t_{rr}	Reverse recovery time	$I_{SD} = 17\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ $T_J = 150\text{ }^\circ\text{C}$ (see Figure 16)	-	404		ns
Q_{rr}	Reverse recovery charge			5.7		μC
I_{RRM}	Reverse recovery current			28		A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

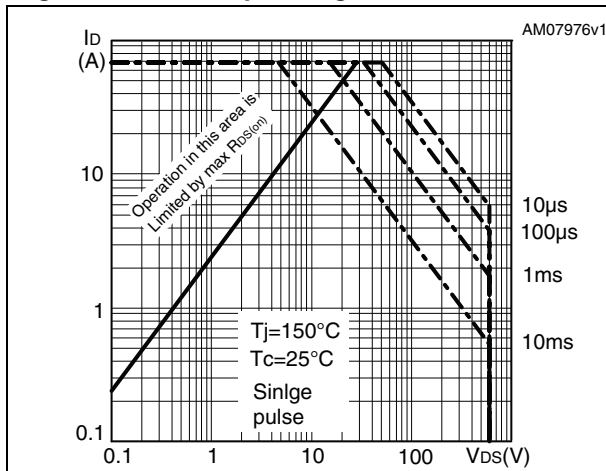


Figure 3. Thermal impedance

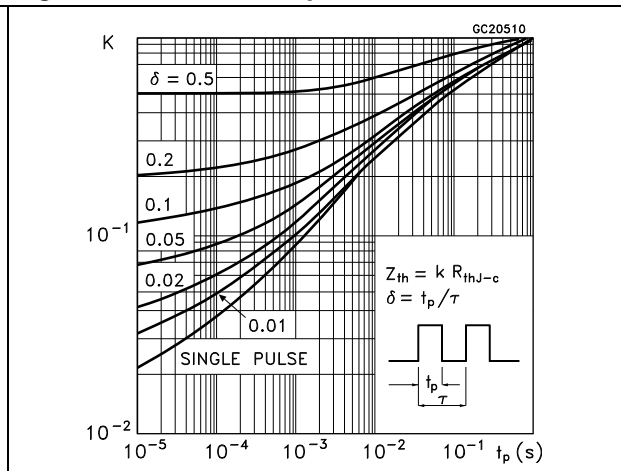


Figure 4. Output characteristics

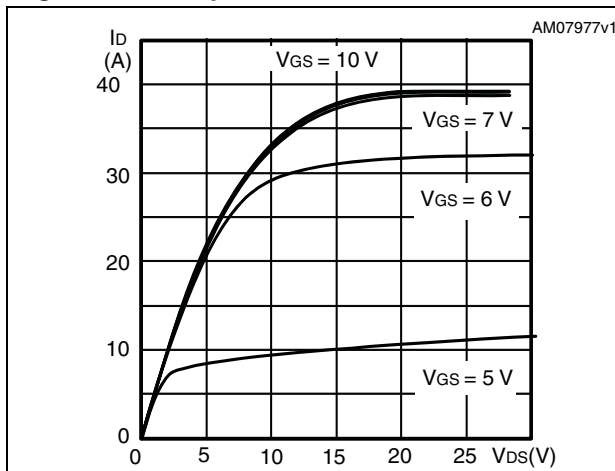


Figure 5. Transfer characteristics

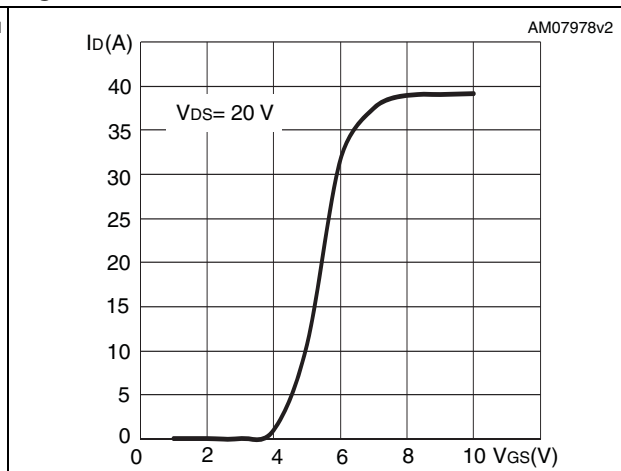


Figure 6. Gate charge vs gate-source voltage

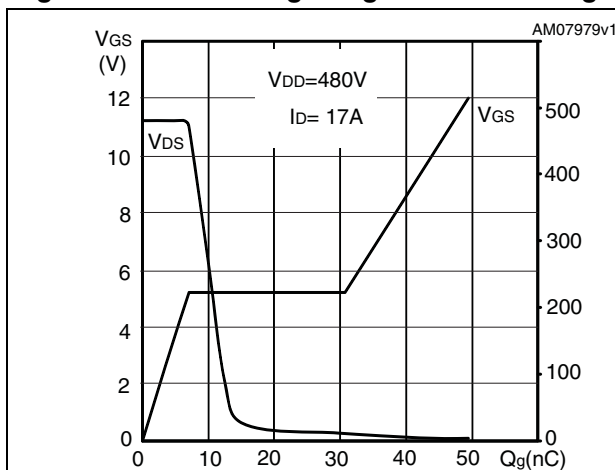


Figure 7. Static drain-source on resistance

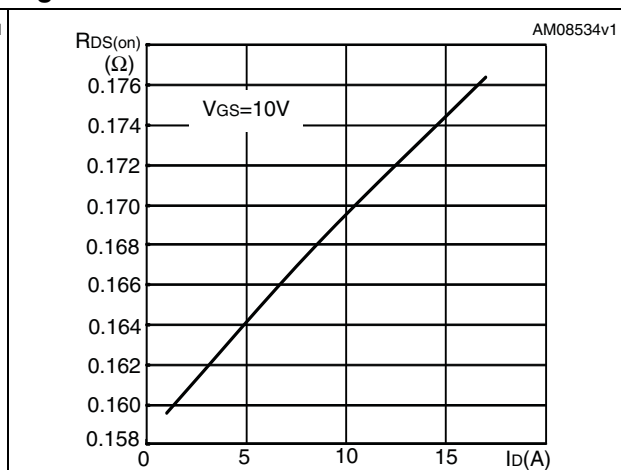


Figure 8. Capacitance variations

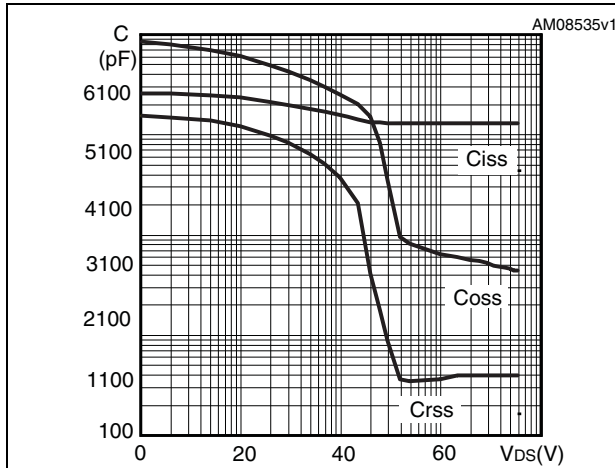


Figure 9. Output capacitance stored energy

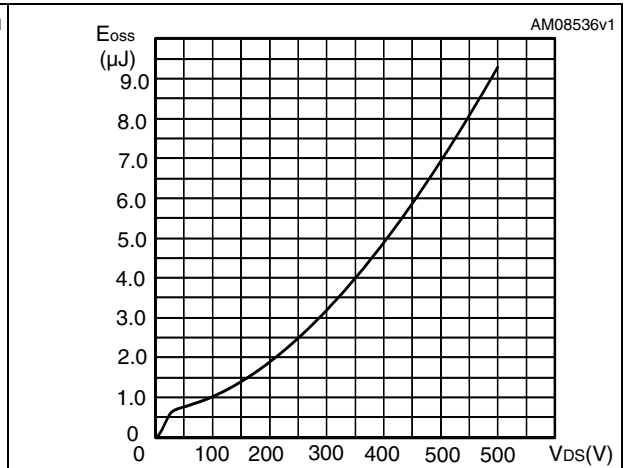


Figure 10. Normalized gate threshold voltage vs temperature

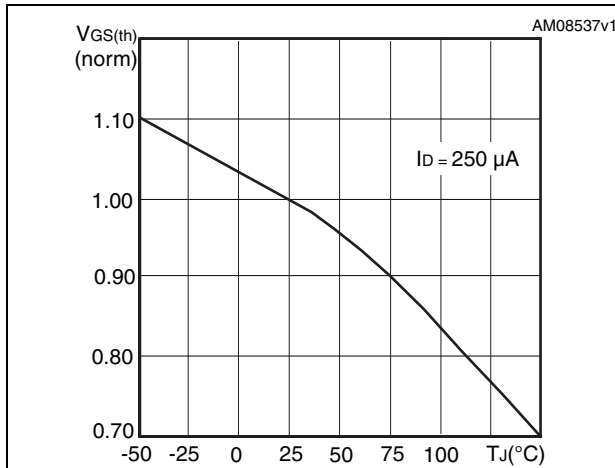


Figure 11. Normalized on resistance vs temperature

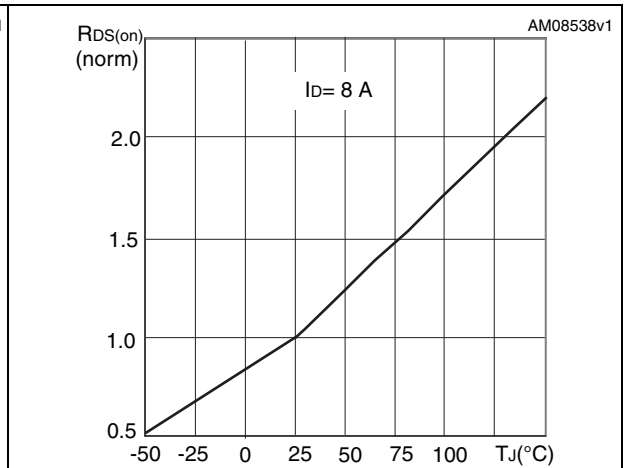


Figure 12. Normalized BV_{DSS} vs temperature

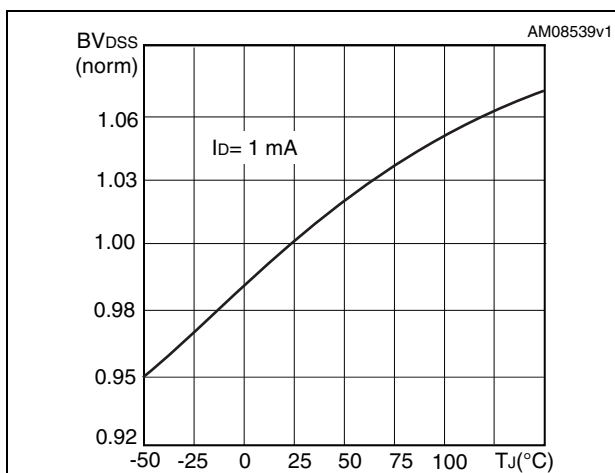
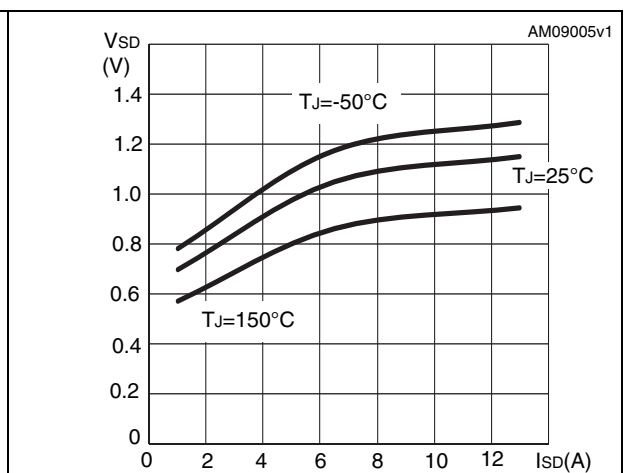


Figure 13. Source-drain diode forward characteristics



3 Test circuits

Figure 14. Switching times test circuit for resistive load



Figure 15. Gate charge test circuit

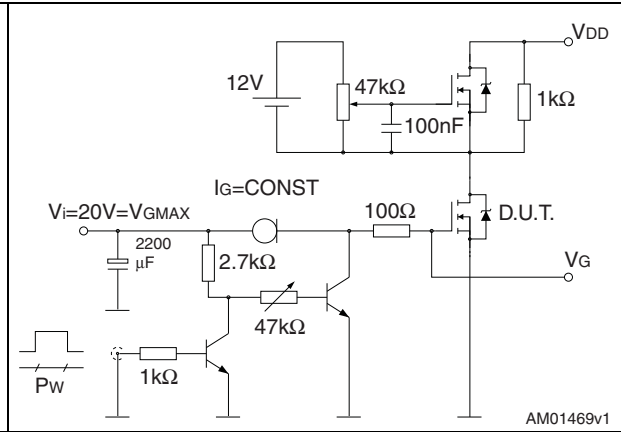


Figure 16. Test circuit for inductive load switching and diode recovery times



Figure 17. Unclamped inductive load test circuit

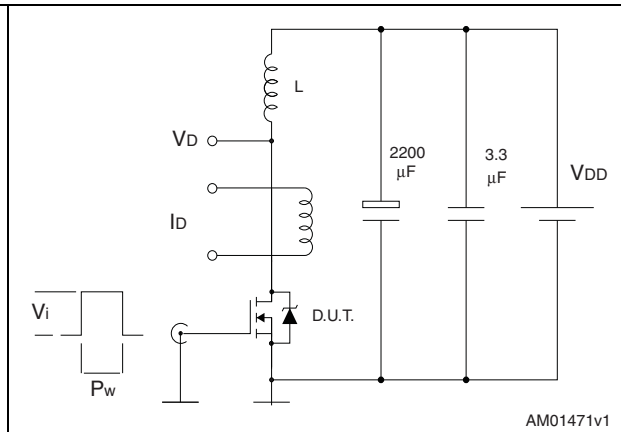


Figure 18. Unclamped inductive waveform

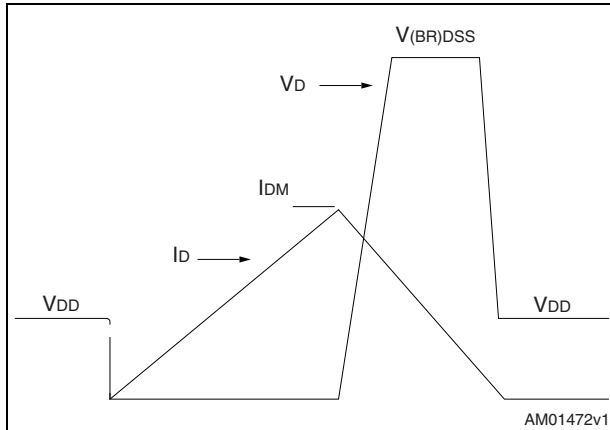
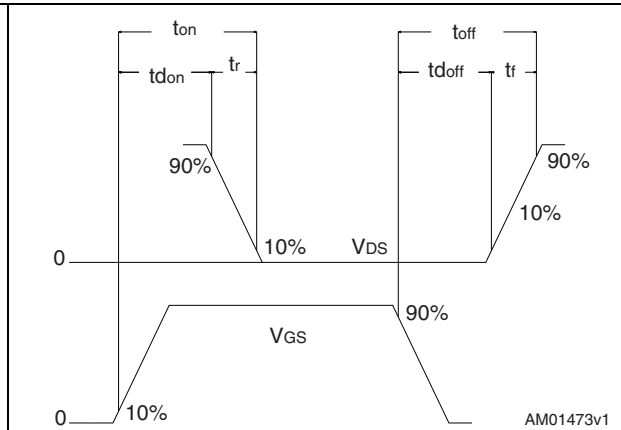


Figure 19. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. D²PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 20. D²PAK (TO-263) drawing

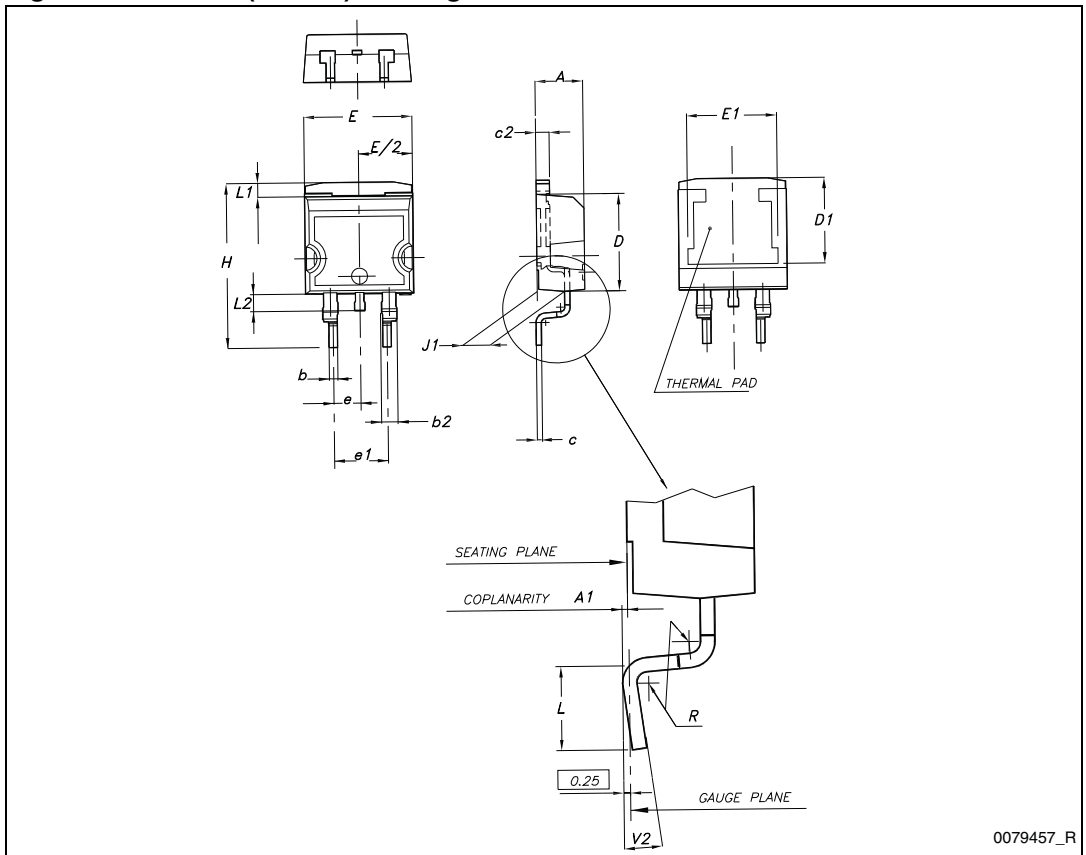
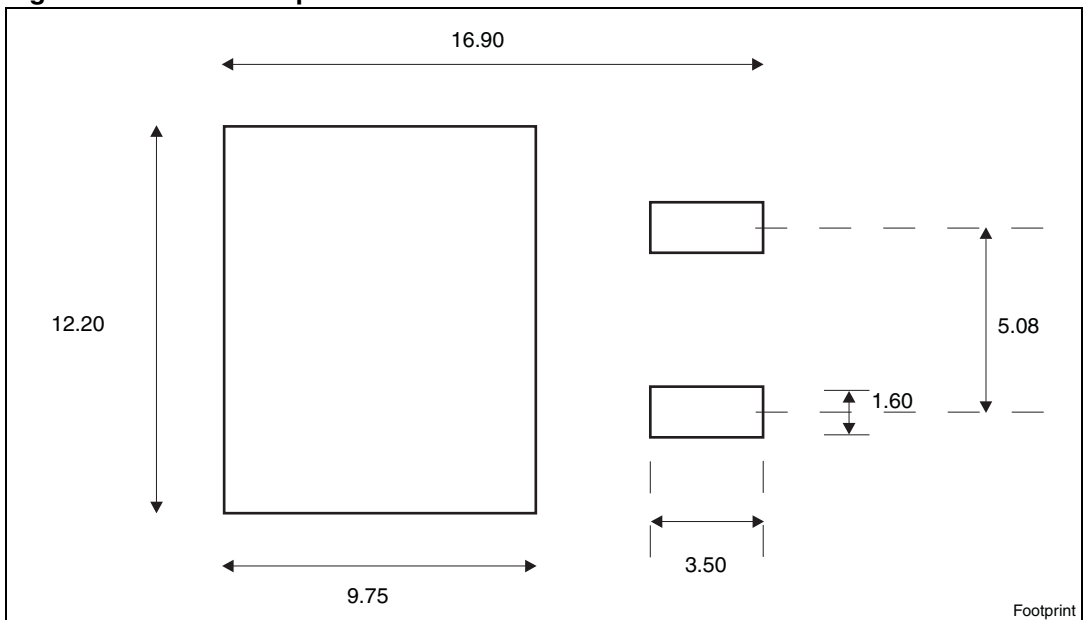


Figure 21. D²PAK footprint^(a)



a. All dimension are in millimeters

5 Packaging mechanical data

Table 10. D²PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Figure 22. Tape

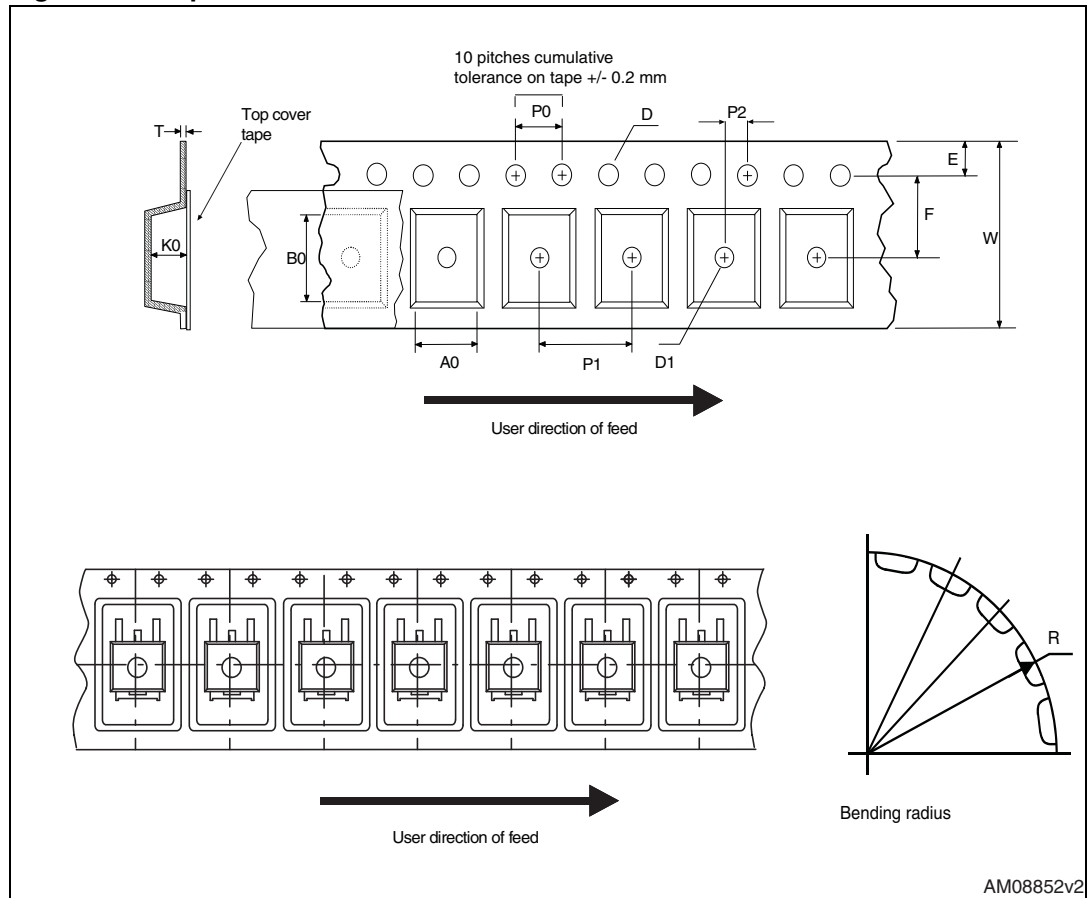
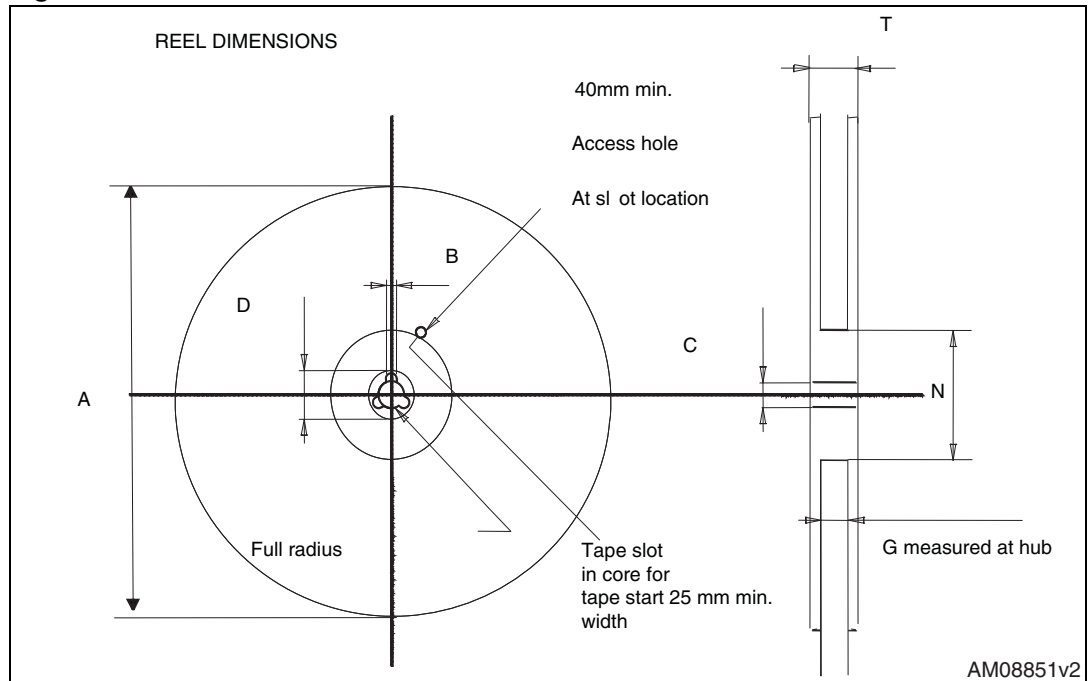


Figure 23. Reel



6 Revision history

Table 11. Document revision history

Date	Revision	Changes
23-Feb-2011	1	First release.

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