



# SM843256

## 10 Gigabit Ethernet and SONET, 6 output, Ultra-Low Jitter LVPECL Frequency Synthesizer

### General Description

The SM843256 provides a low-noise timing solution for high speed, high accuracy synthesis of clock signals. Common applications include SONET, Gigabit Ethernet, 10 Gigabit Ethernet, and similar networking standards. It includes a unique power reduction methodology, along with a patented RotaryWave™ architecture that provides a very stable clock with very low noise.

Power supplies of either 3.3V or 2.5V are supported, with superior jitter and phase noise performance. The device synthesizes different low noise LVPECL output frequencies such as 125MHz, 156.25MHz, 312.5MHz, and 625MHz for Ethernet applications; 77.76MHz, 155.52MHz, 311.04MHz, and 622.08MHz for SONET applications. The crystal reference frequencies used include 25MHz and 19.44Mhz for Ethernet and SONET applications, respectively.

The SM843256 is an excellent replacement for IDT Femto-clocks, with improved accuracy, power consumption, waveform integrity, and jitter.

Data sheets and support documentation can be found on Micrel's web site at: [www.micrel.com](http://www.micrel.com).

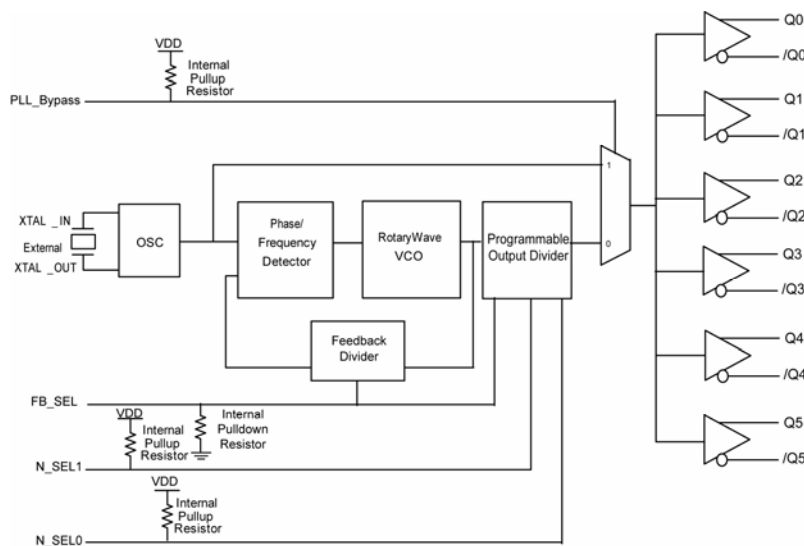
### Features

- Generates six LVPECL outputs
- 2.5V or 3.3V operating range
- Typical phase jitter @ 156.25MHz (1.875MHz to 20MHz): 80fs (typical) @ 3.3V
- 75MHz to 625MHz output frequencies
- Industrial temperature range
- Green, RoHS, and PFOS compliant
- Available in 24-pin TSSOP EPAD
- Operating supply modes:  
Core/Output  
3.3V/3.3V, 3.3V/2.5V, 2.5V/2.5V

### Applications

- SONET
- Gigabit Ethernet
- 10-Gigabit Ethernet
- Infiniband

### Block Diagram



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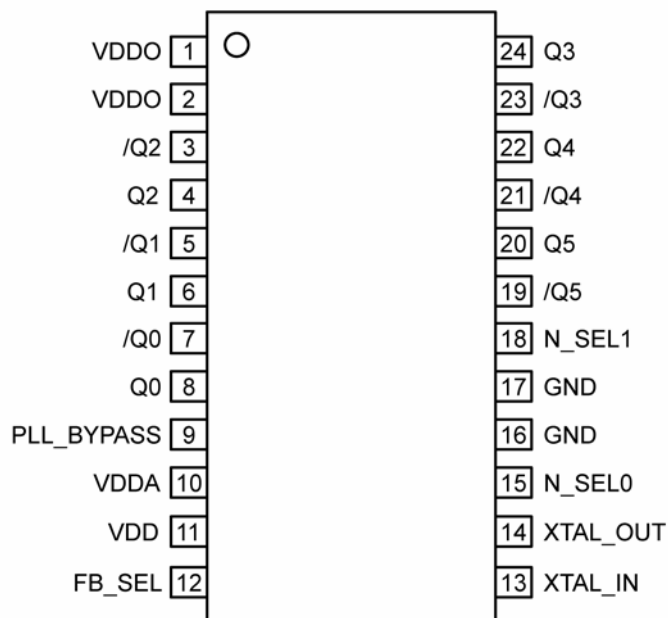
## Ordering Information<sup>(1, 2)</sup>

Part Number	Marking	Shipping	Junction Temperature Range	Package
SM843256KA	843256	Tube, Tape & Reel	-40° to +85°C	24-Pin TSSOP EPAD

**Notes:**

1. Devices are Green, RoHS, and PFOS Compliant.
2. Lead finish is 100% matte tin.

## Pin Configuration



**24-Pin TSSOP EPAD  
(Top View)**

## Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
1, 2	V <sub>DDO</sub>	PWR		2.5V or 3.3V Power Supply
3, 4	/Q2, Q2	O, (DIF)	LVPECL	Differential Clock Output
5, 6	/Q1, Q1	O, (DIF)	LVPECL	Differential Clock Output
7, 8	/Q0, Q0	O, (DIF)	LVPECL	Differential Clock Output
9	PLL_BYPASS	I, (SE)	LVC MOS	Pull-Up 45k, Single-Ended Input Select Pin. Logic (0) = PLL Output Logic (1) = Xtal Reference
10	V <sub>DDA</sub>	PWR		Analog 3.3V or 2.5V Power Supply
11	V <sub>DD</sub>	PWR		3.3V or 2.5V Power Supply
12	FB_SEL	I, (SE)	LVC MOS	Pull-Down 45k, Single-Ended Input Select Pin
13	XTAL_IN	I, (SE)	12pF crystal	Crystal Reference Input, no load caps needed.
14	XTAL_OUT	O, (SE)	12pF crystal	Crystal Reference Output, no load caps needed.
15	N_SEL0	I, (SE)	LVC MOS	Pull-Up 45k, Single-Ended Input Select Pin
16, 17	GND	PWR		Ground
18	N_SEL1	I, (SE)	LVC MOS	Pull-Up 45k, Single-Ended Input Select Pin
19, 20	/Q5, Q5	O, (DIF)	LVPECL	Differential Clock Output
21, 22	/Q4, Q4	O, (DIF)	LVPECL	Differential Clock Output
23, 24	/Q3, Q3	O, (DIF)	LVPECL	Differential Clock Output

## Input and Output Frequency Table

XTAL (MHz)	FB_SEL	N_SEL1	N_SEL0	Outputs (MHz)	Application
24	0	0	0	600	-
24	0	0	1	300	-
24	0	1	0	150	SAS/SATA
24	0	1	1	120	-
25	0	0	0	625	10 Gigabit Ethernet
25	0	0	1	312.50	10 Gigabit Ethernet
25	0	1	0	156.25	10 Gigabit Ethernet
25	0	1	1	125	Gigabit Ethernet/Infiniband/PCI/PCI-E/PCI-X
18.75	1	0	0	600	-
18.75	1	0	1	300	-
18.75	1	1	0	150	SAS/SATA
18.75	1	1	1	75	SAS/SATA
19.44	1	0	0	622.08	10 Gigabit Ethernet/SONET
19.44	1	0	1	311.04	SONET
19.44	1	1	0	155.52	SONET
19.44	1	1	1	77.76	SONET
19.53125	1	0	0	625	10 Gigabit Ethernet
19.53125	1	0	1	312.5	10 Gigabit Ethernet
19.53125	1	1	0	156.25	10 Gigabit Ethernet
19.53125	1	1	1	78.125	10 Gigabit Ethernet

**Absolute Maximum Ratings<sup>(1)</sup>**

Supply Voltage ( $V_{DDA}$ , $V_{DD}$ , $V_{DDO}$ )	+4.6V
Input Voltage ( $V_{IN}$ )	-0.50V to $V_{DD}+0.5V$
LVPECL Output Current ( $I_{OUT}$ )	
Continuous	50mA
Surge	100mA
Lead Temperature (soldering, 20sec.)	260°C
Case Temperature	115°C
Storage Temperature ( $T_s$ )	-65°C to +150°C

**Operating Ratings<sup>(2)</sup>**

Supply Voltage ( $V_{DDO}$ )	+2.375V to +3.465V
Supply Voltage ( $V_{DD}$ , $V_{DDA}$ )	+2.375V to +3.465V
Ambient Temperature ( $T_A$ )	-40°C to +85°C
Junction Thermal Resistance <sup>(3)</sup>	
TSSOP ( $\theta_{JA}$ )(Still Air)	32°C/W

**DC Electrical Characteristics<sup>(4)</sup>**

$V_{DDA} = V_{DD} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{DDO}$	2.5V Operating Voltage		2.375	2.5	2.625	V
$V_{DDA}, V_{DD}$	3.3V Operating Voltage		2.375	3.3	3.465	V
$I_{DDA}$	Analog Supply Range	$F_{OUT} = 156.25MHz$		55	65	mA
		$F_{OUT} = 625.00MHz$		56		
$I_{DD}$	Core Supply Current	$F_{OUT} = 156.25MHz$		13	17	mA
		$F_{OUT} = 625.00MHz$		13		
$I_{DDO}$	I/O Supply Range	$F_{OUT} = 156.25MHz$		235	TBD	mA
		$F_{OUT} = 625.00MHz$		330		

$V_{DDA} = V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{DDA}$ , $V_{DD}$ , $V_{DDO}$	3.3V Operating Voltage		3.135	3.3	3.465	V
$I_{DDA}$	Analog Supply Range	$F_{OUT} = 156.25MHz$		55	65	mA
		$F_{OUT} = 625.00MHz$		56		
$I_{DD}$	Core Supply Current	$F_{OUT} = 156.25MHz$		13	17	mA
		$F_{OUT} = 625.00MHz$		13		
$I_{DDO}$	I/O Supply Range	$F_{OUT} = 156.25MHz$		256	282	mA
		$F_{OUT} = 625.00MHz$		366		

**Notes:**

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

## LVPECL DC Electrical Characteristics<sup>(5, 6)</sup>

$V_{DDA} = V_{DD} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{DDO} = 2.5V$  or  $3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{OH}$	Output High Voltage	$50\Omega$ to $V_{DDO}-2V$	$V_{DDO}$ -1.145	$V_{DDO}$ -0.97	$V_{DDO}$ -0.845	V
$V_{OL}$	Output Low Voltage	$50\Omega$ to $V_{DDO}-2V$	$V_{DDO}$ -1.945	$V_{DDO}$ -1.77	$V_{DDO}$ -1.645	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing	Figure 1	0.6	0.8	1.0	V

## LVC MOS DC Electrical Characteristics<sup>(6)</sup>

$V_{DDA} = V_{DD} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{DDO} = 2.5V$  or  $3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{IH}$	Input High Voltage		2		$V_{DD}$ +0.3	V
$V_{IL}$	Input Low Voltage		-0.3		0.8	V
$I_{IH}$	Input High Current (FB_SEL)	$V_{DD} = V_{IN} = 3.465V$			150	$\mu A$
$I_{IH}$	Input High Current (PLL_BYPASS), (N_SEL0), (NSEL1)	$V_{DD} = V_{IN} = 3.465V$			5	$\mu A$
$I_{IL}$	Input Low Current (FB_SEL)	$V_{DD} = 3.465V$ , $V_{IN} = 0V$	-5			$\mu A$
$I_{IL}$	Input Low Current (PLL_BYPASS), (N_SEL0), (NSEL1)	$V_{DD} = 3.465V$ , $V_{IN} = 0V$	-150			$\mu A$

## AC Electrical Characteristics<sup>(7)</sup>

$V_{DDA} = V_{DD} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{DDO} = 2.5V$  or  $3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless noted.

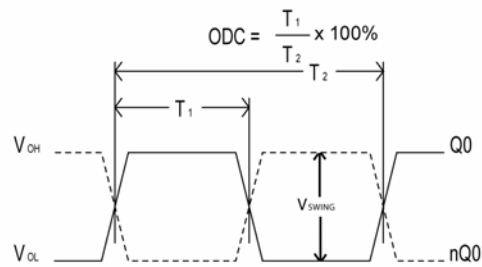
Symbol	Parameter	Condition	Min	Typ	Max	Units
$F_{OUT}$	Output Frequency	Refer to Frequency Table	75		625	MHz
$T_R/T_F$	LVPECL Output Rise/Fall Time	20% – 80%	100	175	350	ps
ODC	Output Duty Cycle		46	50	54	%
$T_{SKEW}$	Output-to-Output Skew	Note 8			45	ps
$T_{LOCK}$	PLL Lock Time				20	ms
$T_{jit}(\emptyset)$	RMS Phase Jitter (Output = 156.25 MHz)	Integration Range (12kHz – 20MHz)		251		fs
		Integration Range (1.875MHz – 20MHz)		80		fs

### Notes:

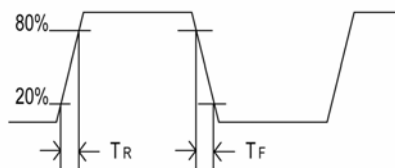
- See Figure 4 for load test circuit example.
- The circuit is designed to meet the DC specifications shown in the above table(s) after thermal equilibrium has been established.
- The circuit is designed to meet the AC specifications shown in the above table(s) after thermal equilibrium has been established.
- Defined as skew between outputs at the same supply voltage and with equal load conditions; Measured at the output differential crossing points.



**Phase Noise Plot: 156.25MHz @ 3.3V**



**Figure 1. Duty Cycle Timing**



**Figure 2. All Outputs Rise/Fall Time**

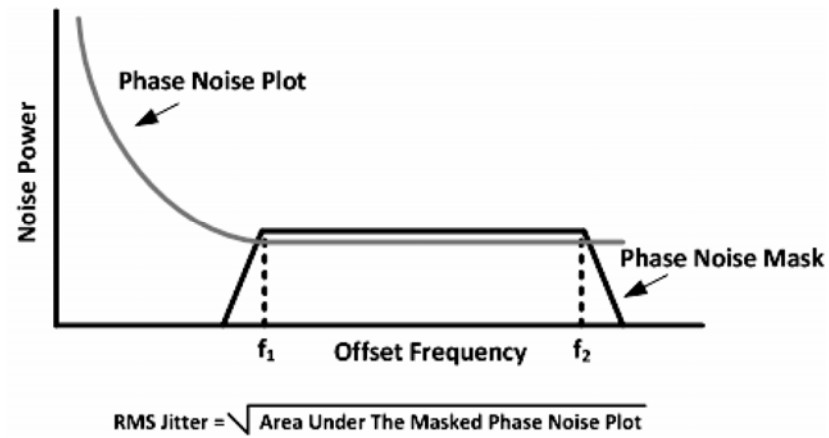


Figure 3. RMS Phase Noise/Jitter

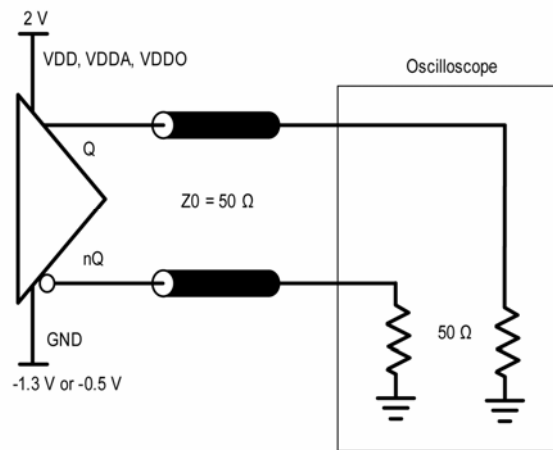


Figure 4. LVPECL Output Load and Test Circuit

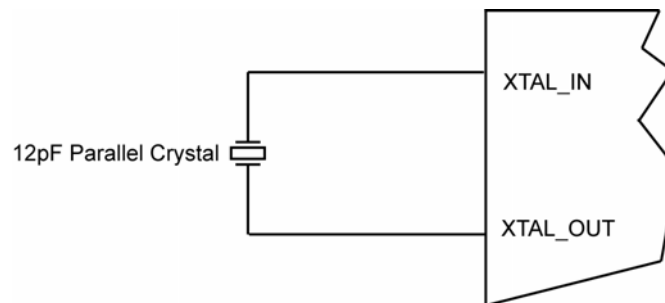
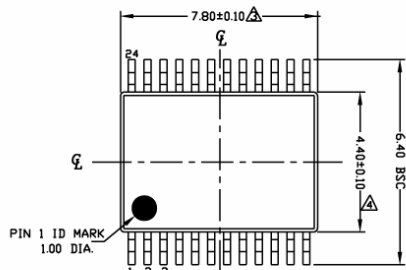
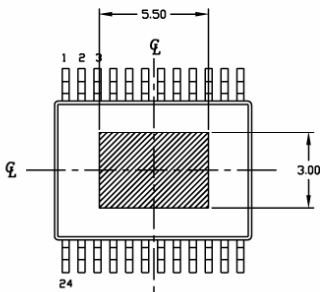


Figure 5. Crystal Input Interface

# Package Information

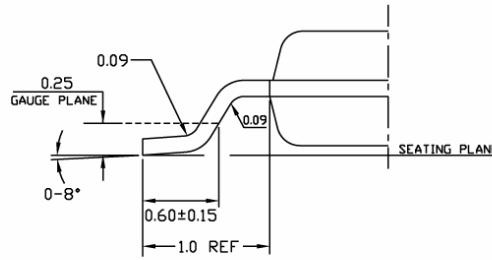


TOP VIEW

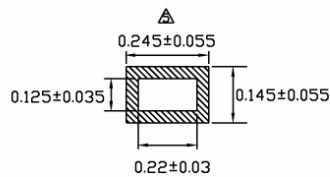


Exposed Pad

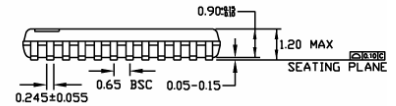
BOTTOM VIEW



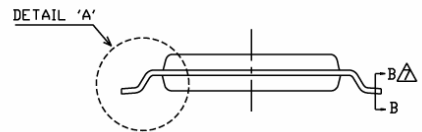
DETAIL 'A'



DETAIL 'B-B'



SIDE VIEW



END VIEW

**NOTES:**

1. DIMENSIONS ARE IN MM.
2. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M-1994.
3. DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURR.
4. DIMENSION 'E1' DOES NOT INCLUDE INTERNAL FLASH OR PROTRUSION.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION.
6. "N" IS THE MAXIMUM NUMBER OF LEAD TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. CROSS SECTION B-B TO BE DETERMINED AT 0.10 TO 0.25mm FROM THE LEAD TIP

**24-pin EPAD TSSOP**

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