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UHF linear push-pull power transistor

BLV62

FEATURES

- Internal matching for an optimum wideband capability and high gain
- Poly-siticon emitter-ballasting resistors for an optimum temperature profile
- Gold metallization ensures excellent reliability.

DESCRIPTION

Two npn silicon planar epitaxial sections in push-pull structure, intended for use in linear television transmitters (vision or sound).

The device is encapsulated in a 4-lead SOT262A2 flange envelope with 2 ceramic caps. The common emitter is connected to the flange.

PINNING - SOT262A2

PIN	DESCRIPTION
1	collector 1
2	collector 2
3	base 1
4	base 2
5	emitter

QUICK REFERENCE DATA

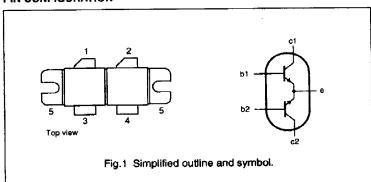
RF performance at $T_h = 25$ °C in a common emitter test circuit.

MODE OF OPERATION	f (MHz)	V _{CE} (V)	P _L (W)	G _p (dB)	Դ _շ (%)	ΔG _p (dB) (note 1)
c.w. class-AB	860	28	150	> 8.5 typ. 9.5	> 45 typ. 50	< 1 typ. 0.5

Note

 Assuming a 3rd order amplitude transfer characteristic, 1 dB gain compression corresponds with 30% sync input/25% sync output compression in television service (negative modulation, CCIR system).

PIN CONFIGURATION



NJ Semi-Conductors reserves the right to change test conditions, parameter limits and package dimensions without notice. Information furnished by NJ Semi-Conductors is believed to be both accurate and reliable at the time of going to press. However, NJ Semi-Conductors assumes no responsibility for any errors or omissions discovered in its use. NJ Semi-Conductors encourages customers to verify that datasheets are current before placing orders.

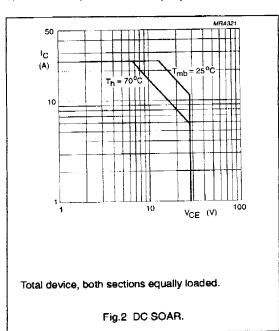
LIMITING VALUES (per transistor section unless otherwise specified)

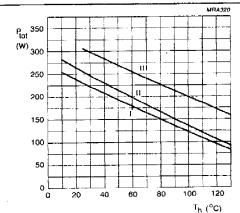
In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CBO}	collector-base voltage	open emitter	_	60	V
V _{CEO}	collector-emitter voltage	open base	-	28	٧
V _{EBO}	emitter-base voltage	open collector	-	3	V
c, Iciavi	collector current	DC or average value	-	12.5	Α
P _{tot}	total power dissipation	DC operation; T _{mb} = 25 °C (note 1)	_	320	w
T _{etg}	storage temperature range		65	150	°C
<u>ац</u> Г.	junction operating temperature		-	200	°C

Note

1. Total device, both sections equally loaded.





Total device, both sections equally loaded.

- (I) Continuous DC operation.
- (II) Continuous RF operation.
- (III) Short time operation during mismatch.

Fig.3 Power/temperature derating curve.

THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
R _{th j-mb(DC)}	from junction to mounting base	P _{tot} = 320 W; T _{mb} = 25 °C (note 1)	0.55	kw
R _{th j-mb(RF)}	from junction to mounting base	P _{lot} = 350 W; T _{mb} = 25 °C (note 1)	0.5	K/W
R _{th mb-h}	from mounting base to heatsink	(note 1)	0.15	KW

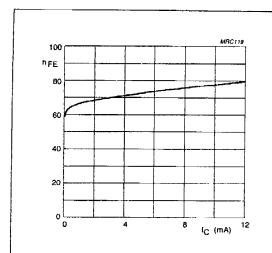
Note

1. Total device, both sections equally loaded.

CHARACTERISTICS

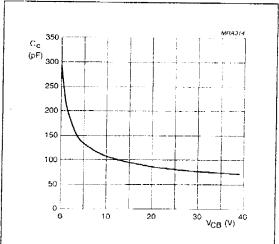
Values apply to either transistor section; $T_i = 25$ °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{(BR)CBO}	collector-base breakdown voltage	open emitter; l _c = 60 mA	60	-	-	٧
V _{(BR)CEO}	collector-emitter breakdown voltage	open base; I _C = 150 mA	28	-	-	V
V _{(BR)EBO}	emitter-base breakdown voltage	open collector; I _E = 3 mA	3	-	-	V
I _{CES}	collector-emitter leakage current	V _{BE} = 0; V _{CE} = 28 V	-	-	30	mA
h _{eE}	DC current gain	V _{CE} = 25 V; I _C = 4.5 A	30	-	-	
Δh _{FE}	DC current gain ratio of both sections	V _{CE} = 25 V; I _C = 4.5 A	0.67	-	1.5	
C _c	collector capacitance	V _{CB} = 28 V; _E = I _o = 0; f = 1 MHz	-	81	-	pF
C _{c-1}	collector-flange capacitance	f = 1 MHz	-	5.7	_	ρF



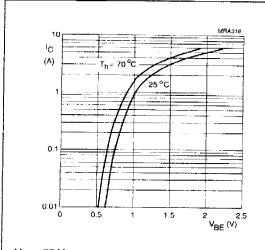
V_{CE} = 25 V.

Fig.4 DC current gain as a function of collector current, typical values.



 $I_E = I_e = 0$; f = 1 MHz.

Fig.5 Collector capacitance as a function of collector-base voltage, typical values.



V_{CE} = 25 V.

Fig.6 Collector current as a function of base-emitter voltage, typical values.