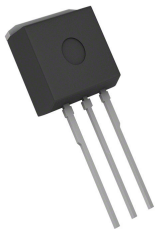
KERSEMI ELECTRONIC CO.,LTD.

# IRF1404S
# IRF1404L

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated

$D^2$Pak
IRF1404S

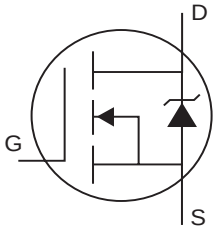
TO-262
IRF1404L



## Description

The $D^2$Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The $D^2$Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.
The through-hole version (IRF1404L) is available for low-profile applications.

Power MOSFET




$V_{DSS}$ = 40V

$R_{DS(on)}$ = 0.004Ω

$I_D$ = 162A⑥

## Absolute Maximum Ratings

| | Parameter | Max. | Units |
|---|---|---|---|
| $I_D$ @ $T_C$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10V⑦ | 162⑥ | A |
| $I_D$ @ $T_C$ = 100°C | Continuous Drain Current, $V_{GS}$ @ 10V⑦ | 115⑥ | |
| $I_{DM}$ | Pulsed Drain Current ①⑦ | 650 | |
| $P_D$ @$T_A$ = 25°C | Power Dissipation | 3.8 | W |
| $P_D$ @$T_C$ = 25°C | Power Dissipation | 200 | W |
| | Linear Derating Factor | 1.3 | W/°C |
| $V_{GS}$ | Gate-to-Source Voltage | ± 20 | V |
| $E_{AS}$ | Single Pulse Avalanche Energy⑦ | 519 | mJ |
| $I_{AR}$ | Avalanche Current① | 95 | A |
| $E_{AR}$ | Repetitive Avalanche Energy① | 20 | mJ |
| dv/dt | Peak Diode Recovery dv/dt ③⑦ | 5.0 | V/ns |
| $T_J$ | Operating Junction and | -55 to +175 | °C |
| $T_{STG}$ | Storage Temperature Range | -55 to +175 | |
| | Soldering Temperature, for 10 seconds | 300 (1.6mm from case ) | |

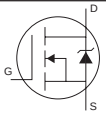
## Thermal Resistance

| | Parameter | Typ. | Max. | Units |
|---|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-Case | —— | 0.75 | °C/W |
| $R_{\theta JA}$ | Junction-to-Ambient (PCB mounted, steady-state)* | —— | 40 | |

## Electrical Characteristics @ $T_J$ = 25°C (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 40 | —— | —— | V | $V_{GS}$ = 0V, $I_D$ = 250μA |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | —— | 0.036 | —— | V/°C | Reference to 25°C, $I_D$ = 1mA |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | —— | 0.0035 | 0.004 | Ω | $V_{GS}$ = 10V, $I_D$ = 95A ④ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 2.0 | —— | 4.0 | V | $V_{DS}$ = 10V, $I_D$ = 250μA |
| $g_{fs}$ | Forward Transconductance | 106 | —— | —— | S | $V_{DS}$ = 25V, $I_D$ = 60A⑦ |
| $I_{DSS}$ | Drain-to-Source Leakage Current | —— | —— | 20 | μA | $V_{DS}$ = 40V, $V_{GS}$ = 0V |
| | | —— | —— | 250 | | $V_{DS}$ = 32V, $V_{GS}$ = 0V, $T_J$ = 150°C |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | —— | —— | 200 | nA | $V_{GS}$ = 20V |
| | Gate-to-Source Reverse Leakage | —— | —— | -200 | | $V_{GS}$ = -20V |
| $Q_g$ | Total Gate Charge | —— | 160 | 200 | nC | $I_D$ = 95A |
| $Q_{gs}$ | Gate-to-Source Charge | —— | 35 | —— | | $V_{DS}$ = 32V |
| $Q_{gd}$ | Gate-to-Drain ("Miller") Charge | —— | 42 | 60 | | $V_{GS}$ = 10V ④⑦ |
| $t_{d(on)}$ | Turn-On Delay Time | —— | 17 | —— | ns | $V_{DD}$ = 20V |
| $t_r$ | Rise Time | —— | 140 | —— | | $I_D$ = 95A |
| $t_{d(off)}$ | Turn-Off Delay Time | —— | 72 | —— | | $R_G$ = 2.5Ω |
| $t_f$ | Fall Time | —— | 26 | —— | | $R_D$ = 0.21Ω ④⑦ |
| $L_S$ | Internal Source Inductance | —— | 7.5 | —— | nH | Between lead, and center of die contact |
| $C_{iss}$ | Input Capacitance | —— | 7360 | —— | pF | $V_{GS}$ = 0V |
| $C_{oss}$ | Output Capacitance | —— | 1680 | —— | | $V_{DS}$ = 25V |
| $C_{rss}$ | Reverse Transfer Capacitance | —— | 240 | —— | | $f$ = 1.0MHz, See Fig. 5 ⑦ |
| $C_{oss}$ | Output Capacitance | —— | 6630 | —— | | $V_{GS}$ = 0V, $V_{DS}$ = 1.0V, $f$ = 1.0MHz |
| $C_{oss}$ | Output Capacitance | —— | 1490 | —— | | $V_{GS}$ = 0V, $V_{DS}$ = 32V, $f$ = 1.0MHz |
| $C_{oss}$ eff. | Effective Output Capacitance ⑤⑦ | —— | 1540 | —— | | $V_{GS}$ = 0V, $V_{DS}$ = 0V to 32V |

## Source-Drain Ratings and Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current (Body Diode) | —— | —— | 162⑥ | A | MOSFET symbol showing the integral reverse p-n junction diode.  |
| $I_{SM}$ | Pulsed Source Current (Body Diode) ① | —— | —— | 650 | | |
| $V_{SD}$ | Diode Forward Voltage | —— | —— | 1.3 | V | $T_J$ = 25°C, $I_S$ = 95A, $V_{GS}$ = 0V ④ |
| $t_{rr}$ | Reverse Recovery Time | —— | 71 | 110 | ns | $T_J$ = 25°C, $I_F$ = 95A |
| $Q_{rr}$ | Reverse RecoveryCharge | —— | 180 | 270 | nC | di/dt = 100A/μs ④⑦ |
| $t_{on}$ | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$+$L_D$) | | | | |

**Notes:**

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting $T_J$ = 25°C, L = 0.12mH $R_G$ = 25Ω, $I_{AS}$ = 95A. (See Figure 12)

③ $I_{SD}$ ≤ 95A, di/dt ≤ 150A/μs, $V_{DD}$ ≤ $V_{(BR)DSS}$, $T_J$ ≤ 175°C

④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

⑤ $C_{oss}$ eff. is a fixed capacitance that gives the same charging time as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80% $V_{DSS}$

⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A

⑦ Use IRF1404 data and test conditions.

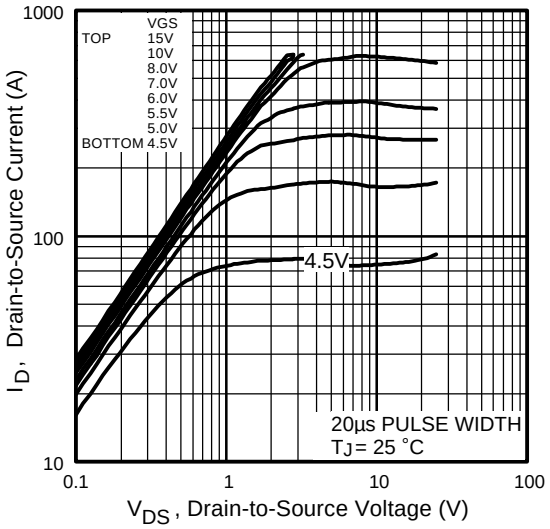



**Fig 1.** Typical Output Characteristics

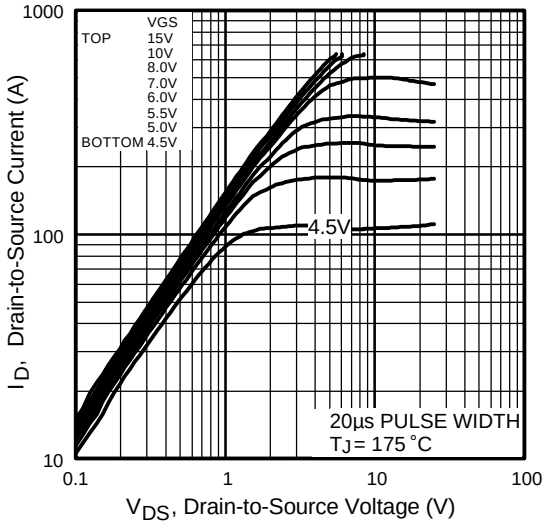



**Fig 2.** Typical Output Characteristics

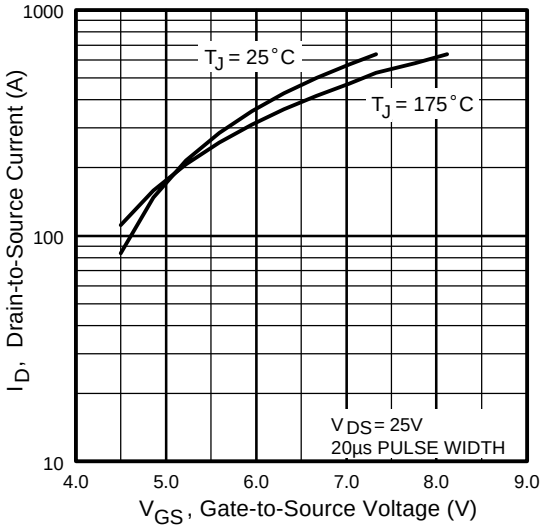



**Fig 3.** Typical Transfer Characteristics

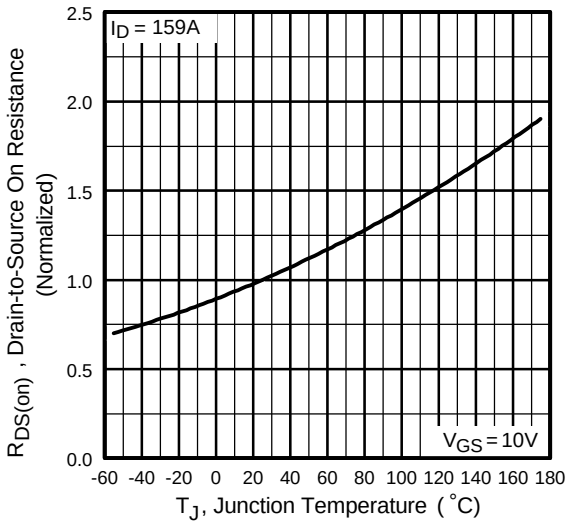



**Fig 4.** Normalized On-Resistance Vs. Temperature

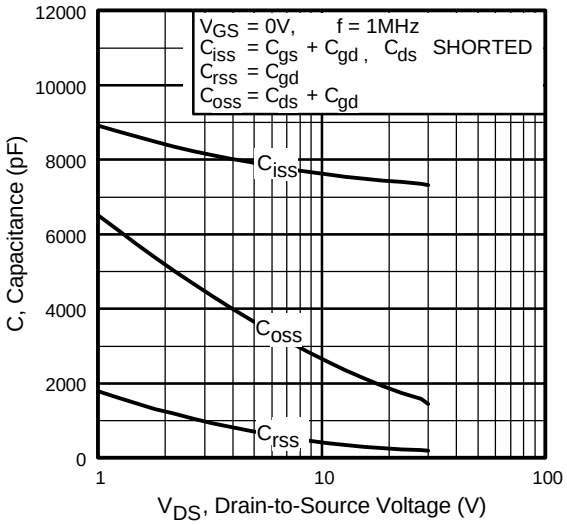



**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage

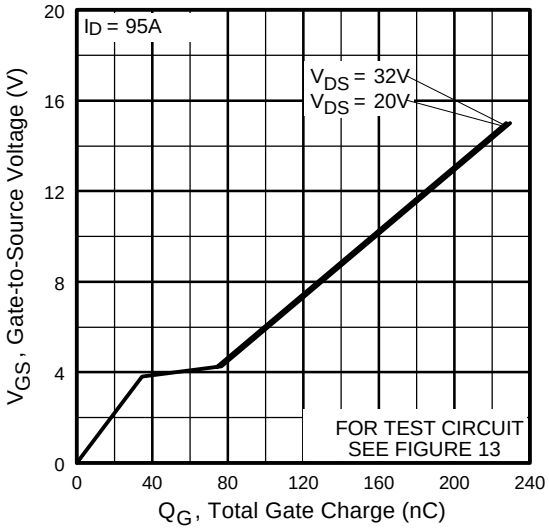



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage

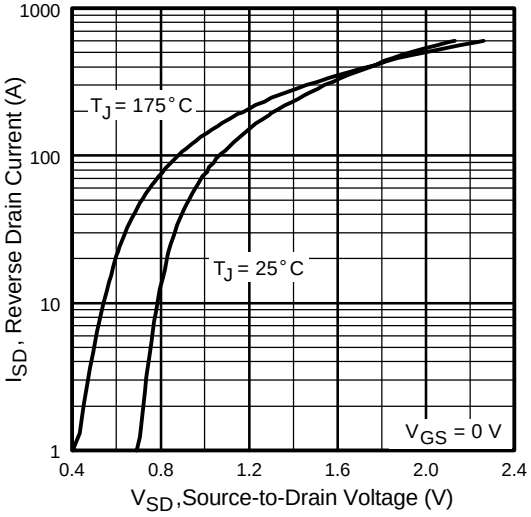



**Fig 7.** Typical Source-Drain Diode Forward Voltage

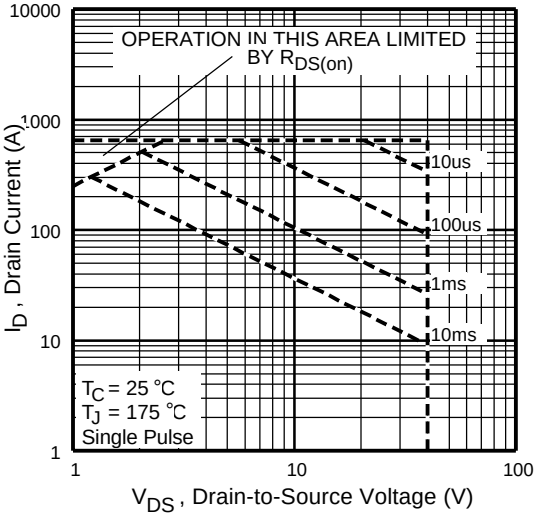



**Fig 8.** Maximum Safe Operating Area

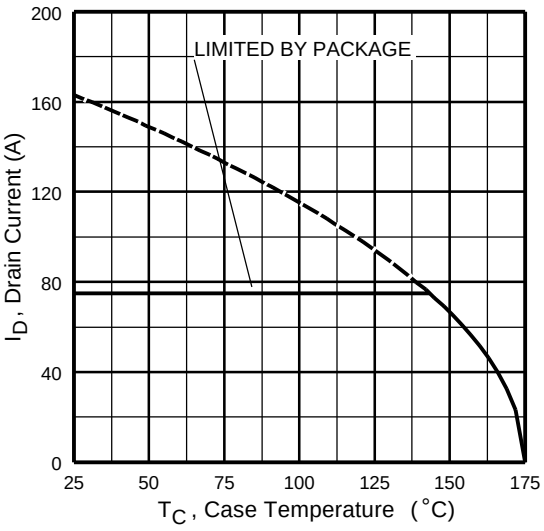



**Fig 9.** Maximum Drain Current Vs. Case Temperature

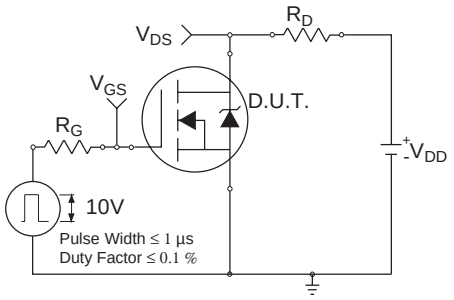



**Fig 10a.** Switching Time Test Circuit

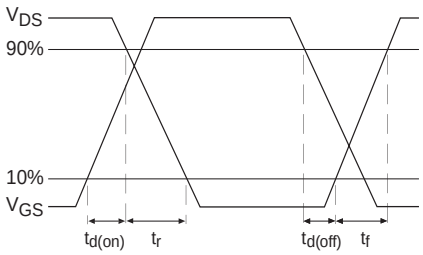



**Fig 10b.** Switching Time Waveforms

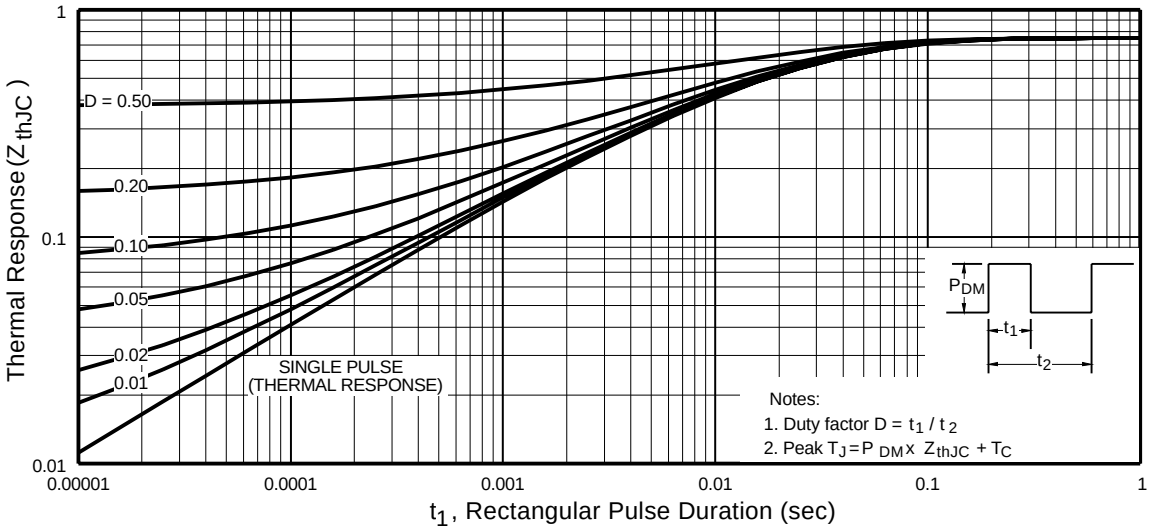



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

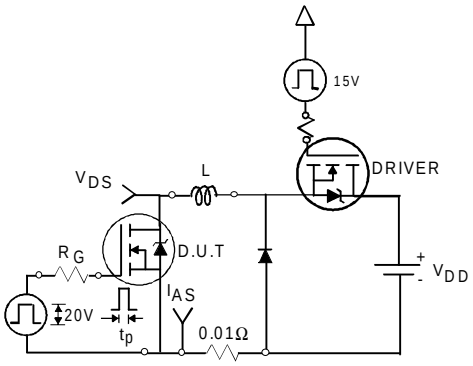



**Fig 12a.** Unclamped Inductive Test Circuit

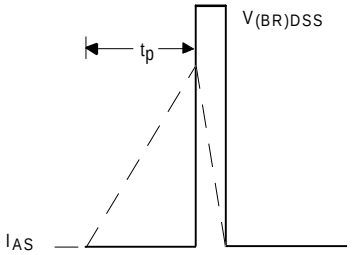



**Fig 12b.** Unclamped Inductive Waveforms

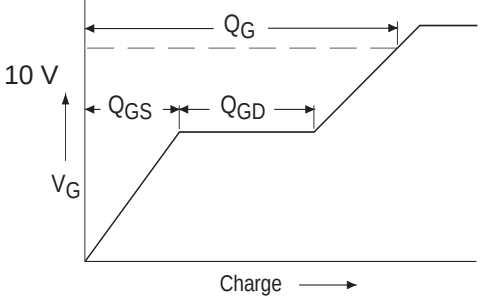



**Fig 13a.** Basic Gate Charge Waveform

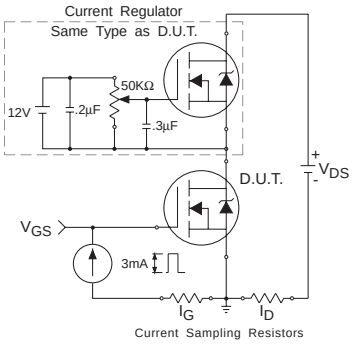



**Fig 13b.** Gate Charge Test Circuit

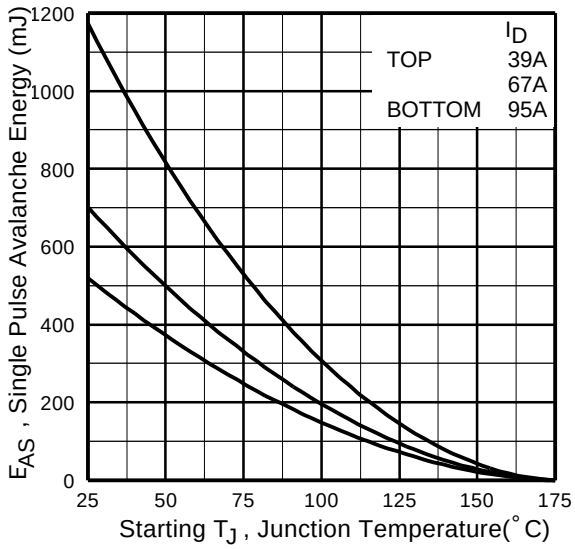



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

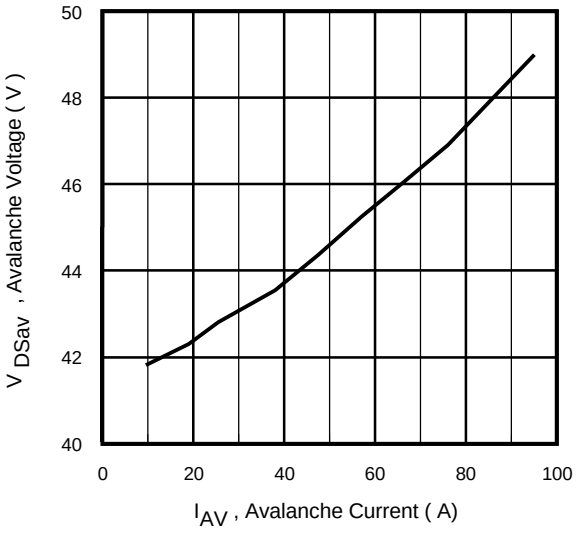
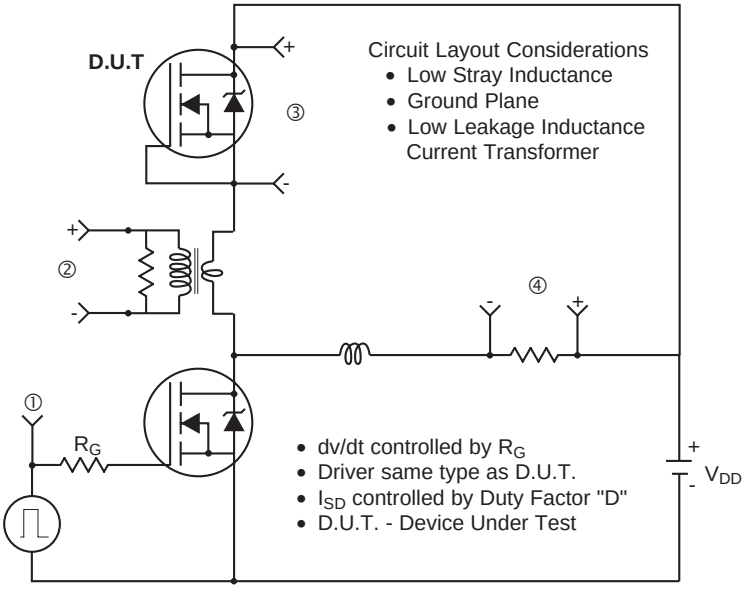
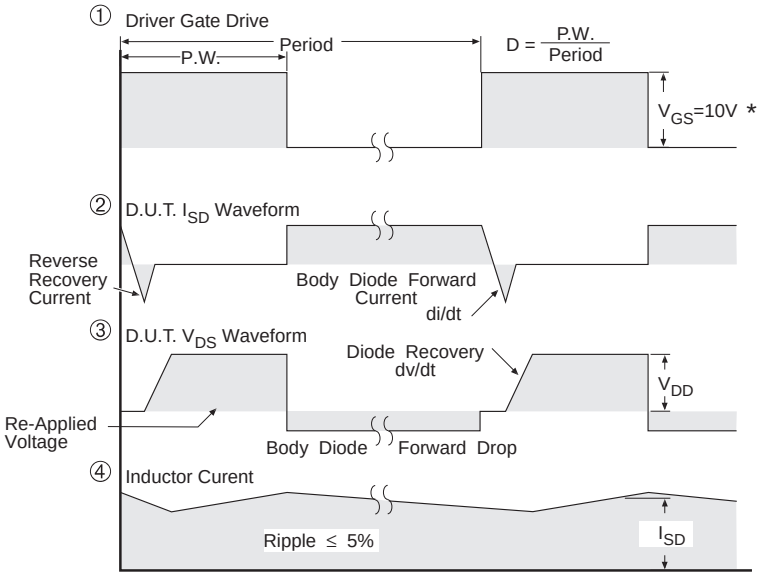



**Fig 12d.** Typical Drain-to-Source Voltage Vs. Avalanche Current

## Peak Diode Recovery dv/dt Test Circuit

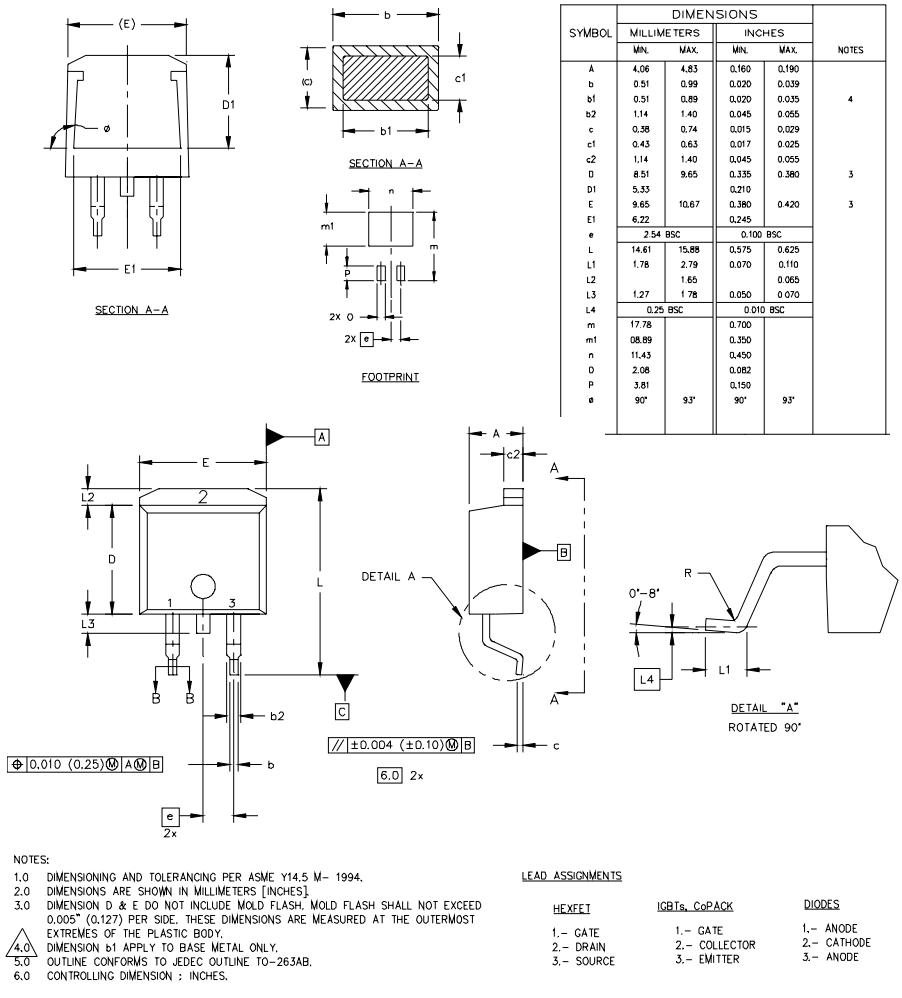



* $V_{GS}$ = 5V for Logic Level Devices

**Fig 14.** For N-channel HEXFET® Power MOSFETs

## D²Pak Package Outline




| SYMBOL | DIMENSIONS | | | | NOTES |
|---|---|---|---|---|---|
| | MILLIMETERS | | INCHES | | |
| | MIN. | MAX. | MIN. | MAX. | |
| A | 4.06 | 4.83 | 0.160 | 0.190 | |
| b | 0.51 | 0.99 | 0.020 | 0.039 | |
| b1 | 0.51 | 0.89 | 0.020 | 0.035 | 4 |
| b2 | 1.14 | 1.40 | 0.045 | 0.055 | |
| c | 0.38 | 0.74 | 0.015 | 0.029 | |
| c1 | 0.43 | 0.63 | 0.017 | 0.025 | |
| c2 | 1.14 | 1.40 | 0.045 | 0.055 | |
| D | 8.51 | 9.65 | 0.335 | 0.380 | 3 |
| D1 | 5.33 | | 0.210 | | |
| E | 9.65 | 10.67 | 0.380 | 0.420 | 3 |
| E1 | 6.22 | | 0.245 | | |
| e | 2.54 BSC | | 0.100 BSC | | |
| L | 14.61 | 15.88 | 0.575 | 0.625 | |
| L1 | 1.78 | 2.79 | 0.070 | 0.110 | |
| L2 | | 1.65 | | 0.065 | |
| L3 | 1.27 | 1.78 | 0.050 | 0.070 | |
| L4 | 0.25 BSC | | 0.010 BSC | | |
| m | 17.78 | | 0.700 | | |
| m1 | 08.89 | | 0.350 | | |
| n | 11.43 | | 0.450 | | |
| Q | 2.08 | | 0.082 | | |
| P | 3.81 | | 0.150 | | |
| ø | 90° | 93° | 90° | 93° | |

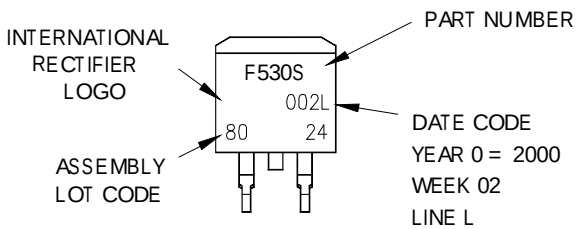
NOTES:
1.0 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M– 1994.
2.0 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
4.0 DIMENSION b1 APPLY TO BASE METAL ONLY.
5.0 OUTLINE CONFORMS TO JEDEC OUTLINE TO–263AB.
6.0 CONTROLLING DIMENSION : INCHES.

LEAD ASSIGNMENTS

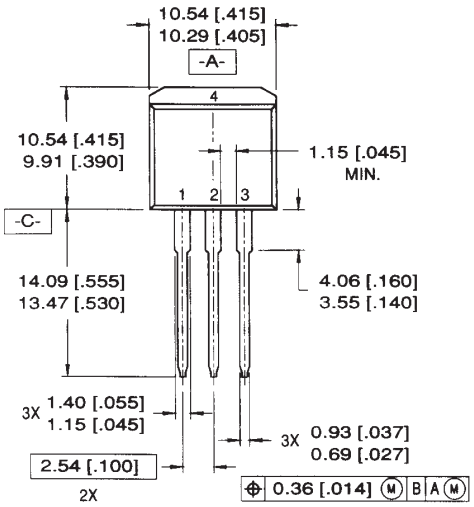
| HEXFET | IGBTs, CoPACK | DIODES |
|---|---|---|
| 1.– GATE | 1.– GATE | 1.– ANODE |
| 2.– DRAIN | 2.– COLLECTOR | 2.– CATHODE |
| 3.– SOURCE | 3.– EMITTER | 3.– ANODE |

## D²Pak Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"



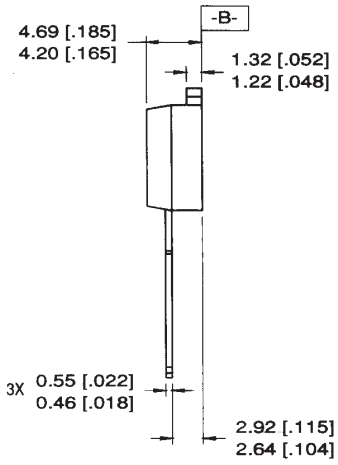
## TO-262 Package Outline




LEAD ASSIGNMENTS

1 = GATE 3 = SOURCE

2 = DRAIN 4 = DRAIN

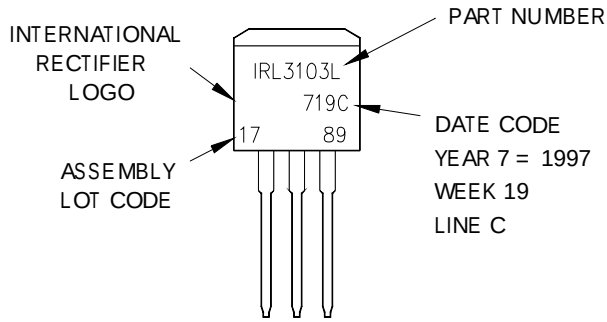



NOTES:

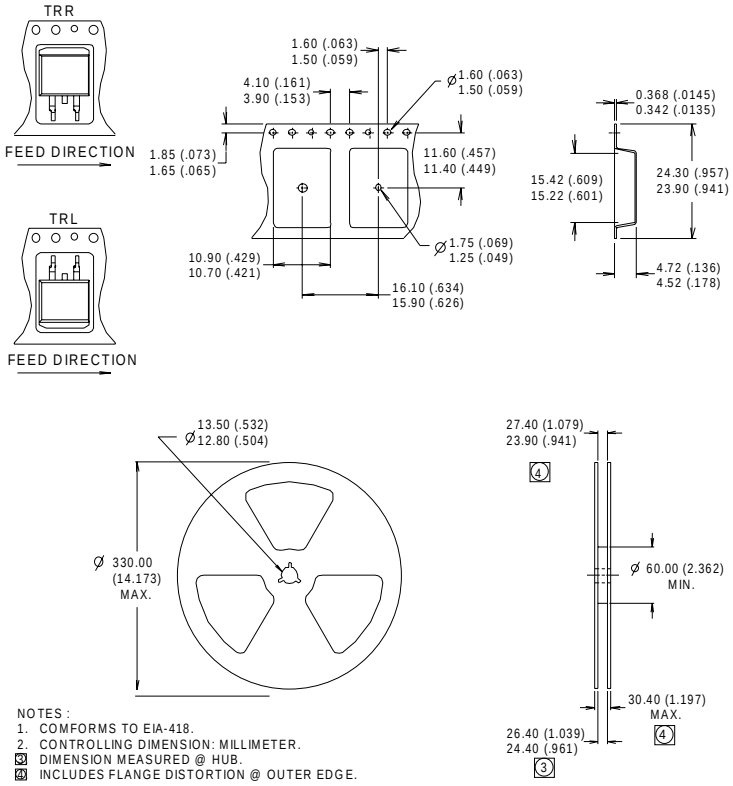
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

## TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



## D$^2$Pak Tape & Reel Information




NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION MEASURED @ HUB.
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.