# SI3909D

## CHARACTERISTICS

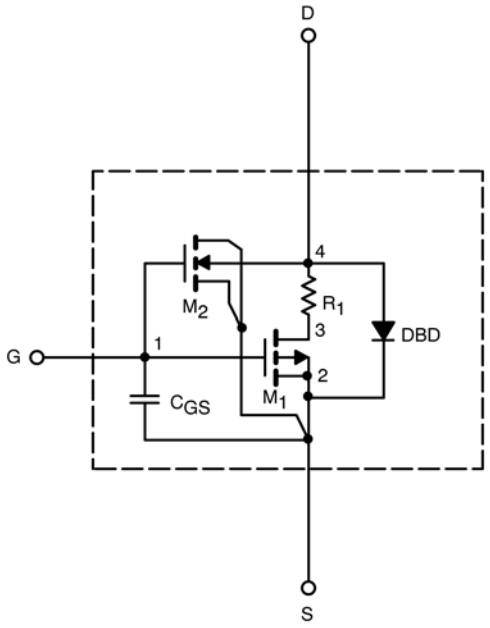
- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the −55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

## DESCRIPTION

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the −55 to 125°C temperature ranges under the pulsed 0-V to 5-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{gd}$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

## SUBCIRCUIT MODEL SCHEMATIC




This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

# SI3909D

| SPECIFICATIONS ($T_J$ = 25°C UNLESS OTHERWISE NOTED) | | | | | |
|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Test Condition** | **Simulated Data** | **Measured Data** | **Unit** |
| **Static** | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = – 250 μA | 1.1 | | V |
| On-State Drain Current[a] | $I_{D(on)}$ | $V_{DS}$ = –5 V, $V_{GS}$ = –4.5 V | 14 | | A |
| Drain-Source On-State Resistance[a] | $r_{DS(on)}$ | $V_{GS}$ = –4.5 V, $I_D$ = – 1.8 A | 0.18 | 0.16 | Ω |
| | | $V_{GS}$ = –3.6 V, $I_D$ = –1.6 A | 0.19 | 0.19 | |
| | | $V_{GS}$ = –2.5 V, $I_D$ = –1 A | 0.25 | 0.28 | |
| Forward Transconductance[a] | $g_{fs}$ | $V_{DS}$ = –10 V, $I_D$ = –1.8 A | 3.6 | 3.6 | S |
| Diode Forward Voltage[a] | $V_{SD}$ | $I_S$ = –1.05 A, $V_{GS}$ = 0 V | –0.78 | –0.83 | V |
| **Dynamic[b]** | | | | | |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = –10 V, $V_{GS}$ = –4.5 V, $I_D$ = –1.8 A | 2.5 | 2.7 | nC |
| Gate-Source Charge | $Q_{gs}$ | | 0.40 | 0.40 | |
| Gate-Drain Charge | $Q_{gd}$ | | 0.60 | 0.60 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = –10 V, $R_L$ = 10 Ω<br>$I_D \cong$ –1 A, $V_{GEN}$ = –4.5 V, $R_G$ = 6 Ω | 10 | 11 | ns |
| Rise Time | $t_r$ | | 8 | 34 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | 52 | 19 | |
| Fall Time | $t_f$ | | 7 | 24 | |
| Source-Drain Reverse Recovery Time | $t_{rr}$ | $I_F$ = –1.05 A, di/dt = 100 A/μs | 20 | 20 | |

Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.