

OKI semiconductor

MSM514400

1,048,576-Word x 4-Bit DYNAMIC RAM: FAST PAGE MODE TYPE

GENERAL DESCRIPTION

The MSM514400 is a new generation dynamic RAM organized as 1,048,576-word x 4-bit. The technology used to fabricate the MSM514400 is OKI's CMOS silicon gate process technology. The device operates at a single +5 V power supply. Its I/O pins are TTL compatible.

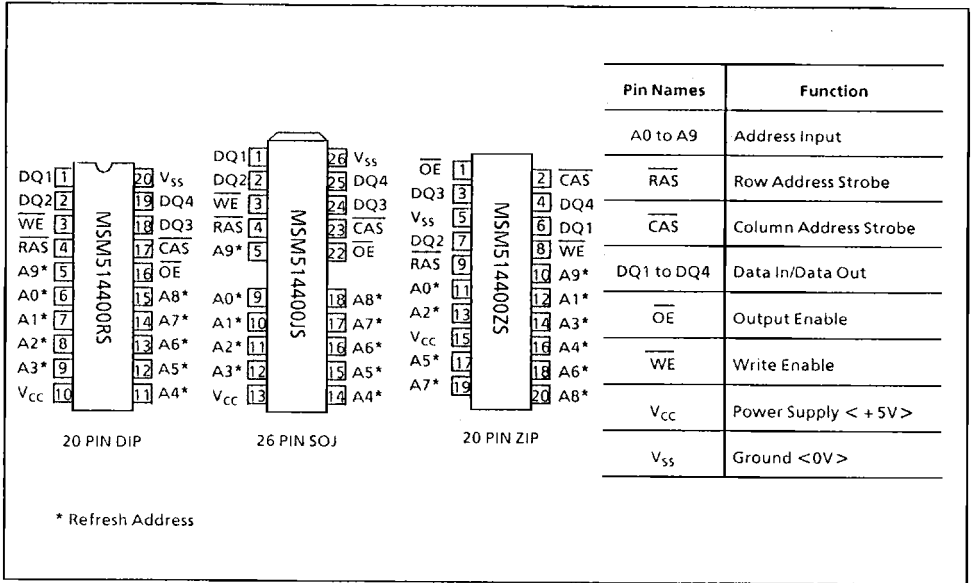
FEATURES

- Silicon gate, quadruple polysilicon CMOS, 1 transistor memory cell
- 1,048,576-word x 4-bit organization
- 350 mil 26-pin plastic SOJ, 400 mil 20-pin plastic ZIP, 400 mil 20-pin plastic DIP
- Single +5 V power supply, $\pm 10\%$ tolerance
- Input: TTL compatible
- Output: TTL compatible, tristate, nonlatch
- Refresh: 1024 cycles/16 ms
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ hidden refresh, $\overline{\text{RAS}}$ -only refresh capability
- Multibit test mode capability
- Built-in V_{BB} generator circuit

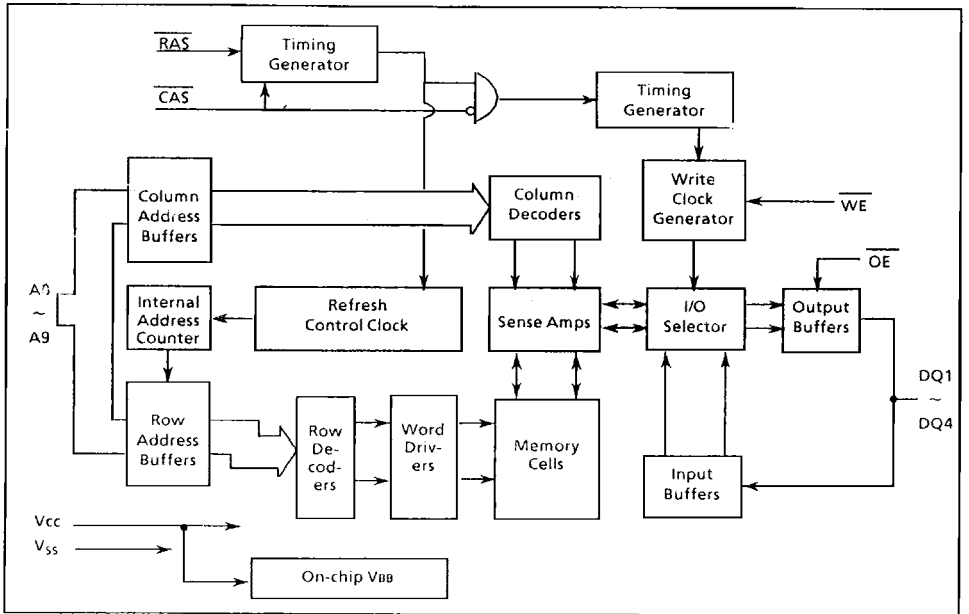
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Family	Access Time (Max)				Cycle Time (Min)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}	t_{OEA}		Operating (Max)	Standby (Max)
MSM514400-70	70 ns	35 ns	20 ns	20 ns	130 ns	550 mW	5.5 mW (MOS level)
MSM514400-80	80 ns	40 ns	20 ns	20 ns	160 ns	495 mW	
MSM514400-10	100 ns	50 ns	25 ns	25 ns	190 ns	440 mW	

PIN CONFIGURATION (TOP VIEW)



FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Conditions	Value	Unit	Notes
Voltage on any pin relative to V_{SS}	V_T	$T_a = 25\text{ }^\circ\text{C}$	- 1.0 to + 7.0	V	1
Short circuit output current	I_{OS}	$T_a = 25\text{ }^\circ\text{C}$	50	mA	1
Power dissipation	P_D	$T_a = 25\text{ }^\circ\text{C}$	1	W	1
Operating temperature	T_{opr}	-	0 to + 70	$^\circ\text{C}$	1
Storage temperature	T_{stg}	-	- 55 to + 150	$^\circ\text{C}$	1

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RECOMMENDED OPERATING CONDITIONS

($T_a = 0\text{ to }+70\text{ }^\circ\text{C}$)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{CC}	4.5	5.0	5.5	V	2
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.4	-	6.5	V	2
Input low voltage	V_{IL}	- 1.0	-	0.8	V	2

Notes: 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. All voltages are referenced to V_{SS} .

DC CHARACTERISTICS

(VCC = 5 V ± 10%, Ta = 0 to + 70°C)

Parameter	Symbol	Conditions	MSM 514400-70		MSM 514400-80		MSM 514400-10		Unit	Notes	
			Min	Max	Min	Max	Min	Max			
Output high voltage	V _{OH}	I _{OH} = - 5.0 mA	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	V		
Output low voltage	V _{OL}	I _{OL} = 4.2 mA	0	0.4	0	0.4	0	0.4	V		
Input leakage current	I _{LI}	0V ≤ V _I ≤ 6.5V; all other pins not under test = 0V	- 10	10	- 10	10	- 10	10	μA		
Output leakage current	I _{LO}	DQ _i = disable 0V ≤ V _O ≤ 5.5 V	- 10	10	- 10	10	- 10	10	μA		
Average power supply current (Operating)	I _{CC1}	RAS, CAS cycling, t _{RC} = min	-	100	-	90	-	80	mA	1, 2	
Power supply current (Standby)	I _{CC2}	RAS = V _{IH} CAS = V _{IH} DQ _i = Hz	TTL	-	2	-	2	-	2	mA	
		MOS	-	1	-	1	-	1	mA		
Average power supply current (RAS-only refresh)	I _{CC3}	RAS cycling, CAS = V _{IH} t _{RC} = min	-	100	-	90	-	80	mA	1, 2	
Power supply current (Standby)	I _{CC5}	RAS = V _{IH} CAS = V _{IL} DQ _i = enable	-	5	-	5	-	5	mA	1	
Average power supply current (CAS before RAS refresh)	I _{CC6}	RAS cycling, CAS before RAS	-	100	-	90	-	80	mA	1	
Average power supply current (Fast page mode)	I _{CC7}	RAS = V _{IL} , CAS cycling t _{PC} = min	-	90	-	80	-	70	mA	1, 3	

Notes: 1. I_{CC} depends on output loading and cycle rates. Specified values are obtained with the output open.

2. Measured by using no more than one address change while RAS = V_{IL}.

3. Measured by using no more than one address change while CAS = V_{IH}.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	Typ	Max	Unit
Input capacitance (A0 to A9)	C _{IN1}	-	-	6	pF
Input capacitance (RAS, CAS, WE, OE)	C _{IN2}	-	-	7	pF
Output capacitance (DQ1 to DQ4)	C _{I/O}	-	-	7	pF

AC CHARACTERISTICS

(VCC = 5 V ± 10%, Ta = 0 to +70°C)

Notes 1, 2, 3, 10

Parameter	Symbol	MSM 514400-70		MSM 514400-80		MSM 514400-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	130	–	160	–	190	–	ns	
Read/write cycle time	t _{RWC}	185	–	215	–	255	–	ns	
Fast page mode cycle time	t _{PC}	45	–	50	–	60	–	ns	
Fast page mode read/write cycle time	t _{PRWC}	105	–	110	–	130	–	ns	
Access time from $\overline{\text{RAS}}$	t _{RAC}	–	70	–	80	–	100	ns	4, 5
Access time from $\overline{\text{CAS}}$	t _{CAC}	–	20	–	20	–	25	ns	4, 5
Access time from column address	t _{AA}	–	35	–	40	–	50	ns	4, 6
Access time from $\overline{\text{OE}}$	t _{OEA}	–	20	–	20	–	25	ns	
Access time from $\overline{\text{CAS}}$ precharge	t _{CPA}	–	40	–	45	–	55	ns	4
Output low impedance time from $\overline{\text{CAS}}$	t _{CLZ}	0	–	0	–	0	–	ns	
Output buffer turn-off delay time	t _{OFF}	0	20	0	20	0	25	ns	7
$\overline{\text{OE}}$ to data output buffer turn-off delay time	t _{OEZ}	0	20	0	20	0	25	ns	7
Transition time	t _T	3	50	3	50	3	50	ns	3
Refresh period	t _{REF}	–	16	–	16	–	16	ms	
$\overline{\text{RAS}}$ precharge time	t _{RP}	50	–	70	–	80	–	ns	
$\overline{\text{RAS}}$ pulse width	t _{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{\text{RAS}}$ pulse width (Fast page mode)	t _{RASP}	70	100,000	80	100,000	100	100,000	ns	
$\overline{\text{RAS}}$ hold time	t _{RSH}	20	–	20	–	25	–	ns	
$\overline{\text{RAS}}$ hold time reference to $\overline{\text{OE}}$	t _{ROH}	20	–	20	–	25	–	ns	
$\overline{\text{CAS}}$ precharge time	t _{CP}	10	–	10	–	10	–	ns	
$\overline{\text{CAS}}$ pulse width	t _{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{\text{CAS}}$ hold time	t _{CSH}	70	–	–	–	100	–	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t _{CRP}	10	–	10	–	10	–	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t _{RCD}	20	50	22	60	25	75	ns	5
$\overline{\text{RAS}}$ to column address delay time	t _{RAD}	15	35	17	40	20	50	ns	6
Row address set-up time	t _{ASR}	0	–	0	–	0	–	ns	
Row address hold time	t _{RAH}	10	–	12	–	15	–	ns	
Column address set-up time	t _{ASC}	0	–	0	–	0	–	ns	
Column address hold time	t _{CAH}	15	–	15	–	20	–	ns	
Column address hold time from $\overline{\text{RAS}}$	t _{AR}	55	–	60	–	75	–	ns	
Column address to $\overline{\text{RAS}}$ lead time	t _{RAL}	35	–	40	–	50	–	ns	

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AC CHARACTERISTICS (CONT.)

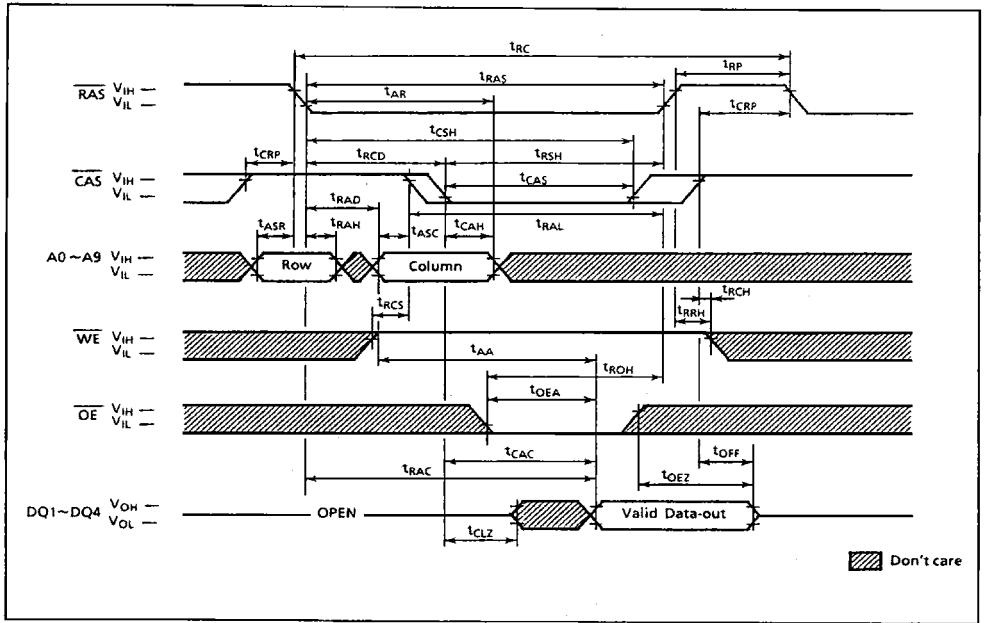
Parameter	Sym- bol	MSM 514400-70		MSM 514400-80		MSM 514400-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read command set-up time	t _{RCS}	0	—	0	—	0	—	ns	
Read command hold time	t _{RCH}	0	—	0	—	0	—	ns	8
Read command hold time reference to RAS	t _{RRH}	10	—	10	—	10	—	ns	8
Write command set-up time	t _{WCS}	0	—	0	—	0	—	ns	9
Write command hold time	t _{WCH}	15	—	15	—	20	—	ns	
Write command pulse width	t _{WP}	15	—	15	—	20	—	ns	
Write command hold time from RAS	t _{WCR}	55	—	60	—	75	—	ns	
OE command hold time	t _{OEH}	20	—	20	—	25	—	ns	
Write command to CAS lead time	t _{CWL}	20	—	20	—	25	—	ns	
Write command to RAS lead time	t _{RWL}	20	—	20	—	25	—	ns	
Data-in set-up time	t _{DS}	0	—	0	—	0	—	ns	
Data-in hold time	t _{DH}	15	—	15	—	20	—	ns	
Data-in hold time from RAS	t _{DHR}	55	—	60	—	75	—	ns	
OE to Data-in delay time	t _{OEED}	20	—	20	—	25	—	ns	
CAS to WE delay time	t _{CWD}	50	—	50	—	60	—	ns	9
Column address to WE delay time	t _{AWD}	65	—	70	—	85	—	ns	
RAS to WE delay time	t _{RWD}	100	—	110	—	135	—	ns	9
CAS active delay time from RAS precharge	t _{RPC}	10	—	10	—	10	—	ns	
RAS to CAS set-up time (CAS before RAS)	t _{CSR}	10	—	10	—	10	—	ns	
RAS to CAS hold time (CAS before RAS)	t _{CHR}	20	—	20	—	20	—	ns	
CAS precharge time (Refresh counter test)	t _{CPT}	30	—	40	—	50	—	ns	
WE to RAS precharge time (CAS before RAS)	t _{WRP}	10	—	10	—	10	—	ns	
WE hold time from RAS (CAS before RAS)	t _{WRH}	20	—	20	—	20	—	ns	
RAS to WE set-up time (Test mode)	t _{WSR}	10	—	10	—	10	—	ns	
RAS to WE hold time (Test mode)	t _{WHR}	20	—	20	—	20	—	ns	

- Notes: 1. An initial pause of 200 us is required after power-up followed by a minimum of eight initialization cycles (examples: $\overline{\text{RAS}}$ -only Refresh or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh) before proper device operation is achieved.
2. The AC measurements assume the transition time (t_T) = 5 ns.
 3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring the timing of the input signals. Transition times are measured between V_{IH} and V_{IL} .
 4. Measured by using an equivalent load circuit of 2 TTL loads and 100pF.
 5. Operating within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. The spec. t_{RCD} (max.) is for reference only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, access time is controlled exclusively by t_{CAC} .
 6. Operating within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. The spec. t_{RAD} (max.) is for reference only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, access time is controlled exclusively by t_{AA} .
 7. The t_{OFF} (max.) and t_{OEZ} (max.) spec. defines at which time the output data achieves a high impedance state and is not referenced to output voltage levels.
 8. Either the t_{RRH} or the t_{RCH} spec. must be satisfied for a proper read cycle.
 9. The specs t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet for reference only. If $t_{WCS} \geq t_{WCS}$ (min.) the cycle is an Early Write cycle and the data out remains in a high impedance state throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min.), $t_{RWD} \geq t_{RWD}$ (min.) and $t_{AWD} \geq t_{AWD}$ (min.), the cycle is a Read-Write cycle and data out contains data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of data out is indeterminate at access time.
 10. Test Mode Feature:

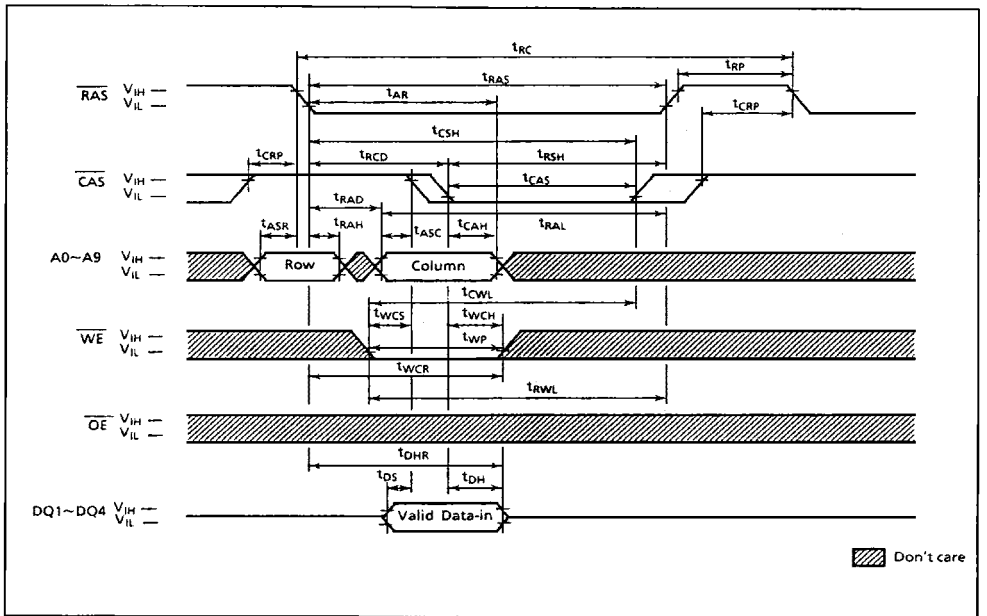
The test mode is activated by executing a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle with $\overline{\text{WE}}$ held at a low level (V_{IL}). The device remains in the test mode until it is deactivated by executing a standard $\overline{\text{RAS}}$ -only refresh or a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh with $\overline{\text{WE}}$ held at a high level (V_{IH}).

In the test mode CA0 is not used and each I/O pin now accesses 2 bit locations. Since all 4 I/O pins are used, a total of 8 data bits can be written in parallel into the memory array, reducing test time by 50%. When executing a read cycle 2 data bits are gated throughout the internal exclusive OR logic and the result is presented at the I/O pin, thus if the two data bits are equal, the I/O pin indicates a logical 1. If the two data bits are not equal, the I/O pin indicates a logical 0. This additional internal operation delays access time by 5ns and should be added to the access time parameters if operating in the test mode.

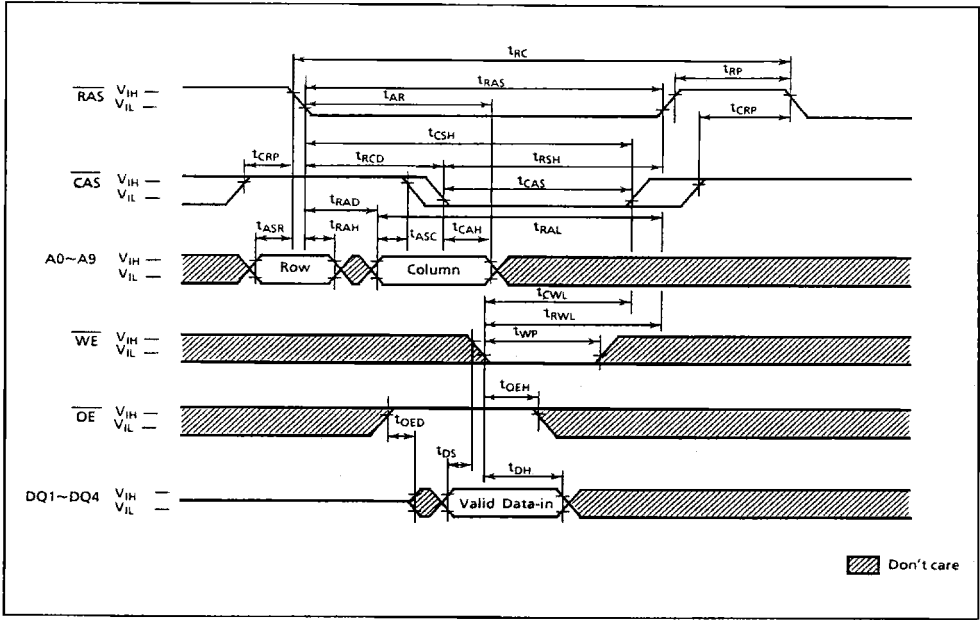
READ CYCLE



WRITE CYCLE (EARLY WRITE)

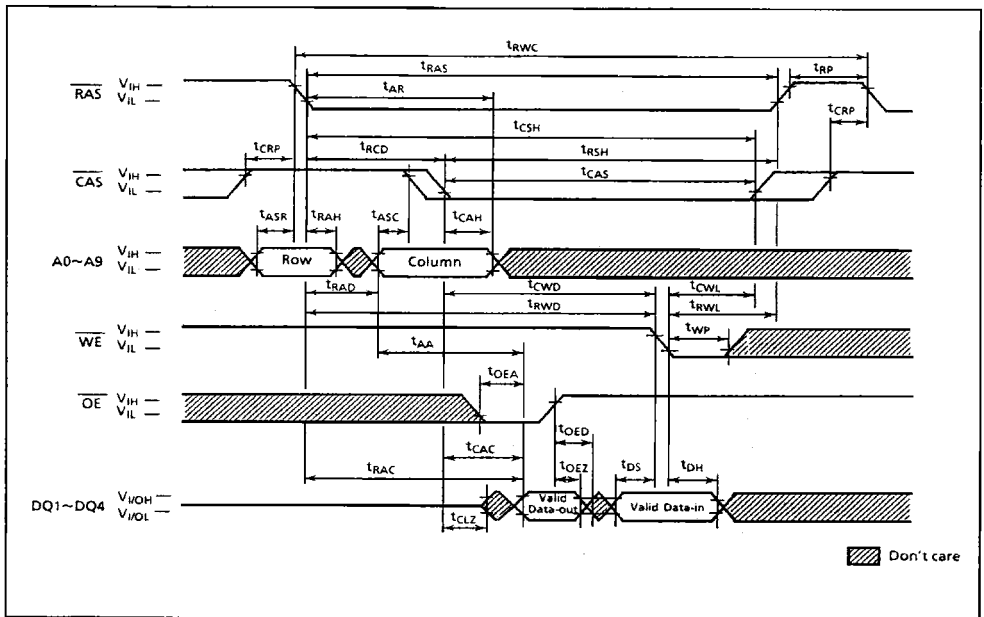


WRITE CYCLE (OE CONTROL WRITE)

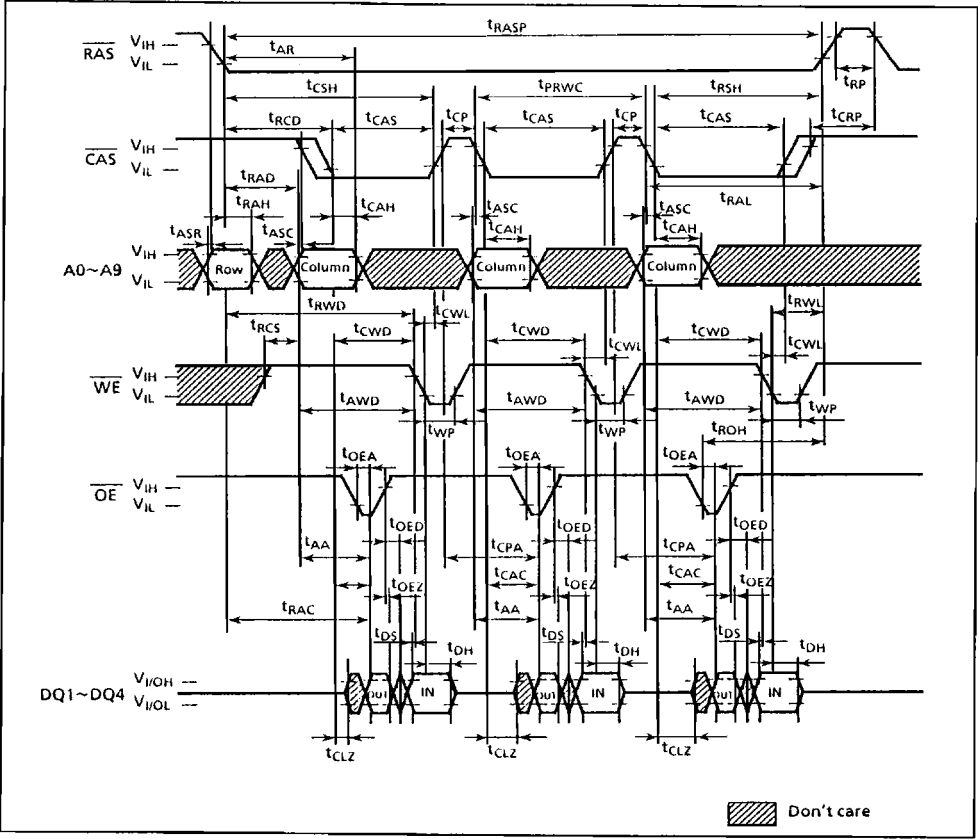


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READ/WRITE CYCLE

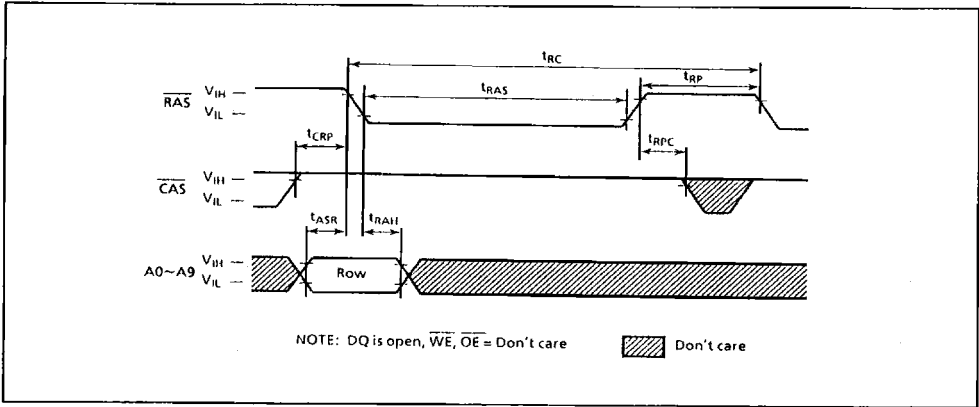


FAST PAGE MODE READ/WRITE CYCLE

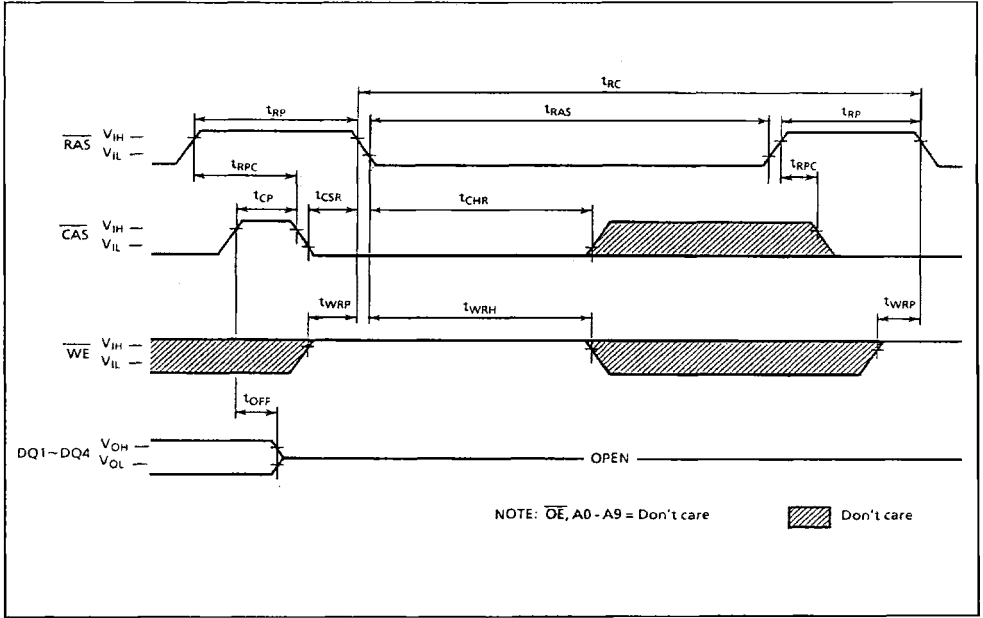


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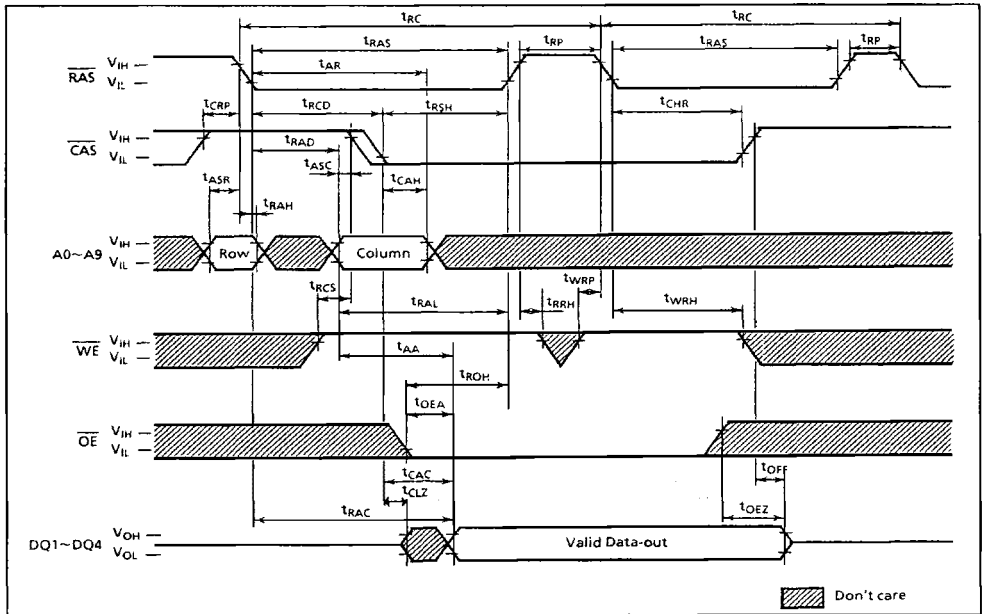
RAS-ONLY REFRESH CYCLE



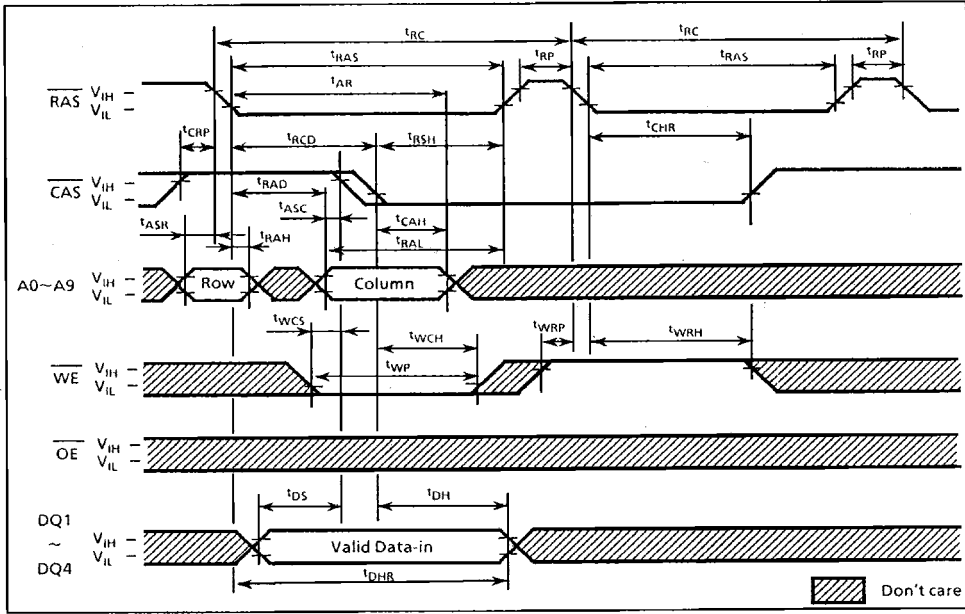
CAS BEFORE RAS AUTO-REFRESH CYCLE



HIDDEN REFRESH READ CYCLE



HIDDEN REFRESH WRITE CYCLE



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TEST MODE INITIATE CYCLE

