FEDL9445-02
Issue Date: Dec. 20, 2013

ML9445

180-Channel LCD Driver with Built-in RAM for LCD Dot Matrix Displays

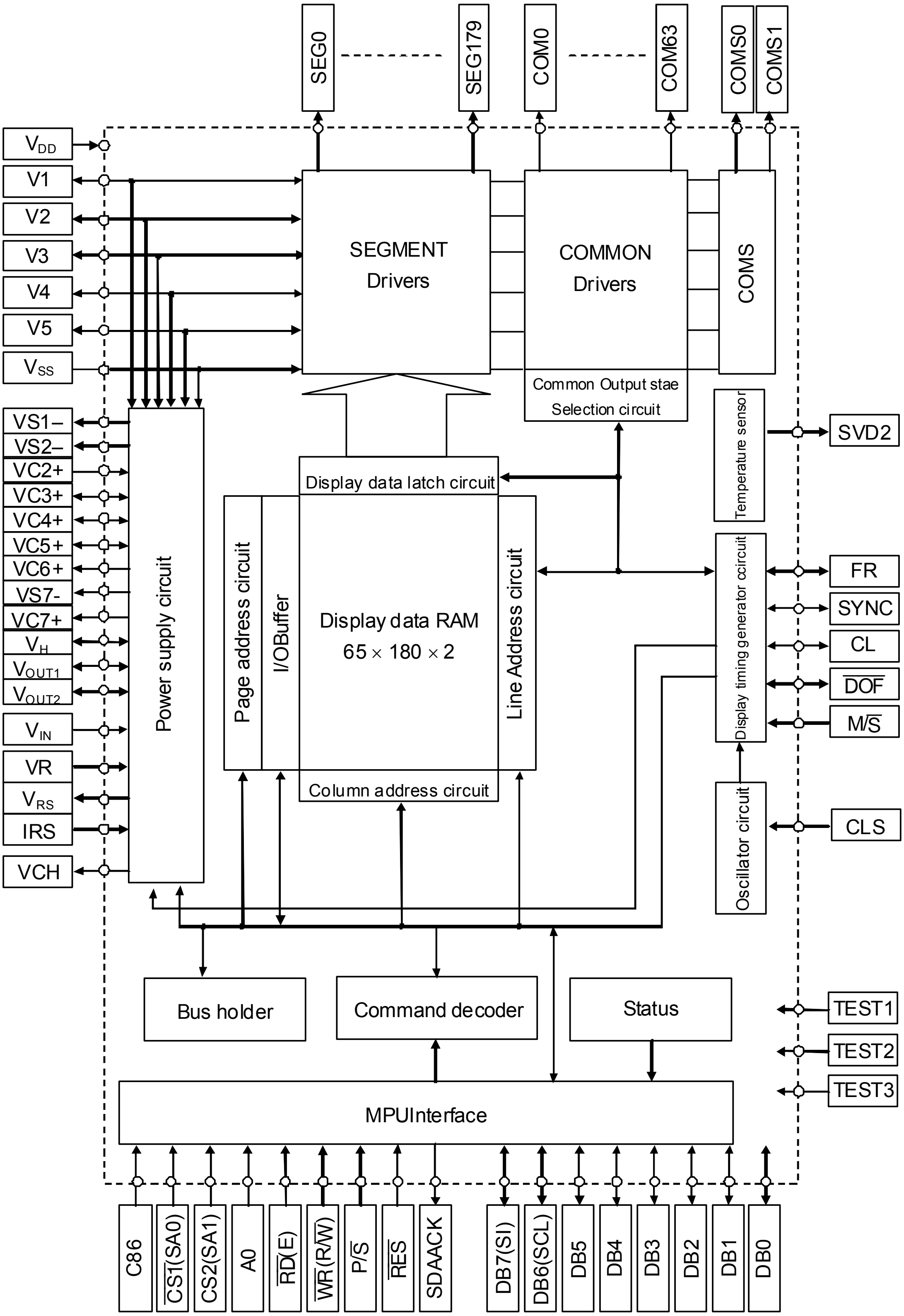
GENERAL DESCRIPTION

The ML9445 is an LSI for dot matrix graphic LCD devices carrying out bit map display. This LSI can drive a dot matrix graphic LCD display panel under the control of an 8-bit microcomputer (hereinafter described MPU). Since all the functions necessary for driving a bit map type LCD device are incorporated in a single chip, using the ML9445 makes it possible to realize a bit map type dot matrix graphic LCD display system with only a few chips. Since the bit map method in which one bit of display RAM data turns ON or OFF one dot in the display panel, it is possible to carry out displays with a high degree of freedom such as Chinese character displays, etc. With one chip, it is possible to construct a graphic display system with a maximum of 65 × 180 dots.
The ML9445 has 65 common signal outputs and 180 segment signal outputs and one chip can drive a display of up to 65 × 180 dots.

FEATURES

- Direct display of the RAM data using the bit map method
  Display RAM data “1” ... Dot is displayed
  Display RAM data “0” ... Dot is not displayed (during forward display)
- Display RAM capacity
  65 × 180 × 2 = 23,400 bits
- LCD Drive circuits
  65 common outputs, 180 segment outputs
- MPU interface: Can select an 8-bit parallel or serial interface or I^2C (Write Only)
- Built-in voltage multiplier circuit for the LCD drive power supply
- Built-in LCD drive voltage adjustment circuit
- Built-in LCD drive bias generator circuit
- Can select frame reversal drive or line reversal drive by command
- Built-in oscillator circuit (Internal RC oscillator/external clock input)
- A variety of commands
  Read/write of display data, display ON/OFF, forward/reverse display, all dots ON/all dots OFF, set page address, set display start address, etc.
- Power supply voltage
  Logic power supply: V_{DD}-V_{SS} = 2.7 V to 5.5 V
  Voltage multiplier reference voltage: V_{IN}-V_{SS} = 2.7 V to 5.5 V
  (2- to 5-time multiplier available)
  LCD Drive voltage: V_{BI}-V_{SS} = 6.0 to 18.5 V
- Package: ML9445DVWA Gold bump chip (Bump hardness: Low, DV)
- This device is not resistant to radiation and light.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{SS} = 0 V

Parameter	Symbol	Condition	Rated value	Unit	Applicable pins
Power supply voltage	V_{DD}	Ta= 25°C	–0.3 to +6.5	V	V_{DD}
Bias voltage	V_{BI}	Ta = 25°C	–0.3 to +20	V	V1 to V5
Voltage multiplier output voltage	V_{OUT}	Ta= 25°C	–0.3 to +20	V	V_{OUT1} ,V_{OUT2}
Voltage multiplier reference voltage	V_{IN}	2-time multiplication 3-time multiplication 4-time multiplication 5-time multiplication	–0.3 to +5.5 –0.3 to +5.5 –0.3 to +5.0 –0.3 to +4.0	V	V_{IN}
Input voltage	V_I	Ta = 25°C	–0.3 to V_{DD}+0.3	V	All inputs
Output short-circuit current	I_S	Ta = 25°C	−2.0 to +2.0	mA	All outputs
Chip temperature	T_C	—	125	°C	—
Storage temperature range	T_{STG}	—	–55 to +150	°C	—

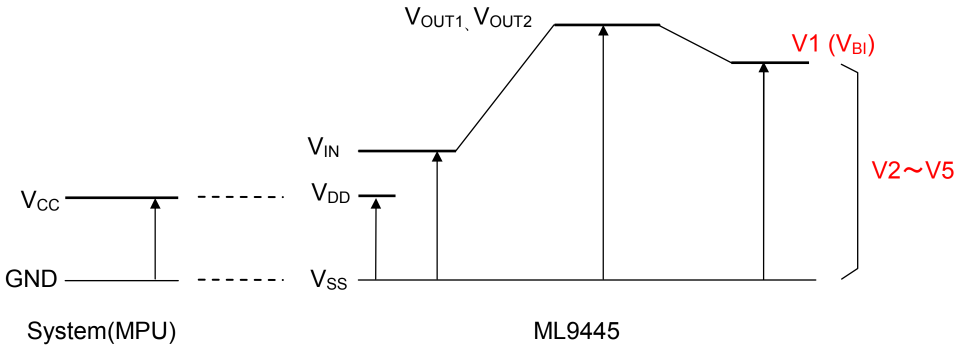
Note: Do not use the ML9445 by short-circuiting one output pin to another output pin as well as to other pin (input pin, input/output pin, or power supply pin).

RECOMMENDED OPERATING CONDITIONS

V_{SS} = 0 V

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	Applicable pins
Power supply voltage	V_{DD}	—	2.7	—	5.5	V	V_{DD}
Bias voltage	V_{BI}	—	6.0	18	18.5	V	V1 to V5
Voltage multiplier reference voltage	V_{IN}	2-time multiplication 3-time multiplication 4-time multiplication 5-time multiplication	3.0 2.7 2.7 2.7	—	5.5 5.5 4.625 3.7	V	V_{IN}
Voltage multiplier output voltage	V_{OUT}	External input	6.0	18	18.5	V	V_{OUT1} ,V_{OUT2}
Operating temperature range	T_a	—	–40	—	105	°C	—

Note 1: The electrical characteristics are influenced by COG trace resistance. This LSI always has to be evaluated before using.



Note 2: The voltages V_{DD}, V_{IN}, V1 to V5, V_{OUT1} and V_{OUT2} are values taking V_{SS} = 0 V as the reference.
Note 3: The highest bias potential is V1 and the lowest is V_{SS}.
Note 4: Always maintain the relationship V1 ≥ V2 ≥ V3 ≥ V4 ≥ V5 ≥ V_{SS} among these voltages.
Note 5: When using an external power supply, follow the procedure for power application.
When applying external power to the V_{OUT1} pin only, apply V_{OUT1} after $V_{DD.}$
When applying external power to the V_{OUT2} pin only, apply V_{OUT2} after $V_{DD.}$
When applying external power to the V1 pin only, apply V1 after V_{DD}.
When applying external power to the V1 pin to V5 pin, apply V1 to V5 after V_{DD}.
Note that the above (Note 4) must be satisfied including transient state at power application.
Note 6: When using an external power supply, follow the procedure for power removal described below.
When external power is in use for the V_{OUT1} pin only, remove V_{OUT1} after V_{DD}.
When external power is in use for the V_{OUT2} pin only, remove V_{OUT2} after V_{DD}.
When external power is in use for the V1 pin only, remove V1 after V_{DD}.
When external power is in use for the V1 pin to V5 pin, remove V1 to V5 after V_{DD}.
Note that the above (Note 4) must be satisfied including transient state at power removal.

ELECTRICAL CHARACTERISTICS

DC Characteristics

[V_{SS} =0V, V_{DD}=2.7 to 5.5V, Ta =–40 to +105°C]

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Applicable pins
"H" Input voltage	V_{IH}		0.8 × V_{DD}	—	V_{DD}	V	*1
"L" Input voltage	V_{IL}		0	—	0.2 × V_{DD}		
"H" Output voltage	V_{OH}	I_{OH} = –0.5 mA	0.8 × V_{DD}	—	—	V	*2
"L" Output voltage1	V_{OL1}	I_{OL} = 0.5 mA	—	—	0.2 × V_{DD}		
"L" Output voltage2	V_{OL2}	I_{OL} = 0.5 mA	—	—	0.2 × V_{DD}	V	SDAACK
Input current 1	I_{IL1}	V_I = V_{DD} or V_I = 0 V	–1.0	—	+1.0	μA	*3
Input current 2	I_{IL2}		–3.0	—	+3.0		*4
Input capacitance	C_I	Ta=25°C, F=10kHz	—	8	12	pF	*1
V1 output voltage temperature gradient	V1TC	Ta = 25°C V1 = 12 V *5	—	-0.06	—	%/°C	V1
Reference voltage	V_{REG}	Ta = 25°C	2.925	3.00	3.075	V	V_{RS}
V1 output voltage	V1	*6	10.59	10.86	11.13	V	V1
Voltage multiplier output voltage	V_{OUT}	2-time multiplication *7	9	—	—	V	V_{OUT1}
		3-time multiplication *8	13.5	—	—		
		4-time multiplication *9	13.5	—	—		
		5-time multiplication *10	13.5	—	—		
V_{OUT} - V1 voltage	Vot1	*11	0.6	—	—	V	V_{OUT2}, V1
LCD driver ON resistance	R_{ON}	I_O = ±50 μA, V1=10V, 1/9bias	—	1.0	1.5	kΩ	SEG0 to 179, COMS0, COMS1, COM0 to 63
		I_O = ±50 μA, V1=6V, 1/4bias	—	2.0	3.0		
Oscillator frequency: Internal oscillation	f_{OSC}	Ta = 25°C	799	832	865	kHz	*12
			666	—	998	kHz	
Oscillator frequency: External input	f_{EXT}		—	100	250	kHz	CL*12

*1: A0, DB0 to DB5, DB6 (SCL), DB7 (SI), $\overline{\text{RD}}$ (E), $\overline{\text{WR}}$ (R/$\overline{\text{W}}$), $\overline{\text{CS1}}$, CS2, CLS, CL, M/$\overline{\text{S}}$, C86, P/$\overline{\text{S}}$, $\overline{\text{RES}}$, IRS, FR, $\overline{\text{DOF}}$, SYNC Pins
*2: DB0 to DB7, FR, $\overline{\text{DOF}}$, SYNC, CL Pins
*3: A0, $\overline{\text{RD}}$ (E), $\overline{\text{WR}}$ (R/$\overline{\text{W}}$), $\overline{\text{CS1}}$, CS2, CLS, M/$\overline{\text{S}}$, C86, P/$\overline{\text{S}}$, $\overline{\text{RES}}$, IRS Pins
*4: Applicable to the pins DB0 to DB5, DB6 (SCL), DB7 (SI), CL, FR, $\overline{\text{DOF}}$, SYNC in the high impedance state.
*5: Temperature gradient select : (DB2, DB1, DB0)=(0, 1, 0)
*6: Ta = 25°C, D7=0,α =57, (1+Rb/Ra) = 4, Voltage multiplier output voltage (V_{OUT}) = 13.5 V (External input), LCD drive output = no-load, See Power Supply Circuit. (Page 39)

*7: V_{IN} = 5.0 V, voltage multiplier capacitor C1 = 2.6 to 4.0 μF, voltage multiplier output load current I = 500 μA. Only a voltage multiplier circuit operates, not activating the voltage adjustment circuit and V/F circuit, by power control set command.

*8: V_{IN} = 5.00 V, voltage multiplier capacitor C1 = 2.6 to 4.0 μF, voltage multiplier output load current I = 500 μA. Only a voltage multiplier circuit operates, not activating the voltage adjustment circuit and V/F circuit, by power control set command.

*9: V_{IN} = 3.75 V, voltage multiplier capacitor C1 = 2.6 to 4.0 μF, voltage multiplier output load current I = 500 μA. Only a voltage multiplier circuit operates, not activating the voltage adjustment circuit and V/F circuit, by power control set command.

*10: V_{IN} = 3.0 V, voltage multiplier capacitor C1 = 2.6 to 4.0 μF, voltage multiplier output load current I = 500 μA. Only a voltage multiplier circuit operates, not activating the voltage adjustment circuit and V/F circuit, by power control set command.

*11: V1 load current I = 400 μA. 8 V is externally input to V_{OUT2}.
The voltage adjustment circuit and V/F circuit operate by power control set command.
LCD output = no load

*12: See Table 1 for the relationship between the oscillator frequency and the frame frequency.

Table 1. Relationship among the oscillator frequency (f_{OSC}), external input frequency(f_{EXT}) display clock frequency (f_{LCDCK}), and LCD frame frequency (f_{FR})

Ratio of dividing frequency: 1/n , Number of Display Line : L

	Parameter		Display clock frequency (f_{LCDCK})	LCD frame frequency (f_{FR})
ML9445	When the internal oscillator is used	1/65 to 1/50 duty	Fosc/16/n	F_{OSC} /(16*n*L)
		1/49 to 1/34 duty	F_{OSC}* (2/3)/16/n	F_{OSC} *(3/4) /(16*n*L)
		1/33 to 1/18 duty	F_{OSC} *(1/2)/16/n	F_{OSC} *(1/2) /(16*n*L)
		1/17 or less	F_{OSC} * (1/4)/16/n	F_{OSC} *(1/4) /(16*n*L)
	When the internal oscillator is not used		f_{EXT}/16	f_{EXT}/(16*L)

• Operating current consumption value

(1) During display operation, internal power supply OFF (The current flowing through V_{DD} with V1 to V5 externally applied when an external power supply is used, not including the current for the LCD drive)

[V_{SS}=0 V, Ta = 25°C]

Display mode	Symbol	Condition	Rated value			Unit
			Min	Typ	Max	
All-white	I_{DD}	V_{DD} = 5 V, V1- V_{SS} = 11 V, no load	—	175	300	µA
		V_{DD} = 2.7 V, V1- V_{SS} = 8 V, no load	—	155	250	
Checker pattern	I_{DD}	V_{DD} = 5 V, V1- V_{SS} = 11 V, no load	—	175	300	µA
		V_{DD} = 2.7 V, V1- V_{SS} = 8 V, no load	—	155	250	

(2) During display operation, internal power supply ON (Total of currents flowing through V_{DD} and V_{IN})

[V_{SS}=0V, Ta=25°C]

Display mode	Symbol	Condition	Rated value			Unit
			Min	Typ	Max	
All-white	I_{DDIN}	Frame reversal, V_{DD}, V_{IN} = 5 V, 3-time voltage multiplication V1 - V_{SS}= 11 V, no load	—	450	700	µA
		Frame reversal, V_{DD}, V_{IN} = 2.7 V, 4-time voltage multiplication V1 - V_{SS}= 8 V, no load	—	300	600	
		16-line reversal, V_{DD}, V_{IN} = 5 V, 3-time voltage multiplication V1 - V_{SS}= 11 V, no load	—	600	800	
Checker pattern	I_{DDIN}	Frame reversal, V_{DD}, V_{IN} = 5 V, 3-time voltage multiplication V1 - V_{SS}= 11 V, no load	—	1450	1700	µA
		Frame reversal, V_{DD}, V_{IN} = 2.7 V, 4-time voltage multiplication V1 - V_{SS}= 8 V, no load	—	1700	2000	
		16-line reversal, V_{DD}, V_{IN} = 5 V, 3-time voltage multiplication V1 - V_{SS}= 11 V, no load	—	1500	1700	

• Power save mode current consumption

[V_{SS}=0V, Ta=25°C]

Parameter	Symbol	Condition	Rated value			Unit
			Min	Typ	Max	
Sleep mode	I_{DDS1}	V_{DD} = 3.7 V	—	4	20	µA

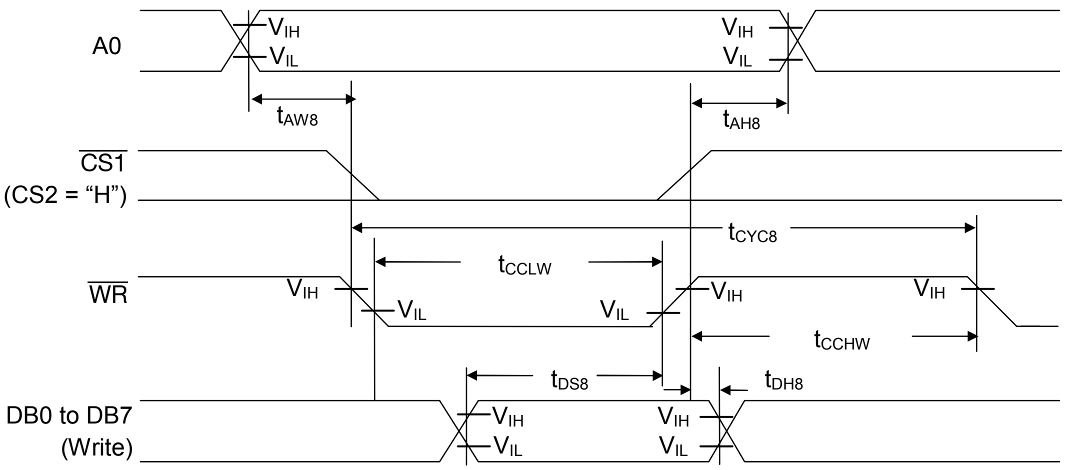
Temperature Sensor Characteristics

[V_{SS}=0 V, V_{DD}=2.7 to5.5 V, Ta=–40 to+105°C]

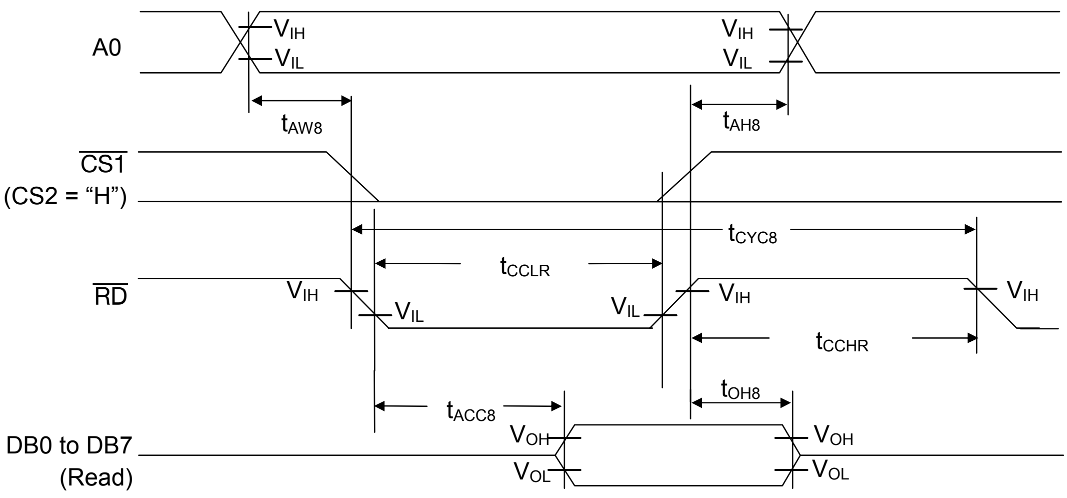
Parameter	Symbol	Condition	Rated value			Unit
			Min	Typ	Max	
Output voltage	V_{SVD2}	-40℃ 25℃ 105℃	1.482 1.177 0.801	1.506 1.2 0.824	1.529 1.224 0.848	V
Output voltage temperature gradient	V_{GRA}	—	—	-4.7	—	mV/℃
Output voltage setup time	t_{SEN}	—	100	—	—	ms
Operating current	I_{SEN}	25℃	—	10	30	μA

Switching Characteristics

• System bus Write characteristics 1 (80-series MPU)



• System bus Read characteristics 1 (80-series MPU)



[V_{DD}=2.7 to 5.5V, Ta=–40 to+105°C]

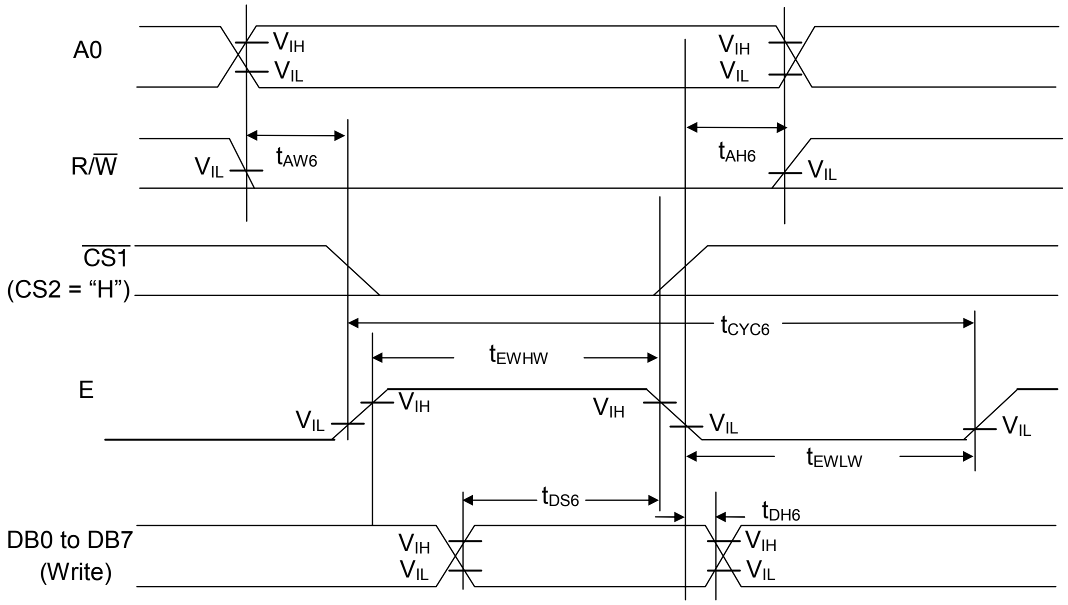
Parameter	Symbol	Condition	Rated value		Unit
			Min	Max	
Address hold time	t_{AH8}		5	—	ns
Address setup time	t_{AW8}		5	—	
System cycle time	t_{CYC8}		300	—	
Control L pulse width ($\overline{WR}$)	t_{CCLW}		60	—	
Control L pulse width ($\overline{RD}$)	t_{CCLR}		240	—	
Control H pulse width ($\overline{WR}$)	t_{CCHW}		60	—	
Control H pulse width ($\overline{RD}$)	t_{CCHR}		60	—	
Data setup time	t_{DS8}		40	—	
Data hold time	t_{DH8}		15	—	
$\overline{RD}$ Access time	t_{ACC8}	CL = 100 pF	—	240	
Output disable time	t_{OH8}		10	100	

Note 1: The input signal rise and fall times are specified as 15ns or less.
When using the system cycle time for fast speed, the specified values are
$(tr + tf) \leq (t_{CYC8} - t_{CCLW} - t_{CCHW})$ or $(tr + tf) \leq (t_{CYC8} - t_{CCLR} - t_{CCHR})$.

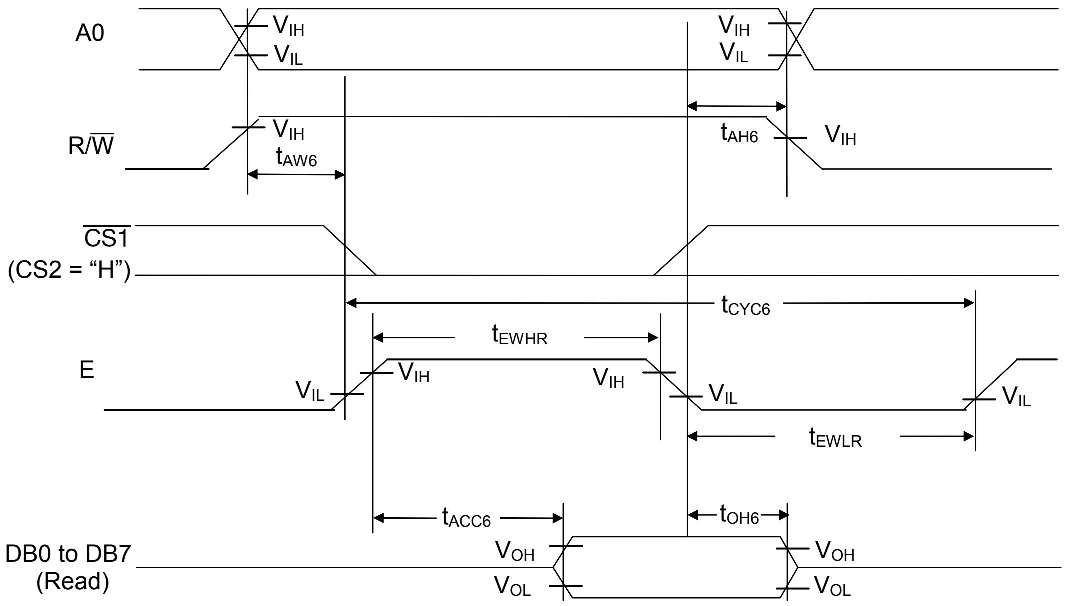
Note 2: All timings are specified taking the levels of 20% and 80% of V_{DD} as the reference.

Note 3: The values of t_{CCLW} and t_{CCLR} are specified during the overlapping period of $\overline{CS1}$ at "L" (CS2 = "H") and the "L" levels of $\overline{WR}$ and $\overline{RD}$, respectively.

• System bus Write characteristics 2 (68-series MPU)



• System bus Read characteristics 2 (68-series MPU)



[V_{DD}=2.7to5.5V, Ta=–40 to+105°C]

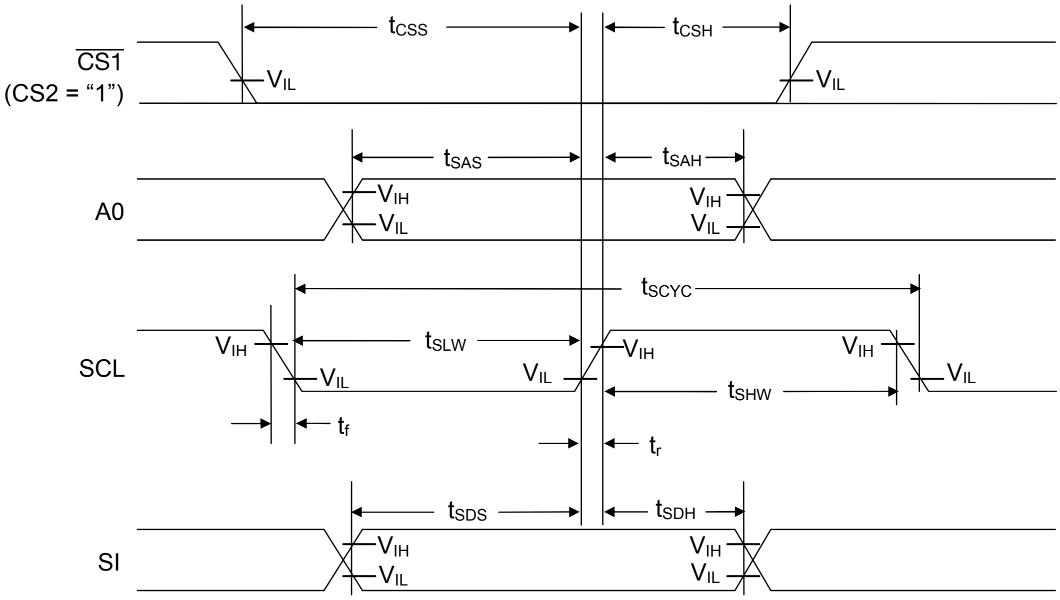
Parameter		Symbol	Condition	Rated value		Unit
				Min	Max	
Address hold time		t_{AH6}		5	—	ns
Address setup time		t_{AW6}		5	—	
System cycle time		t_{CYC6}		300	—	
Data setup time		t_{DS6}		40	—	
Data hold time		t_{DH6}		15	—	
Access time		t_{ACC6}	CL = 100 pF	—	240	
Output disable time		t_{OH6}		10	100	
Enable H pulse width	Read	t_{EWHR}		240	—	
	Write	t_{EWHW}		60	—	
Enable L pulse width	Read	t_{EWLR}		60	—	
	Write	t_{EWLW}		60	—	

Note 1: The input signal rise and fall times are specified as 15ns or less.
When using the system cycle time for fast speed, the specified values are
$(tr + tf) \le (t_{CYC6} - t_{EWLW} - t_{EWHW})$ or $(tr + tf) \le (t_{CYC6} - t_{EWLR} - t_{EWHR})$.

Note 2: All timings are specified taking the levels of 20% and 80% of V_{DD} as the reference.

Note 3: The values of t_{EWLW} and t_{EWLR} are specified during the overlapping period of $\overline{CS1}$ at "L" (CS2 = "H") and the "H" level of E.

• Serial interface

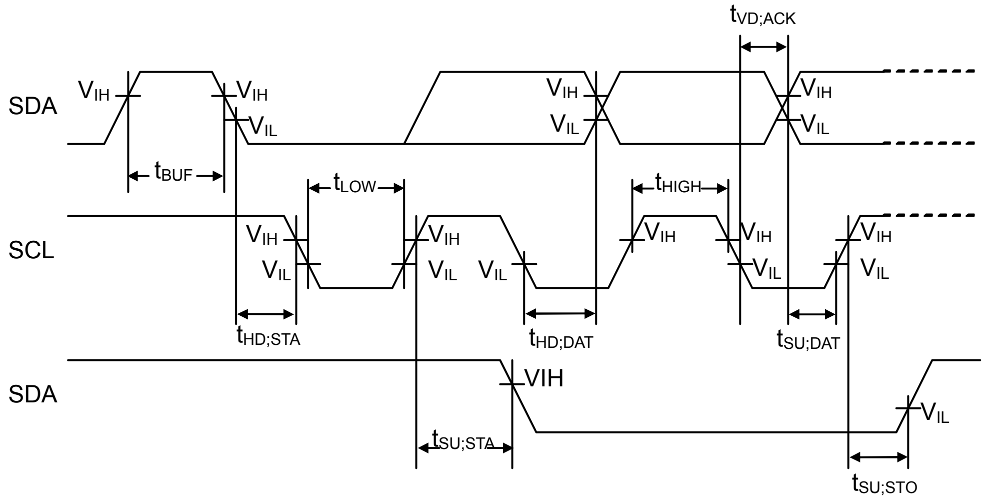


[V_{DD}=2.7to4.5 V, Ta=–40 to+105°C]

Parameter	Symbol	Condition	Rated value		Unit
			Min	Max	
Serial clock period	t_{SCYC}		250	—	ns
SCL "H" Pulse width	t_{SHW}		100	—	
SCL "L" Pulse width	t_{SLW}		100	—	
Address setup time	t_{SAS}		150	—	
Address hold time	t_{SAH}		150	—	
Data setup time	t_{SDS}		100	—	
Data hold time	t_{SDH}		100	—	
CS setup time	t_{CSS}		150	—	
CS hold time	t_{CSH}		150	—	

Note 1: The input signal rise and fall times are specified as 15ns or less.
Note 2: All timings are specified taking the levels of 20% and 80% of V_{DD} as the reference.

• I^2C interface timing

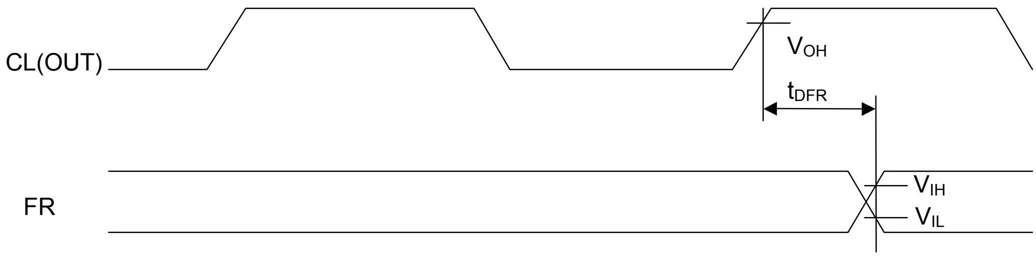


(V_{DD} = 2.7 to 5.5 V, Ta = -40 to +105°C)

Item	Symbol	Condition	Min.	Max.	Unit
SCL clock frequency	f_{SCL}	—	—	3.4	MHz
Hold time (repeat) "STATRT" condition	$t_{HD,STA}$	—	160	—	ns
SCL "L" pulse width	t_{LOW}	—	160	—	
SCL "H" pulse width	t_{HIGH}	—	60	—	
Setup time for repeat "START" condition	$t_{SU,STA}$	—	160	—	
Data hold time	$t_{HD,DAT}$	—	0	70	
Data setup time	$t_{SU,DAT}$	—	10	—	
Setup time for "STOP" condition	$t_{SU,STO}$	—	160	—	
Bus free time between "STOP" condition and "START" condition	t_{BUF}	—	160	—	
Data valid acknowledge time	$t_{VD,ACK}$	—	—	240	
Data bus load capacitance	Cb	—	—	100	pF
Noise pulse width tolerance	t_{wf}	—	—	10	ns

Note 1: The input signal rise and fall times are specified as 0.1μs or less.
Note 2: All timings are specified taking the levels of 20% and 80% of V_{DD} as the reference.

• Display control output timing

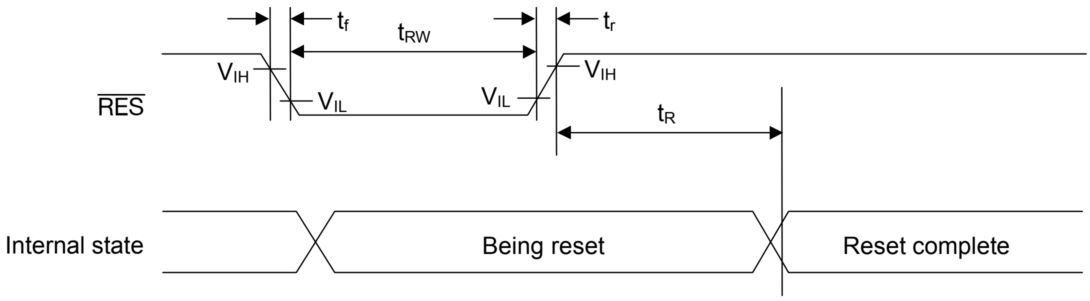


[V_{DD}=2.7to5.5V, Ta=–40to+105°C]

Parameter	Symbol	Condition	Rated value			Unit
			Min	Typ	Max	
FR Delay time	t_{DFR}	CL = 50 pF	—	20	80	ns

Note 1: All timings are specified taking the levels of 20% and 80% of V_{DD} as the reference.
Note 2: Valid only when the device operates in master mode.

• Reset input timing



[V_{DD} = 2.7 to 5.5 V, Ta = –40 to +105°C]

Parameter	Symbol	Condition	Rated value			Unit
			Min	Typ	Max	
Reset time	t_R	—	—	—	1	μs
Reset "L" pulse width	t_{RW1}		1	—	—	
Noise pulse width tolerance	t_{RW2}		—	—	50	ns

Note 1: The input signal rise and fall times (t_r, t_f) are specified as 15 ns or less.
Note 2: All timings are specified taking the levels of 20% and 80% of V_{DD} as the reference.

PIN DESCRIPTION

Function	Pin name	Number of pins	I/O	Description
MPU Interface	DB0 to DB7	2*8	I/O	These are 8-bit bi-directional data bus pins that can be connected to 8-bit standard MPU data bus pins. When a serial interface is selected (P/$\overline{\text{S}}$ = “L”,C86= “H”): DB7: Serial data input pin (SI) DB6: Serial clock input pin (SCL) When the serial interface and the I2C interface are selected, DB0 to DB5 pins will be in the high impedance state. Fix the DB0 to DB5 pins at “H” or “L” level. DB0 to DB7 will be in the high impedance state when the chip select is in the inactive state.
	A0	2	I	Normally, the lowest bit of the MPU address bus is connected and used for distinguishing between data and commands. A0 = “H”: Indicates that DB0 to DB7 is display data. A1 = “L”: Indicates that DB0 to DB7 is control data.
	$\overline{\text{RES}}$	2	I	Initial setting is made by making $\overline{\text{RES}}$ = “L”. The reset operation is made during the active level of the $\overline{\text{RES}}$ signal.
	$\overline{\text{CS1}}$(SA0) CS2(SA1)	2*2	I	When the parallel interface and the serial interface are selected: These are the chip select signals. The Chip Select of the LSI becomes active when CS1 is “L” and also CS2 is “H” and allows the input/output of data or commands. When the I2C interface is selected: These are the slave address input signals. They set the lower 2 bits of the slave address.
	$\overline{\text{RD}}$ (E)	2	I	The active level of this signal is “L” when connected to an 80-series MPU. This pin is connected to the $\overline{\text{RD}}$ signal of the 80-series MPU, and the data bus of the ML9445 goes into the output state when this signal is “L”. The active level of this signal is “H” when connected to a 68-series MPU. This pin will be the Enable and clock input pin when connected to a 68-series MPU. When a serial interface and I^2C interface are selected (P/$\overline{\text{S}}$ = “L”), fix this pin at “H” or “L” level.
	$\overline{\text{WR}}$ (R/$\overline{\text{W}}$)	2	I	The active level of this signal is “L” when connected to an 80-series MPU. This pin is connected to the $\overline{\text{WR}}$ signal of the 80-series MPU. The data on the data bus is latched into the ML9445 at the rising edge of the $\overline{\text{WR}}$ signal. When connected to a 68-series MPU, this pin becomes the input pin for the Read/Write control signal. R/$\overline{\text{W}}$ = “H”: Read, R/$\overline{\text{W}}$ = “L”: Write When a serial interface and I^2C interface are selected (P/$\overline{\text{S}}$ = “L”), fix this pin at “H” or “L” level.

<table>
<tr><th>Function</th><th>Pin name</th><th>Number of pins</th><th>I/O</th><th>Description</th></tr>
<tr><td rowspan="3">MPU Interface</td><td>C86</td><td>2</td><td>I</td><td>This is the pin for selecting the MPU interface type.
When parallel interface is selected (P/$\overline{S}$ = “H”):
C86 = “H”: 68-Series MPU interface.
C86 = “L”: 80-Series MPU interface.
When serial interface and I^2C interface are selected (P/$\overline{S}$ = “L”):
C86 = “H”: Serial interface.
C86 = “L”: I^2C interface.</td></tr>
<tr><td>P/$\overline{S}$</td><td>2</td><td>I</td><td>P/$\overline{S}$ = “H”: Parallel interface.
P/$\overline{S}$ = “L”: Serial interface or I^2C interface.
The pins of the LSI have the following functions depending on the state of P/$\overline{S}$ input.
<table>
<tr><th>P/$\overline{S}$</th><th>Data/command</th><th>Data</th><th>Read/Write</th><th>Serial clock</th></tr>
<tr><td>“H”</td><td>A0</td><td>DB0 to DB7</td><td>$\overline{RD}$, $\overline{WR}$</td><td>—</td></tr>
<tr><td>“L”</td><td>A0</td><td>SI/SDA (DB7)</td><td>—</td><td>SCL(DB6)</td></tr>
</table>
During serial data input, it is not possible to read the display data in the RAM</td></tr>
<tr><td>SDAACK</td><td>2</td><td>I</td><td>The I^2C bus acknowledge output signal. Normally, use it as it is connected with the SDA pin. Connect an external pull-up resistor whenever necessary, as it is an open drain pin. The pull-up connection destination supply voltage shall be the V_{DD} supply voltage or less.</td></tr>
<tr><td>Oscillator circuit</td><td>CLS</td><td>2</td><td>I</td><td>This is the pin for selecting whether to enable or disable the internal oscillator circuit for the display clock.
CLS = “H”: The internal oscillator circuit is enabled.
CLS = “L”: The internal oscillator circuit is disabled (External input).
When CLS = “L”, the display clock is input at the pin CL.</td></tr>
<tr><td>Display timing generator circuit</td><td>M/$\overline{S}$</td><td>2</td><td>I</td><td>This is the pin for selecting whether master operation or slave operation is made towards the ML9445. During slave operation, the synchronization with the LCD display system is achieved by inputting the timing signals necessary for LCD display.
M/$\overline{S}$ = “H”: Master operation
M/$\overline{S}$ = “L”: Slave operation
The functions of the different circuits and pins will be as follows depending on the states of M/$\overline{S}$ and CLS signals.
<table>
<tr><th>M/$\overline{S}$</th><th>CLS</th><th>Oscillator circuit</th><th>Power supply circuit</th><th>CL</th><th>FR</th><th>SYNC</th><th>$\overline{DOF}$</th></tr>
<tr><td rowspan="2">“H”</td><td>“H”</td><td>Enabled</td><td>Enabled</td><td>Output</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>“L”</td><td>Disabled</td><td>Enabled</td><td>Input</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td rowspan="2">“L”</td><td>“H”</td><td>Disabled</td><td>Disabled</td><td>Input</td><td>Input</td><td>Input</td><td>Input</td></tr>
<tr><td>“L”</td><td>Disabled</td><td>Disabled</td><td>Input</td><td>Input</td><td>Input</td><td>Input</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Function</th><th>Pin name</th><th>Number of pins</th><th>I/O</th><th>Description</th></tr>
<tr><td rowspan="4">Display timing generator circuit</td><td>CL</td><td>2</td><td>I/O</td><td>This is the clock input/output pin.
The function of this pin will be as follows depending on the states of M/$\overline{S}$ and CLS signals.
<table><tr><th>M/$\overline{S}$</th><th>CLS</th><th>CL</th></tr><tr><td rowspan="2">“H”</td><td>“H”</td><td>Output</td></tr><tr><td>“L”</td><td>Input</td></tr><tr><td rowspan="2">“L”</td><td>“H”</td><td>Input</td></tr><tr><td>“L”</td><td>Input</td></tr></table>
When the ML9445 is used in the master/slave mode, the corresponding CL pin has to be connected.</td></tr>
<tr><td>FR</td><td>2</td><td>I/O</td><td>This is the input/output pin for LCD display frame reversal signal.
M/$\overline{S}$ = “H”: Output
M/$\overline{S}$ = “L”: Input
When the ML9445 is used in the master/slave mode, the corresponding FR pin has to be connected.</td></tr>
<tr><td>$\overline{DOF}$</td><td>2</td><td>I/O</td><td>This is the blanking control pin for the LCD display.
M/$\overline{S}$ = “H”: Output
M/$\overline{S}$ = “L”: Input
When the ML9445 is used in the master/slave mode, the corresponding $\overline{DOF}$ pin has to be connected.</td></tr>
<tr><td>SYNC</td><td>2</td><td>I/O</td><td>This is the input/output pin for LCD synchronize signal.
When the ML9445 is used in the master/slave mode, the corresponding SYNC pin has to be connected.</td></tr>
<tr><td rowspan="5">Power supply circuit</td><td>IRS</td><td>2</td><td>I</td><td>This is the pin for selecting the resistor for adjusting the voltage V1.
IRS = “H”: The internal resistor is used.
IRS = “L”: The internal resistor is not used. The voltage V1 is adjusted using the external potential divider resistors connected to the pins VR. This pin is effective only in the master operation. This pin is tied to the “H” or the “L” level during slave operation.</td></tr>
<tr><td>V_{DD}</td><td>10</td><td>—</td><td>These pins are tied to the MPU power supply pin V_{CC}.</td></tr>
<tr><td>V_{SS}</td><td>12</td><td>—</td><td>These are the 0 V pins connected to the system ground (GND).</td></tr>
<tr><td>VCH</td><td>3</td><td>—</td><td>These pins are internal logic power supply pin.
Connect capacitors between V_{SS} pin.</td></tr>
<tr><td>V_{IN}</td><td>3</td><td>—</td><td>These are the reference power supply pins of the voltage multiplier circuit for driving the LCD.</td></tr>
</table>

<table>
<tr><th>Function</th><th>Pin name</th><th>Number of pins</th><th>I/O</th><th>Description</th></tr>
<tr><td rowspan="10">Power supply circuit</td><td>V_{RS}</td><td>2</td><td>—</td><td>These are the output pins for the LCD power supply voltage adjustment circuit. Leave these pins open.</td></tr>
<tr><td>V_{OUT1}</td><td>4</td><td>I/O</td><td>These are the output pins during 1st voltage multiplication.
Connect a capacitor between these pins and V_{SS}.</td></tr>
<tr><td>V_H</td><td>4</td><td>I/O</td><td>These are the power input/output pins during 2nd voltage multiplication.
Connect a capacitor between these pins and V_{SS}.</td></tr>
<tr><td>V_{OUT2}</td><td>3</td><td>I/O</td><td>These are the output pins during 2nd voltage multiplication.
Connect a capacitor between these pins and V_{SS}.</td></tr>
<tr><td>V1
V2
V3
V4
V5</td><td>4*5</td><td>I/O</td><td>These are the multiple level power supply pins for the LCD power supply. The voltages specified for the LCD cells are applied to these pins after resistor network voltage division or after impedance transformation using operational amplifiers. The voltages are specified taking V_{SS} as the reference, and the following relationship should be maintained among them.
$V1 \geq V2 \geq V3 \geq V4 \geq V5 \geq V_{SS}$
Master operation: When the power supply is ON, the following voltages are applied to V2 to V5 from the built-in power supply circuit. The selection of voltages is determined by the LCD bias set command.
<table>
<tr><td>Bias</td><td>1/4</td><td>1/5</td><td>1/6</td><td>1/7</td><td>1/8</td><td>1/9</td></tr>
<tr><td>V2</td><td>3/4×V1</td><td>4/5×V1</td><td>5/6×V1</td><td>6/7×V1</td><td>7/8×V1</td><td>8/9×V1</td></tr>
<tr><td>V3</td><td>2/4×V1</td><td>3/5×V1</td><td>4/6×V1</td><td>5/7×V1</td><td>6/8×V1</td><td>7/9×V1</td></tr>
<tr><td>V4</td><td>2/4×V1</td><td>2/5×V1</td><td>2/6×V1</td><td>2/7×V1</td><td>2/8×V1</td><td>2/9×V1</td></tr>
<tr><td>V5</td><td>1/4×V1</td><td>1/5×V1</td><td>1/6×V1</td><td>1/7×V1</td><td>1/8×V1</td><td>1/9×V1</td></tr>
</table></td></tr>
<tr><td>VR</td><td>2</td><td>I</td><td>Voltage adjustment pins. Voltages between V1 and V_{SS} are applied using a resistance voltage divider. These pins are effective only when the internal resistors for voltage V1 adjustment are not used (IRS = “L”).
Do not use these pins when the internal resistors for voltage V1 adjustment are used (IRS = “H”).</td></tr>
<tr><td>VS1–</td><td>7</td><td>O</td><td>These are the pins for connecting the negative side of the capacitors for 1st voltage multiplication.
Connect capacitors between these pins and VC3+, VC5+.</td></tr>
<tr><td>VS2–</td><td>7</td><td>O</td><td>These are the pins for connecting the negative side of the capacitors for 1st voltage multiplication.
Connect capacitors between these pins and VC4+, VC6+.</td></tr>
<tr><td>VC2+</td><td>5</td><td>I</td><td>These are the input pins for 1st voltage multiplication.
This pin inputs voltage which is open or same with V_{IN} depending on voltage multiplication scaling factor.</td></tr>
<tr><td>VC3+</td><td>5</td><td>I/O</td><td>These are the input pins for 1st voltage multiplication.
Apply the voltage equal to V_{IN} to the pins or leave them open, depending on voltage multiplication values.</td></tr>
</table>

<table>
<tr><th>Function</th><th>Pin name</th><th>Number of pins</th><th>I/O</th><th>Description</th></tr>
<tr><td rowspan="5">Power supply circuit</td><td>VC4+</td><td>5</td><td>I/O</td><td>These are the pins for connecting the positive side of the capacitors for 1^{st} voltage multiplication. Connect capacitors between VS2– and these pins. For 3-time voltage multiplication, the pins are configured as inputs for voltage multiplication.</td></tr>
<tr><td>VC5+</td><td>5</td><td>I/O</td><td>These are the pins for connecting the positive side of the capacitors for 1^{st} voltage multiplication. Connect capacitors between VS1– and these pins. For 2-time voltage multiplication, the pins are configured as inputs for voltage multiplication.</td></tr>
<tr><td>VC6+</td><td>5</td><td>O</td><td>These are the pins for connecting the positive side of the capacitors for 1^{st} voltage multiplication.
Connect capacitors between VS2– and these pins.</td></tr>
<tr><td>VS3-</td><td>4</td><td>O</td><td>These are the pins for connecting the positive side of the capacitors for 2^{nd} voltage multiplication.
Connect capacitors between VC7+ and these pins.</td></tr>
<tr><td>VC7+</td><td>4</td><td>O</td><td>These are the pins for connecting the positive side of the capacitors for 2^{nd} voltage multiplication.
Connect capacitors between VS3- and these pins.</td></tr>
<tr><td rowspan="2">LCD Drive output</td><td>SEG0 to SEG179</td><td>180</td><td>O</td><td>These are the LCD segment drive outputs.
One of the levels among V1, V3, V4, and V_{SS} is selected depending on the combination of the display RAM content and the FR signal
<table>
<tr><th rowspan="2">RAM Data</th><th rowspan="2">FR</th><th colspan="2">Output voltage</th></tr>
<tr><th>Forward display</th><th>Reverse display</th></tr>
<tr><td>H</td><td>H</td><td>V1</td><td>V3</td></tr>
<tr><td>H</td><td>L</td><td>V_{SS}</td><td>V4</td></tr>
<tr><td>L</td><td>H</td><td>V3</td><td>V1</td></tr>
<tr><td>L</td><td>L</td><td>V4</td><td>V_{SS}</td></tr>
<tr><td>Power save</td><td>—</td><td colspan="2">V_{SS}</td></tr>
</table>
The output voltage is V_{SS} when the Display OFF command is executed.</td></tr>
<tr><td>COM0 to COM63</td><td>64</td><td>O</td><td>These are the LCD common drive outputs.
One of the levels among V1, V2, V5, and V_{SS} is selected depending on the combination of the scan data and the FR signal.
<table>
<tr><th>Scan data</th><th>FR</th><th>Output voltage</th></tr>
<tr><td>H</td><td>H</td><td>V_{SS}</td></tr>
<tr><td>H</td><td>L</td><td>V1</td></tr>
<tr><td>L</td><td>H</td><td>V2</td></tr>
<tr><td>L</td><td>L</td><td>V5</td></tr>
<tr><td>Power save</td><td>—</td><td>V_{SS}</td></tr>
</table>
The output voltage is V_{SS} when the Display OFF command is executed.</td></tr>
</table>

Function	Pin name	Number of pins	I/O	Description
LCD Drive output	COMS0 COMS1	2	O	These are the common output pins only for indicators. Both pins output the same signal. Leave these pins open when they are not used. The same signal is output in both master and slave operation modes.
Temp sensor	SVD2	2	O	This is analog voltage output pin for temperature sensor.
Test pin	TEST1 TEST3	2*2	I	These are the pins for testing the IC chip. It has a Internal pull-down resistor. Use it as it is connected to GND.
	TEST2	2	I	This pins for testing the IC chip. Leave these pins open during normal use.
—	DUMMY	31	—	This is a floating pin. Avoid this pin from shorting with pins other than DUMMY in the wiring on the Chip On Glass.

FUNCTIONAL DESCRIPTION

MPU Interface

• Selection of interface type

The ML9445 carries out data transfer using either the 8-bit bi-directional data bus (DB0 to DB7) or the serial data input line (SI/SDA). Either the 8-bit parallel data input or serial data input can be selected interfaces as shown in Table 2 by setting the P/$\overline{S}$ pin and C86 pin to the "H" or the "L" level.

Table 2 Selection of interface type (parallel/serial/I^2C)

P/$\overline{S}$	C86	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	DB7	DB6	DB0 to DB5
H: Parallel input	H:68	$\overline{CS1}$	CS2	A0	E	R/$\overline{W}$	DB7	DB6	DB0 to DB5
	L:80	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	DB7	DB6	DB0 to DB5
L: Serial input	H: Serial	$\overline{CS1}$	CS2	A0	—	—	SI	SCL	—
I^2C	L:I^2C	SA0	SA1	—	—	—	SDA	SCL	—

A hyphen (—) indicates that the pin can be tied to the "H" or the "L" level.

• Parallel interface

When the parallel interface is selected, (P/$\overline{S}$ = "H"), it is possible to connect this LSI directly to the MPU bus of either an 80-series MPU or a 68-series MPU as shown in Table 3. depending on whether the pin C86 is set to "H" or "L".

Table 3 Selection of MPU during parallel interface (80–/68–series)

C86	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	DB0 to DB7
H: 68-Series MPU bus	$\overline{CS1}$	CS2	A0	E	R/$\overline{W}$	DB0 to DB7
L: 80-Series MPU bus	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	DB0 to DB7

The data bus signals are identified as shown in Table 4 below depending on the combination of the signals A0, $\overline{RD}$ (E), and $\overline{WR}$ (R/$\overline{W}$) of Table 3.

Table 4 Identification of data bus signals during parallel interface

	Common	68-Series	80-Series	
	A0	R/$\overline{W}$	$\overline{RD}$	$\overline{WR}$
Display data read	1	1	0	1
Display data write	1	0	1	0
Status read	0	1	0	1
Control data write (command)	0	0	1	0

Serial Interface

When the serial interface is selected (P/$\overline{S}$ = “L”, C86 =“H”), the serial data input (SI) and the serial clock input (SCL) can be accepted if the chip is in the active state ($\overline{CS1}$ = “L” and CS2 = “H”). The serial interface consists of an 8-bit shift register and a 3-bit counter. The serial data is read in from the serial data input pin in the sequence DB7, DB6, ... , DB0 at the rising edge of the serial clock input, and is converted into parallel data at the rising edge of the 8th serial clock pulse and processed further. The identification of whether the serial data is display data or command is judged based on the A0 input, and the data is treated as display data when A0 is “H” and as command when A0 is “L”. The A0 input is read in and identified at the rising edge of the (8 × n) th serial clock pulse after the chip has become active. Fig. 1 shows the signal chart of the serial interface. (When the chip is not active, the shift register and the counter are reset to their initial states. No data read out is possible in the case of the serial interface. It is necessary to take sufficient care about wiring termination reflection and external noise in the case of the SCL signal. We recommend verification of operation in an actual unit.)

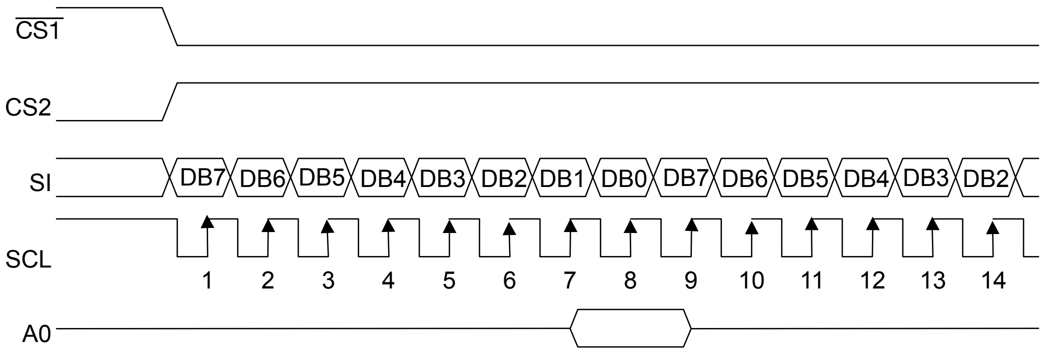
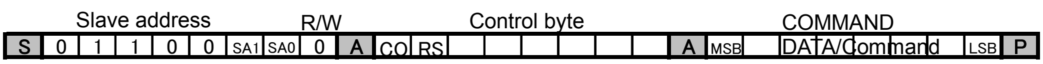


Fig. 1 Signal chart during serial interface

• I²C Interface



Salve address: 0 1 1 0 0

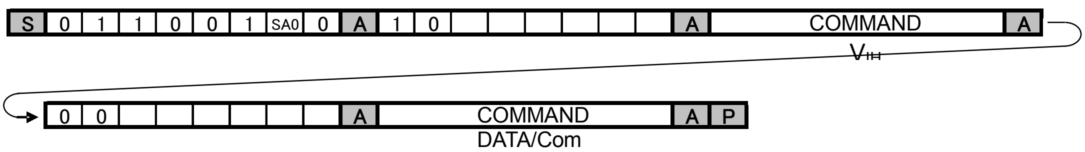
CO: Consecutive control byte setting bit
0: Last control byte, 1: Consecutive control byte
RS: Command/data setting bit
0: Command data, 1: Display data

When the I²C interface is selected (P/$\overline{S}$ = “L”, C86 =“L”), the I²C data input (SDA) and the I²C clock input (SCL) can be data input. For the I²C interface, each IC is assigned with a 7-bit slave address. The first one byte in the transfer consists of this 7-bit slave address and the R/W bit that indicates the data transfer direction. Always input "0" to the eighth R/W bit because the ML9445 is a write-only LSI.
The eight bits next to the slave address is a control byte. The first one bit is CO: consecutive command setting bit and the next one bit is RS: command/data setting bit (the remaining six bits are the Don't care bits).
When CO = "0": Means the last control byte.
When CO = "1": Means the control bytes are successively input.
When RS = "0": Means the data to be input next is the command data.
When RS = "1": Means the data to be input next is the display data.
The display data can be successively input.

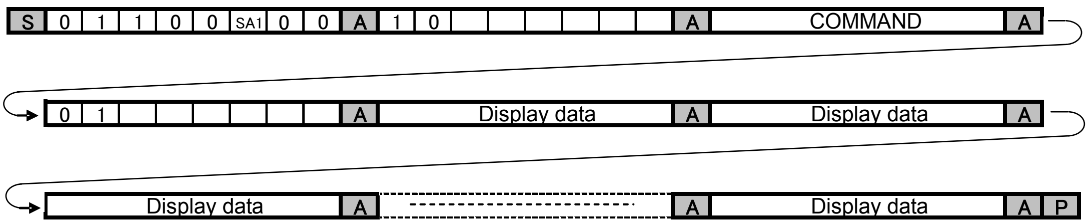
Example of Data Setting

- When inputting two commands

When inputting two commands



- When inputting the command and display data



• Chip select
The ML9445 has the two chip select pins $\overline{CS1}$ and CS2, and the MPU interface or the serial interface is enabled only when $\overline{CS1}$ = "L" and CS2 = "H". When the chip select signals are in the inactive state, the DB0 to DB7 lines will be in the high impedance state and the inputs A0, $\overline{RD}$, and $\overline{WR}$ will not be effective. When the serial interface has been selected, the shift register and the counter are reset when the chip select signals are in the inactive state. When the I2C interface is selected, CS1 and CS2 become the slave address setting pins SA0 and SA1.

• Accessing the display data RAM and the internal registers
Accessing the ML9445 from the MPU side requires merely that the cycle time (t_{CYC}) be satisfied, and high speed data transfer without requiring any wait time is possible. Also, during the data transfer with the MPU, the ML9445 carries out a type of pipeline processing between LSIs via a bus holder associated with the internal data bus. For example, when the MPU writes data in the display data RAM, the data is temporarily stored in the bus holder, and is then written into the display data RAM before the next data read cycle. Further, when the MPU reads out data in the display data RAM, first a dummy data read cycle is carried out to temporarily store the data in the bus holder which is then placed on the system bus and is read out during the next read cycle. There is a restriction on the read sequence of the display data RAM, which is that the read instruction immediately after setting the address does not read out the data of that address, but that data is output as the data of the address specified during the second data read sequence, and hence care should be taken about this during reading. Therefore, always one dummy read is necessary immediately after setting the address or after a write cycle: (The status read cannot use dummy read cycles.) This relationship is shown in Figs 2(a) and 2(b).

• Data write

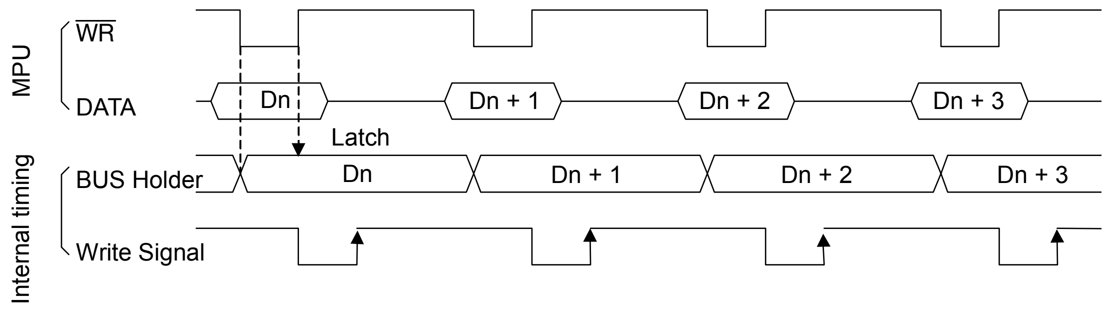


Fig. 2(a) Write sequence of display data RAM

• Data read

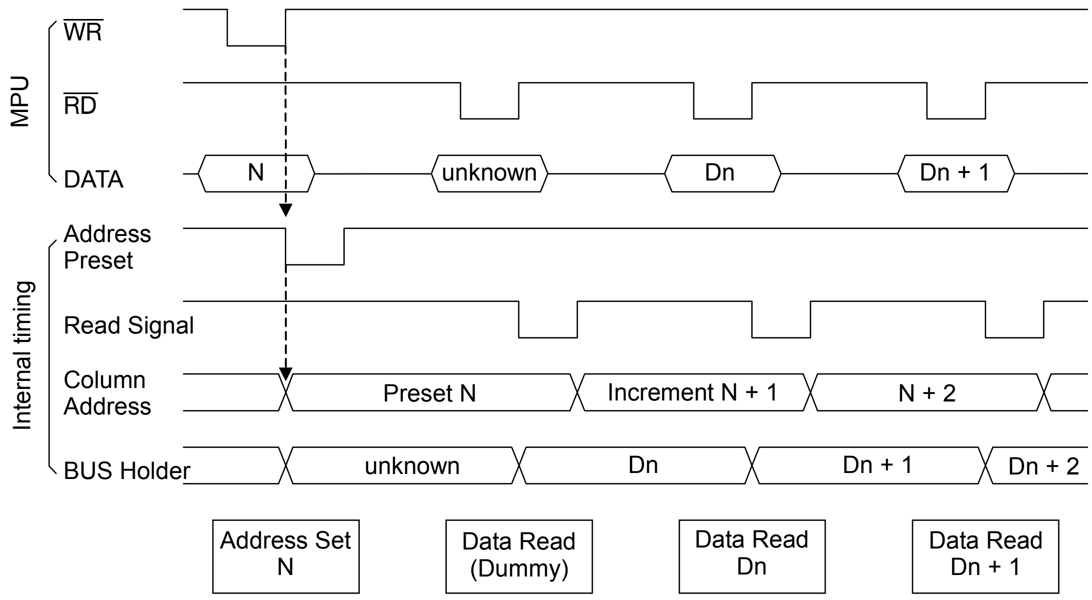


Fig. 2(b) Read sequence of display data RAM

Dn = Data
N = Address data

Display Data RAM

• Display data RAM

This is the RAM storing the dot data for display and has an organization of 65 (8 pages × 8 bits +1) × 180 × 2 bits. It is possible to access any required bit by specifying the page address and the column address. Since the display data DB7 to DB0 from the MPU corresponds to the LCD display in the direction of the common lines as shown in Fig. 3, there are fewer restrictions during display data transfer when the ML9445 is used in a multiple chip configuration, thereby making it easily possible to realize a display with a high degree of freedom. Also, since the display data RAM read/write from the MPU side is carried out via an I/O buffer, it is done independent of the signal read operation for the LCD drive. Consequently, the display is not affected by flickering, etc., even when the display data RAM is accessed asynchronously during the LCD display operation.

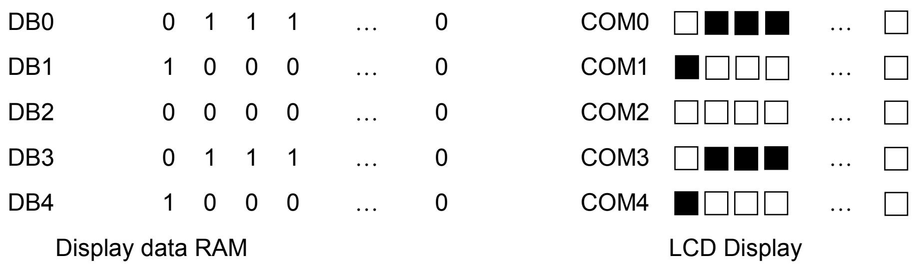


Fig. 3 Relationship between display data RAM and LCD display

• Page address circuit / Column address circuit

The page address of the display data RAM is specified using the page address set command as shown in Fig. 4. For Address incremental direction, either the column direction or page direction can be selected by the Display Data Input Direction Select command. Whichever direction is chosen, increment is carried out by positive one(+1) after write or read operation.

When the column direction is selected for address increment, the column address is increased by +1 for every write or read operation. After the column address has accessed up to B3H, the page address is incremented by +1 and the column address shifts to 00H.

When the page direction is selected for address increment, the page address is increased with the column address locked in position. When the page address has accessed up to Page17, the column address is incremented by +1, and the page address goes to Page 0.

Whichever direction is selected for address increment, the page address goes back to Page 0 and column address to 00H after access up to the column address B3H of page address Page17.

Also, as is shown in Table 5, it is possible to reverse the correspondence relationship between the display data RAM column address and the segment output using the ADC command (the segment driver direction select command). This reduces the IC placement restrictions at the time of assembling LCD modules.

Table 5 Correspondence relationship between the display data RAM column address and the segment output

ADC	SEGMENT Output				
	SEG0				SEG179
DB0 = "0"	00(H)	→	Column Address	→	B3(H)
DB0 = "1"	B3(H)	←	Column Address	←	00(H)

• Line address circuit
The line address circuit is used for specifying the line address corresponding to the common output when displaying the contents of the display data RAM as is shown in Fig. 4. Normally, the topmost line in the display is specified using the display start line address set command (COM0 output in the forward display state of the common output, and COM63 output in the reverse display state). The display area starts from the specified display start line address to cover the area corresponding to the lines specified by the Duty Set command in the direction where the line address increments.

It is possible to carry out screen scrolling by dynamically changing the line address using the display start line address set command.

• Display data latch circuit
The display data latch circuit is a latch for temporarily storing the data from the display data RAM before being output to the LCD drive circuits. Since the commands for selecting forward/reverse display and turning the display ON/OFF control the data in this latch, the data in the display data RAM will not be changed.

Oscillator Circuit

This is an RC oscillator that generates the display clock. The oscillator circuit is effective only when M/$\overline{S}$ = "H" and also CLS = "H". The oscillations will be stopped when CLS = "L", and the display clock has to be input to the CL pin.

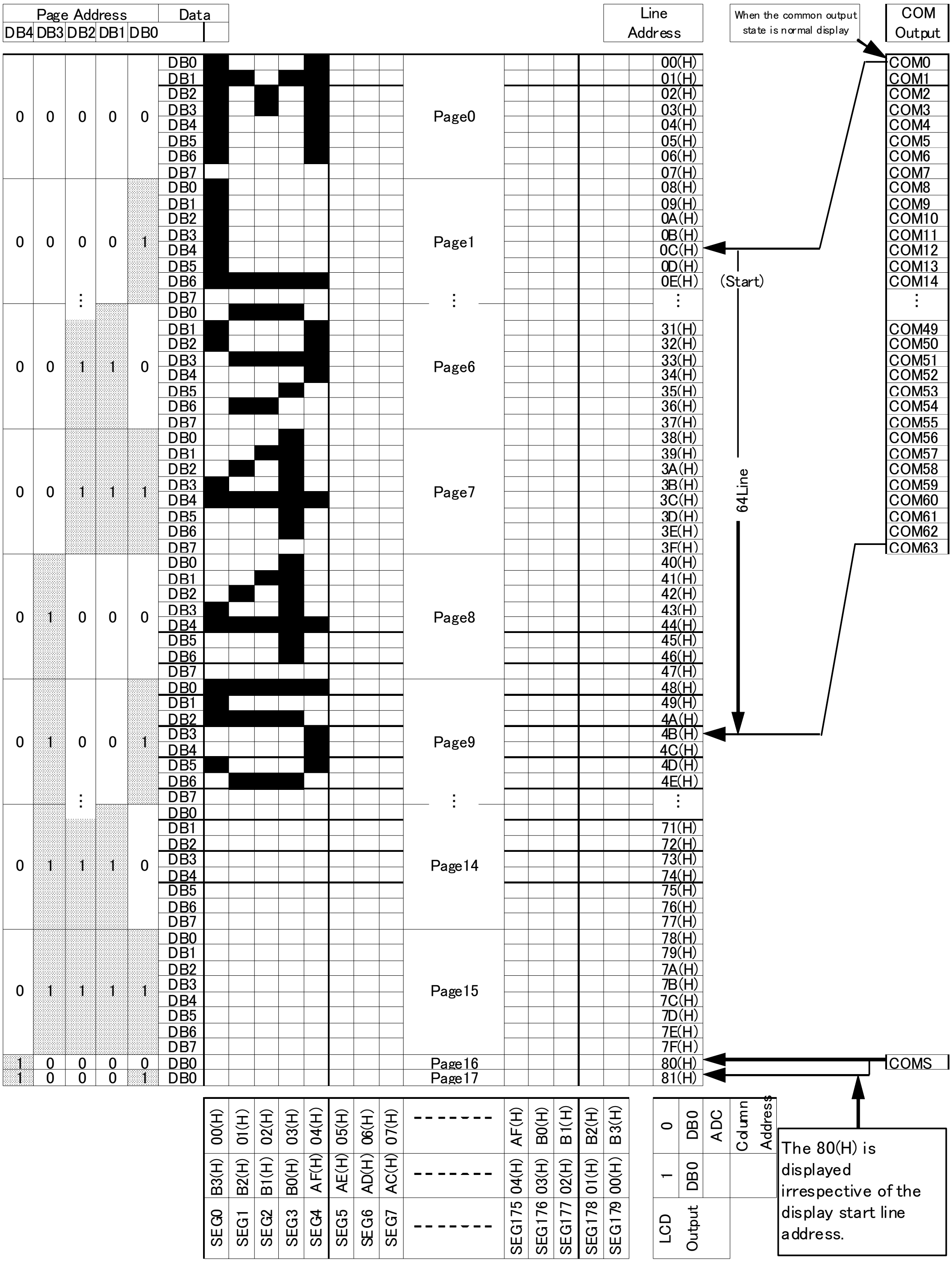


Fig. 4 Display data RAM address map

Display Timing Generator Circuit

This circuit generates the timing signals for the line address circuit and the display data latch circuit from the display clock. The display data is latched in the display data latch circuit and is output to the segment drive output pins in synchronization with the display clock. This circuit generates the timing signals for the line address circuit and the display data latch circuit from the display clock. The display data is latched in the display data latch circuit and is output to the segment drive output pins in synchronization with the display clock. The read out of the display data to the LCD drive circuits is completely independent of the display data RAM access from the MPU. As a result, there is no bad influence such as flickering on the display even when the display data RAM is accessed asynchronously during the LCD display. Also, the internal common timing and LCD frame reversal (FR), field start signal (SYNC) are generated by this circuit from the display clock. The drive waveforms of the frame reversal drive method shown in Fig. 5(a) for the LCD drive circuits are generated by this circuit. The drive waveforms of the line reversal drive method shown in Fig. 5(b) are also generated by the command.

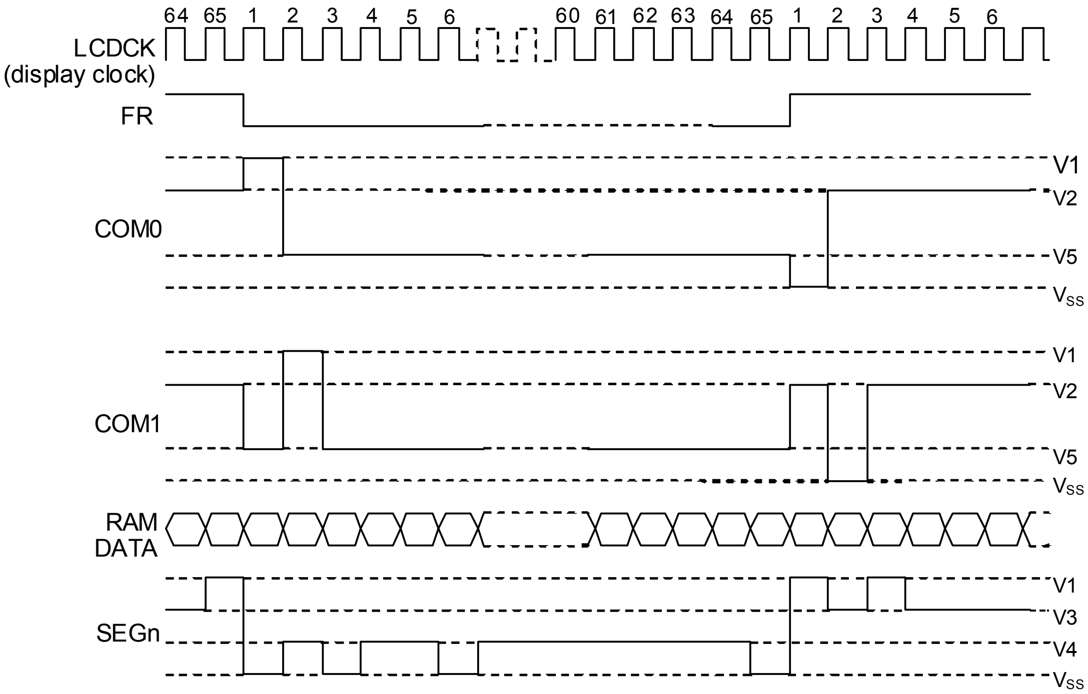


Fig. 5(a) Waveforms in the frame reversal drive method

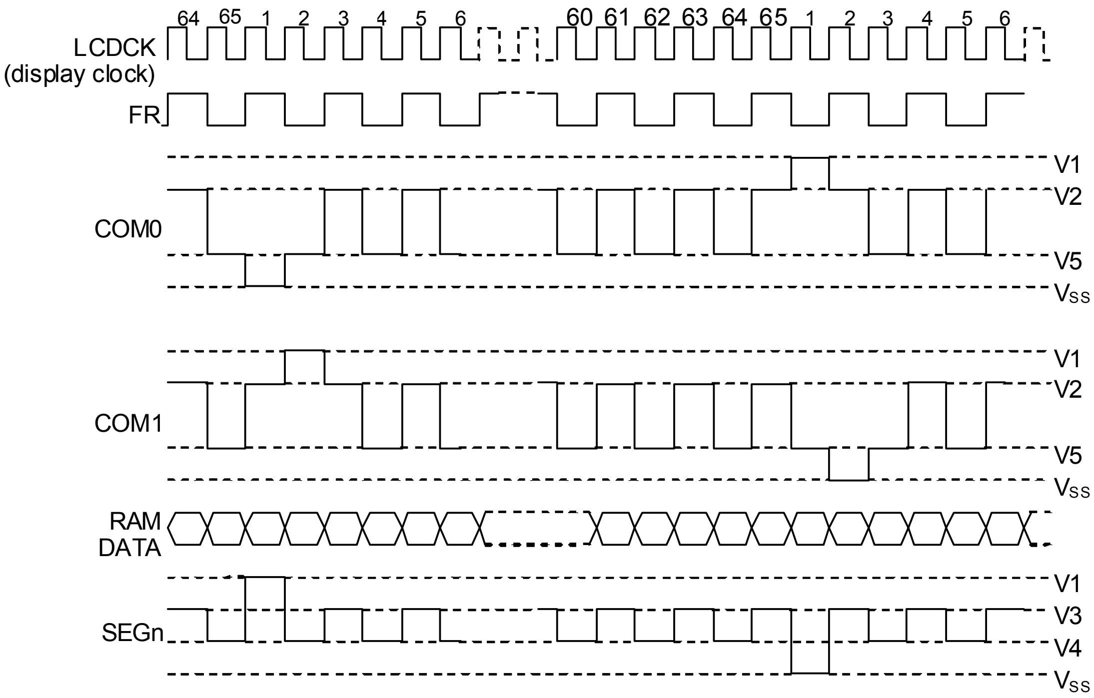


Fig. 5(b) Waveforms in the line reversal drive method

When the ML9445 is used in a multiple chip configuration, it is necessary to supply the slave side display timing signals (FR, CL, and $\overline{\text{DOF}}$) from the master side.
The statuses of the signals FR, CL, and $\overline{\text{DOF}}$ are shown in Table 6.

Table 6 Display timing signals in master mode and slave mode

Operating mode		FR	CL	$\overline{\text{DOF}}$	SYNC
Master mode (M/$\overline{\text{S}}$ = "H")	Internal oscillator circuit enabled (CLS = H)	Output	Output	Output	Output
	Internal oscillator circuit disabled (CLS = L)	Output	Input	Output	Output
Slave mode (M/$\overline{\text{S}}$ = "L")	Internal oscillator circuit disabled (CLS = H)	Input	Input	Input	Input
	Internal oscillator circuit disabled (CLS = L)	Input	Input	Input	Input

Common Output State Selection Circuit (see Table 7)

Since the common output scanning directions can be set using the common output state selection command in the ML9445, it is possible to reduce the IC placement restrictions at the time of assembling LCD modules.

Table 7 Common output state settings

State	Common Scanning direction
Forward Display	COM0 → COM63
Reverse Display	COM63 → COM0

LCD Drive Circuit

This LSI incorporates 246 sets of multiplexers for the ML9445 that generate 4-level outputs for driving the LCD. These output the LCD drive voltage in accordance with the combination of the display data, common scanning signals, and the FR signal. Fig. 6 shows examples of the segment and common output waveforms in the frame reversal drive method.

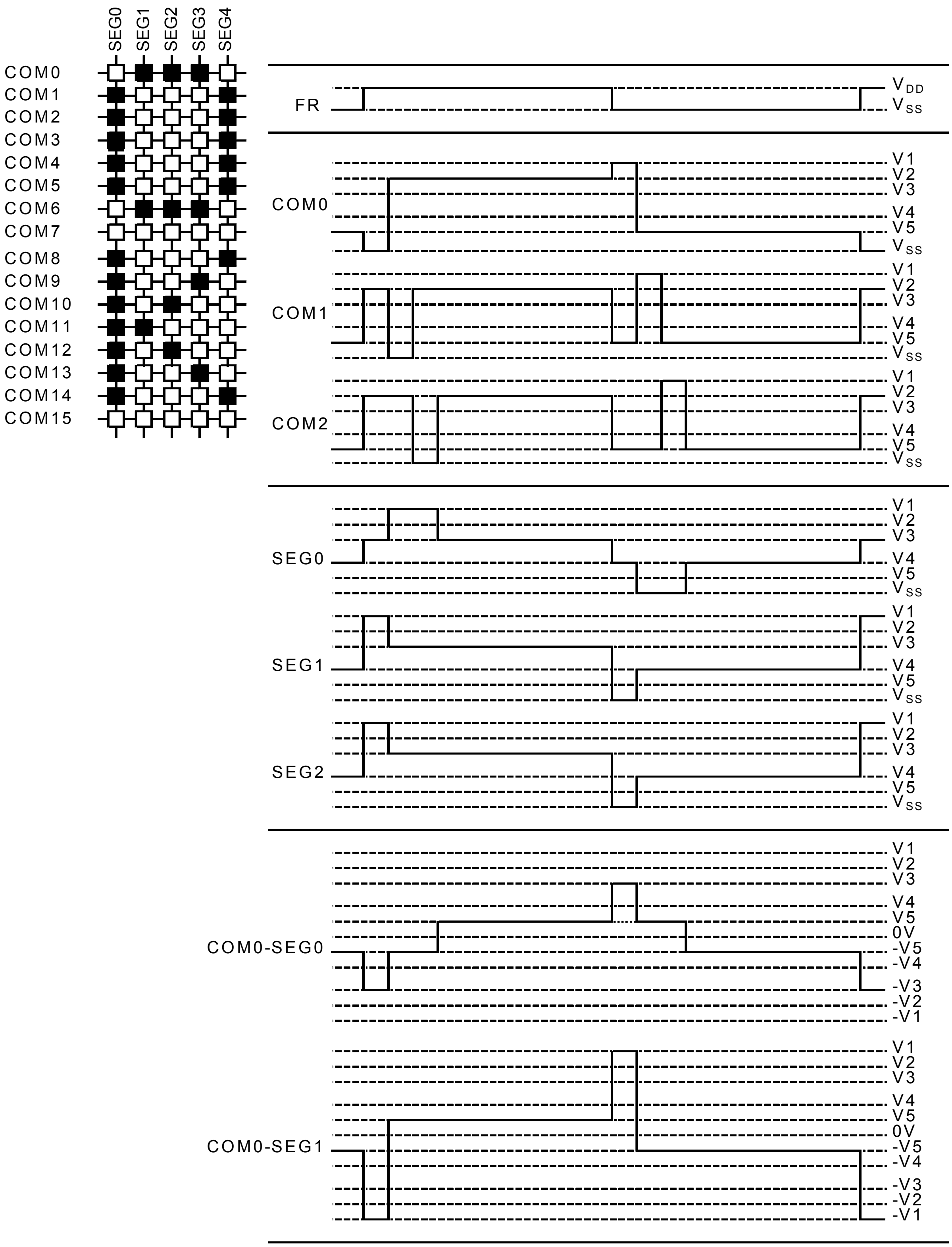


Fig. 6 Output waveforms in the frame reversal drive method (FR waveform/common waveform/segment waveform/voltage difference between common and segment)

Power Supply Circuit

The ML9445 includes a power supply circuit for generating the voltage required for driving liquid crystals, consisting of four blocks; the 1st voltage multiplier circuit, 2nd voltage multiplier circuit, V1 voltage adjustment circuit, and voltage follower circuit. The circuit is effective only when the master operates. In the power supply circuit, it is possible to control the ON/OFF of each of the circuits of the 1st voltage multiplier circuit, 2nd voltage multipliers circuit, V1 voltage adjustment circuit, and voltage follower circuit separately, by using the power control set command. As a result, it is possible to use some parts of functions of both the external power supply and the internal power supply. Table 8-1 describes the functions controlled by the 4-bit data of the power control set command and Table 8-2 outlines the functions of power supply blocks.
Figure 6-2 shows the voltage relationship among the power supply circuit blocks.

Table 8-1 Details of functions controlled by the bits of the power control set command

Control bit	Function controlled by the bit
DB3	2nd Voltage multiplier circuit control bit
DB2	1st Voltage multiplier circuit control bit
DB1	Voltage adjustment circuit (V1 voltage adjustment circuit) control bit
DB0	Voltage follower circuit (V/F circuit) control bit

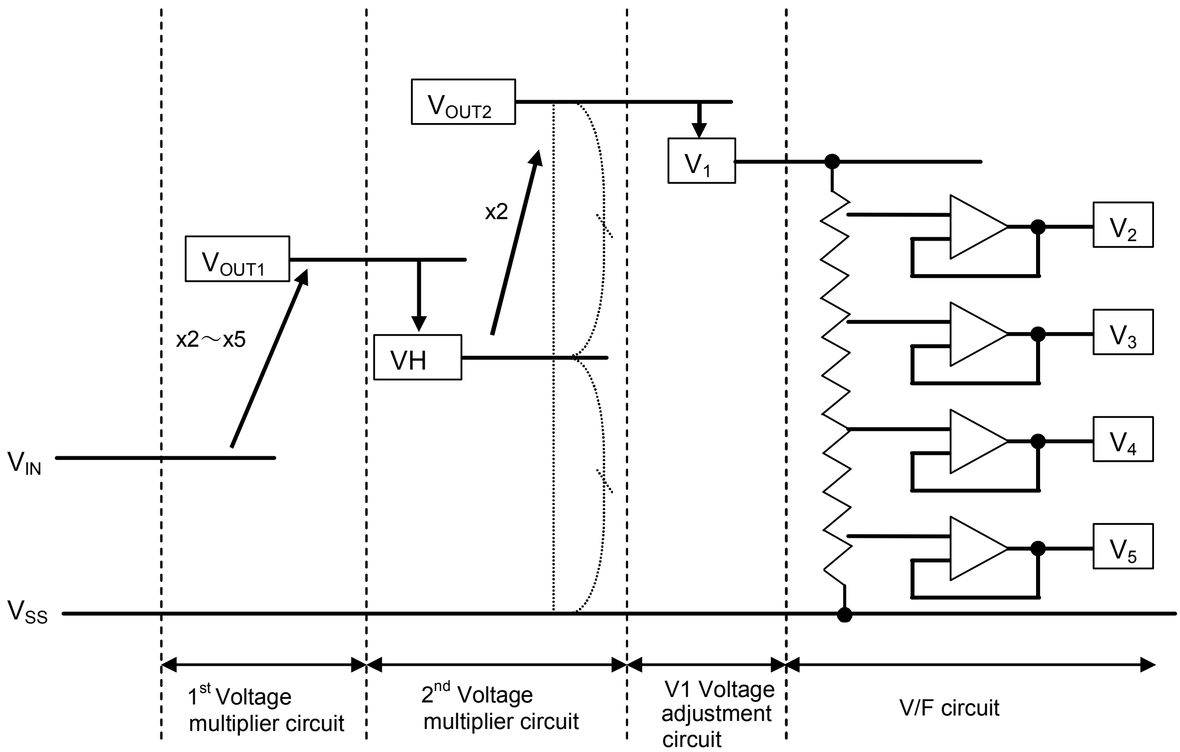


Fig. 6-2 The Voltage relationship among the power supply circuit blocks.

Table 8-2 Overview of Power Supply Block Functions

Parameter	Function	Input Voltage	Output Voltage
1st Voltage multiplier circuit	Generates a multiplied voltage VOUT1 by multiplying the voltage between VIN and GND using the charge pump. Connecting a capacitor for voltage multiplication allows you to multiply the voltage by 2 to 5 times.	V_{IN}	V_{OUT1}
2nd Voltage multiplier circuit	Consists of a voltage adjustment circuit and a 2-time voltage multiplier circuit. The voltage adjustment circuit generates VRS as the base voltage of the 2-time voltage multiplier circuit, and then the 2-time voltage multiplier circuit generates VOUT2 by multiplying VRS by 2 times.	V_{OUT1}	VH, V_{OUT2}
V1 voltage adjustment circuit	This circuit adjusts the V1 voltage and generates the LCD drive voltage V1.	V_{OUT2}	V1
Voltage follower circuit	Resistive division is performed between V1 and VSS with a specified bias ratio, and the LCD drive voltages V2, V3, V4, and V5 are generated by the voltage follower.	V1	V2, V3, V4, V5

For the combination of power supply circuit operations, the six possible states shown in Table 9 can be set by the register value of the power control set command.

Table 9 Sample combination for reference

No.	State used	DB3	DB2	DB1	DB0	Circuit				External voltage input
						2nd Voltage multiplier	1st Voltage multiplier	V1 Adjustment	V/F	
1	Only the internal power supply is used	1	1	1	1	ON	ON	ON	ON	V_{IN}
2	Only the internal power supply is used (2nd Voltage multiplier is not used)	0	1	1	1	OFF	ON	ON	ON	V_{IN}
3	Only the internal power supply is used (1st Voltage multiplier is not used)	1	0	1	1	ON	OFF	ON	ON	V_{OUT1}
4	V1 adjustment and V/F circuits are used	0	0	1	1	OFF	OFF	ON	ON	V_{OUT2}
5	Only V/F circuits are used	0	0	0	1	OFF	OFF	OFF	ON	V1
6	Only the external power supply is used	0	0	0	0	OFF	OFF	OFF	OFF	V1 to V5

If combinations other than the above are used, normal operation is not guaranteed.

1, The 1st voltage multiplier circuit, 2nd voltage multipliers circuit, V1 voltage adjustment circuit, and V/F circuit are used(all internal power supplies)

Use this combination when not using the power supply from the external. All voltages required for driving LCD are generated from the VIN voltage. All internal power supplies are used. See Figure 13-1.

2, Only the 1st voltage multiplier circuit, V1 voltage adjustment circuit, and V/F circuit are used (2nd voltage multiplier circuit is not used)

Use this combination when not using the power supply from the external. All voltages required for driving LCD are generated from the VIN voltage.
The number of capacitors for voltage multiplication can be reduced by stopping the 2nd voltage multiplier circuit. Short V_{OUT1}, V_H, and V_{OUT2} to use this combination. See Figure 13-2.

3, Only the 2nd voltage multiplier circuit, V1 voltage adjustment circuit, and V/F circuit are used (1st voltage multiplier circuit is not used)

Use this combination when the V_{OUT1} voltage can be supplied from the external. Although the capacitor for the 1st voltage multiplication is not connected, set the command to use the 1st voltage multiplier circuit (DB2 = “0”). See Figure 13-3.

4, Only the V1 voltage adjustment circuit and V/F circuit are used

Use this combination when the V_{OUT2} voltage can be supplied from the external. The V2, V3, V4, and V5 voltages are generated, which are the LCD drive voltages generated by the internal V1 voltage adjustment circuit and V/F circuit. Connect capacitors for retaining voltages to the V1 to V5 pins. The V1 voltage can be adjusted by the V1 voltage adjustment command and the electronic potentiometer command. See Figure 13-4.

5, Only the V/F circuit is used

Use this combination when the V1 voltage can be supplied from the external.
Connect capacitors for retaining voltages to the V2, V3, V4, and V5 pins which output the LCD drive voltages generated by the V/F circuit. See Figure 13-5.

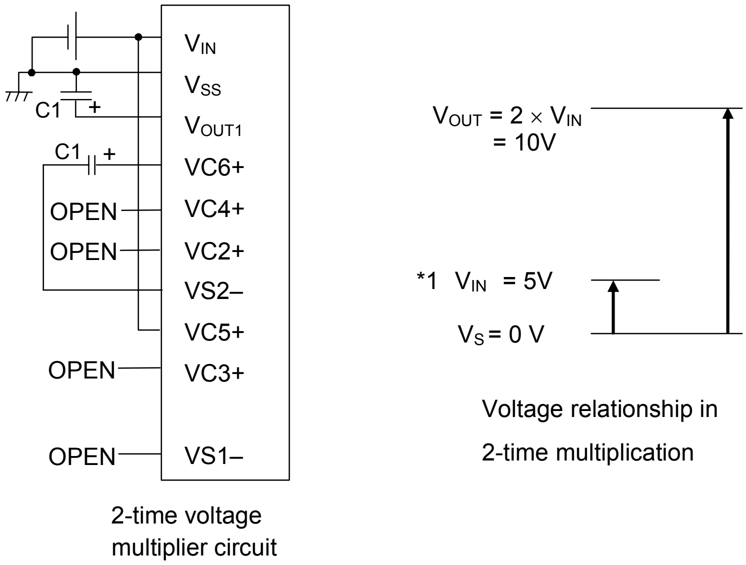
6, Only the external power supply is used (all internal power supplies are OFF)

Use this combination when the V1, V2, V3, V4, and V5 voltages can be supplied from the external.
See Figure 13-6.

• 1st Voltage multiplier circuits

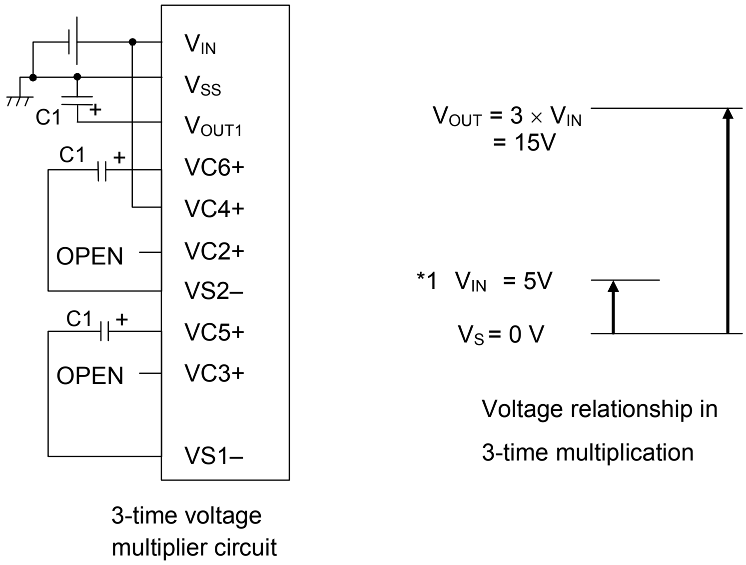
The 1st voltage multiplier circuit can multiply the VIN to VSS voltage by 2, 3, 4, or 5 times.
Fig. 7-1 to 7-4 show the circuit connections and the voltage relationships.

Fig. 7-1 2-time voltage multiplier circuit and voltage relationships in 2-time multiplication



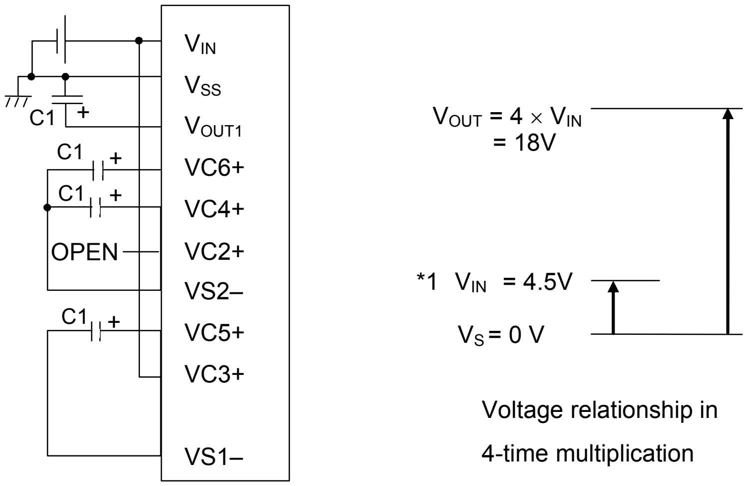
Connect capacitors between VC6+ and VS2- and between V_{OUT1} and V_{SS}, open the VC4+, VC2+, VC3+, and VS1- pins, and short the V_{IN} and VC5+ pins to use this connection. Should be used in the range of VIN = 3 to 5.5 V.

Fig. 7-2 3-time voltage multiplier circuit and voltage relationships in 3-time multiplication



Connect capacitors between VC6+ and VS2-, between VC5+ and VS1-, and between V_{OUT1} and V_{SS}, open the VC2+, and VC3+ pins, and short the V_{IN} and VC4+ pins to use this connection.
Should be used in the range of VIN = 2.7 to 5.5 V.

Fig. 7-3 4-time voltage multiplier circuit and voltage relationships in 4-time multiplication

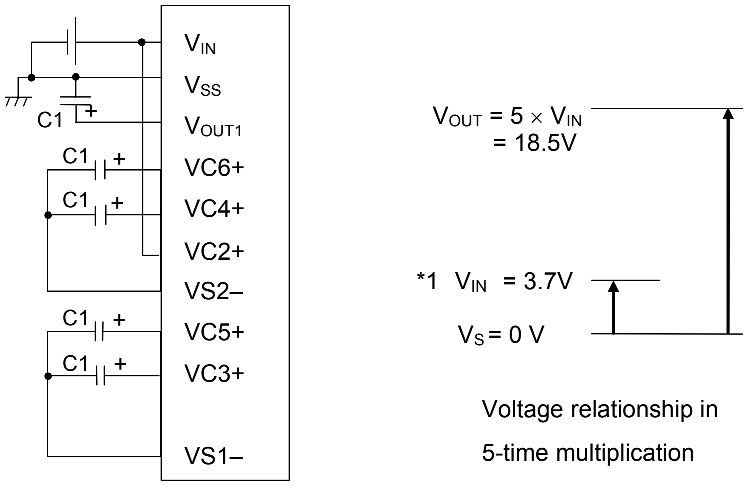


4-time voltage multiplier circuit

Voltage relationship in 4-time multiplication

Connect capacitors between VC6+ and VS2-, between VC4+ and VS2-, between VC5+ and VS1-, and between V_{OUT1} and V_{SS}, open the VC2+ pin, and short the V_{IN} and VC3+ pins.
Should be used in the range of VIN = 2.7 to 4.625 V.

Fig. 7-4 5-time voltage multiplier circuit and voltage relationships in 5-time multiplication



5-time voltage multiplier circuit

Voltage relationship in 5-time multiplication

Connect capacitors between VC6+ and VS2-, between VC4+ and VS2-, between VC5+ and VS1-, between VC3+ and VS1-, and between V_{OUT1} and V_{SS}, and short the V_{IN} and VC2+ pins to use this connection.
Should be used in the range of VIN = 2.7 to 3.7 V.

*1: The voltage range of V_{IN} should be set from 6V to 18.5V so that the voltage at the pin V_{OUT} does not exceed the voltage multiplier output voltage operating range.

• 2nd Voltage multiplier circuits

It consists of a voltage adjustment circuit and 2-time voltage multiplier circuit. The voltage adjustment circuit operates in V_{OUT1} voltage systems, generates V_H which is the base voltage of the 2nd voltage multiplier circuit, and generates V_{OUT2} with 2-time voltage multiplication of V_H.
The connection example for 2nd voltage multiplier circuits is shown in Fig. 9.

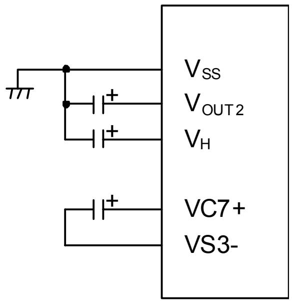


Fig. 9 Connection examples for 2nd voltage multiplier circuits

Connect capacitors between V_{OUT2} and V_{SS}, between V_H and V_{SS}, and between VC7+ and VS3-.
When you stop the 2nd voltage multiplier circuit and operate the V1 voltage adjustment circuit with the 1st boost output, short the V_{OUT2} pin to use V_H and V_{OUT2}.

• Voltage adjustment circuit

The voltage multiplier output V_{OUT} produces the LCD drive voltage V1 via the voltage adjustment circuit. Since the ML9445 incorporates a high accuracy constant voltage generator, a 128-level electronic potentiometer function, and also resistors for voltage V1 adjustment, it is possible to build a high accuracy voltage adjustment circuit with very few components.

(a) When the internal resistors for voltage V1 adjustment are used

It is possible to control the LCD power supply voltage V1 and adjust the intensity of LCD display using commands and without needing any external resistors, if the internal voltage V1 adjustment resistors and the electronic potentiometer function are used. The voltage V1 can be obtained by the following equation A-1 or A-2 in the range of V1<VOUT.

Electronic potentiometer setting, DB7=0

$V1 = (1 + (Rb/Ra)) \bullet VEV = (1 + (Rb/Ra)) \bullet (1 - (\alpha/600)) \bullet VREG$ (Eqn. A-1)

Electronic potentiometer setting, DB7=1

$V1 = (1 + (Rb/Ra)) \bullet VEV = (1 + (Rb/Ra)) \bullet (1 - (\alpha/300)) \bullet VREG$ (Eqn. A-2)

With the setting of the most significant bit for the electronic potentiometer setting, the values of ΔV for each step can be changed. DB7=1 has 2-time ΔV than DB7=0.

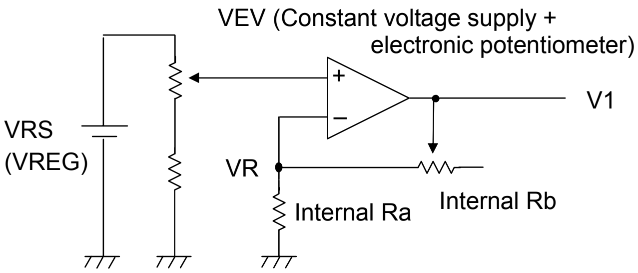


Fig. 10 V1 voltage adjustment circuit (equivalent circuit)

VREG is a constant voltage generated inside the IC and VRS pin output voltage.
Here, α is the electronic potentiometer function which allows one level among 128 levels to be selected by merely setting the data in the 7-bit electronic potentiometer register. The values of α set by the electronic potentiometer register are shown in Table 10.

Table 10 Relationship between electronic potentiometer register and α

α	DB6	DB5	DB4	DB3	DB2	DB1	DB0
127	0	0	0	0	0	0	0
126	0	0	0	0	0	0	1
125	0	0	0	0	0	1	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	1	0
0	1	1	1	1	1	1	1

For the V1 voltage setting using the electronic potentiometer function, the nominal value of the V1 output voltage accuracy is ±2.5%.

This value is shown under the following conditions: Ta=25℃, 4-time the voltage V1 adjustment internal resistor ratio, external resistor Vout=18.5V, no V1 load, and display OFF. Rb/Ra is the voltage V1 adjustment internal resistor ratio and can be adjusted to one of 8 levels by the voltage V1 adjustment internal resistor ratio set command. The reference values of the ratio (1 + Rb/Ra) according to the 3-bit data set in the voltage V1 adjustment internal resistor ratio setting register are listed in Table 11.

Table 11 Voltage V1 adjustment internal resistor ratio setting register values and the ratio (1+Rb/Ra) (Nominal)

Register			(1 + Rb/Ra)
DB2	DB1	DB0	
0	0	0	2.5
0	0	1	3.0
0	1	0	3.5
0	1	1	4.0
1	0	0	4.5
1	0	1	5.0
1	1	0	5.5
1	1	1	6.0

Note: Use V1 gain in the range from 2.5 to 6 times. Because this LSI has temperature gradient, V1 voltage rises at lower temperatures. When using V1 gain of 6 times, adjust the built-in electronic potentiometer so that V1 voltage does not exceed 18.5 V.

When V1 is set using the built-in resistance ratio, the accuracies are shown in Table 12.

Table 12 Relation between V1 Output Voltage Accuracy and V1 Gain Using Built-in Resistor

Parameter	V1 gain								Unit
	2.5 times	3 times	3.5 times	4 times	4.5 times	5 times	5.5 times	6 times	
V1 output voltage accuracy	±2.5	±2.5	±2.5	±2.5	±2.5	±2.5	±2.5	±2.5	%
V1 maximum output voltage	7.5	9	10.5	12	13.5	15	16.5	18	V

Note: The V1 maximum output voltages in Table 12 are nominal values when Tj = 25°C, and electronic potentiometer α = 0. The V1 output voltage accuracy in Table 12 are values when V1 load current I = 0 µA, 18.5 V is externally input to V_{OUT}, and display is turned OFF.

(b) When external resistors are used (voltage V1 adjustment internal resistors are not used)
It is also possible to set the LCD drive power supply voltage V1 without using the internal resistors for voltage V1 adjustment but connecting external resistors (Ra' and Rb') between V_{SS} & VR and between VR & V1. Even in this case, it is possible to control the LCD power supply voltage V1 and adjust the intensity of LCD display using commands if the electronic potentiometer function is used.
The voltage V1 can be obtained by the following equation B-1 or B-2 in the range of $V1<V_{OUT}$ by setting the external resistors Ra' and Rb' appropriately.

When the Electronic potentiometer setting DB7=0
$V1 = (1 + (Rb'/Ra')) \bullet VEV = (1 + (Rb'/Ra')) \bullet (1 - (\alpha/600)) \bullet VREG$ (Eqn. B-1)

When the Electronic potentiometer setting DB7=1
$V1 = (1 + (Rb'/Ra')) \bullet VEV = (1 + (Rb'/Ra')) \bullet (1 - (\alpha/300)) \bullet VREG$ (Eqn. B-2)

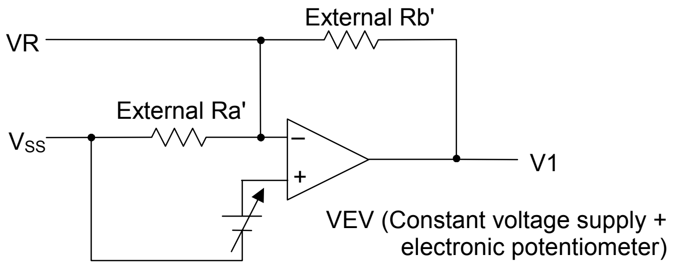


Fig. 11 V1 voltage adjustment circuit (equivalent circuit)

Setting example: Setting V1 = 7 V at Tj = 25°C

When the electronic potentiometer register value is set to the middle value of (DB7, DB6, DB5, DB4, DB3, DB2, DB1, DB0) = (0, 1, 0, 0, 0, 0, 0, 0), the value of α will be 63 and that of VREG will be 3.0 V, and hence the equation B-1 becomes as follows:

V1 = (1 + (Rb'/Ra')) • (1 – (α/600)) • VREG
7 = (1 + (Rb'/Ra')) • (1 – (63/600)) • 3.0 (Eqn. B-3)

Further, if the current flowing through Ra' and Rb' is set as 5 µA, the value of Ra' + Rb' will be - Ra' + Rb' = 1.4 MΩ (Eqn. B-4)
and hence,
Rb'/Ra' = 1.61, Ra' = 537 kΩ, Rb' = 863 kΩ.
In this case, the variability range of voltage V1 using the electronic potentiometer function will be as given in Table 13.

Table 13 Example 1 of V1 variable-voltage range using electronic potentiometer function

V1	Min	Typ	Max	Unit
Variable-voltage range	6.17 (α = 127)	7.0 (α = 31)	7.82 (α = 0)	[V]

(c) When external resistors are used (voltage V1 adjustment internal resistors are not used) and a variable resistor is also used
It is possible to set the LCD drive power supply voltage V1 using fine adjustment of Ra' and Rb' by adding a variable resistor to the case of using external resistors in the above case. Even in this case, it is possible to control the LCD power supply voltage V1 and adjust the intensity of LCD display using commands if the electronic potentiometer function is used.
The voltage V1 can be obtained by the following equation C-1 and C-2 in the range of V1<V_{OUT} by setting the external resistors R_1, R_2 (variable resistor), and R_3 appropriately and making fine adjustment of R_2 (ΔR_2).

When the Electronic potentiometer setting DB7=0
V1 = $(1 + (R_3 + R_2 - \Delta R_2)/(R_1 + \Delta R_2))$ • VEV
= $(1 + (R_3 + R_2 - \Delta R_2)/(R_1 + \Delta R_2))$ • (1 – (α/600)) • VREG (Eqn. C-1)

When the Electronic potentiometer setting DB7=1
V1 = $(1 + (R_3 + R_2 - \Delta R_2)/(R_1 + \Delta R_2))$ • VEV
= $(1 + (R_3 + R_2 - \Delta R_2)/(R_1 + \Delta R_2))$ • (1 – (α/300)) • VREG (Eqn. C-2)

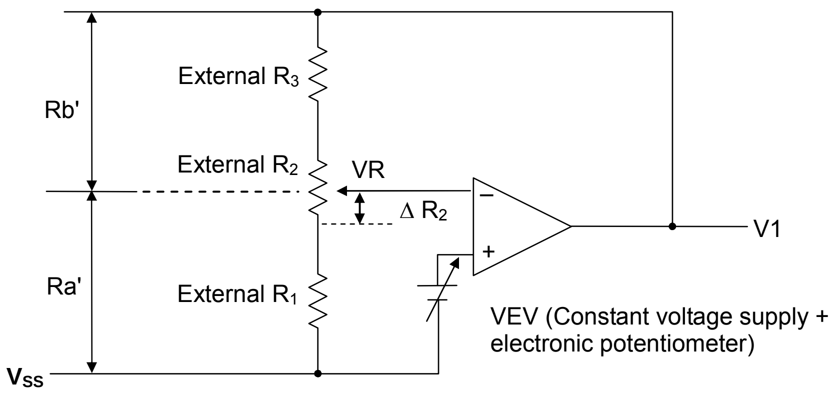


Fig. 12 V1 voltage adjustment circuit (equivalent circuit)

Setting example: Setting V1 in the range 5 V to 9 V using R_2 at Tj = 25°C .

When the electronic potentiometer register value is set to (DB5, DB4, DB3, DB2, DB1, DB0) = (1, 0, 0, 0, 0, 0), the value of α will be 63 and that of VREG will be 3.0 V, and hence in order to make V1 = 9 V when $\Delta R_2 = 0\Omega$, the equation C-1 becomes as follows:
$9 = (1 + (R_3 + R_2)/R_1) \bullet (1 - (63/600)) \bullet (3.0)$ (Eqn. C-2)
In order to make V1 = 5 V when $\Delta R_2 = R_2$,
$5 = (1 + R_3/(R_1+R_2)) \bullet (1 - (63/600)) \bullet (3.0)$ (Eqn. C-3)
Further, if the current flowing between V_{SS} and V1 is set as 5 μA, the value of $R_1 + R_2 + R_3$ becomes-
$R_1 + R_2 + R_3 = 1.8\ M\Omega$ (Eqn. C-4)
and hence,
$R_1 = 537\ k\Omega$, $R_2 = 430\ k\Omega$, $R_3 = 833\ k\Omega$.
In this case, the variability range of voltage V1 using the electronic potentiometer function and the increment size will be as given in Table 14.

Table 14 Example 2 of V1 variable-voltage range using electronic potentiometer function and variable resistor

V1	Min	Typ	Max	Unit
Variable-voltage range	4.40(α = 127)	7.0 (α = 63)	10.06 (α = 0)	[V]

In Figures 11 and 12, the voltage VEV is obtained by the following equation by setting the electronic potentiometer between 0 and 127.

VEV = (1 - (α/600)) • VREG
α = 0 : VEV = (1 – (0/600)) • 3.0 V = 3.0 V
α = 63 : VEV = (1 – (63/600)) • 3.0 V = 2.680 V
α = 127 : VEV = (1 – (127/600)) • 3.0 V = 2.365 V

The increment size of the electronic potentiometer at VEV when VREG = 3.0 is :

$$\Delta = \frac{3.0 - 2.365}{127} = 5\ mV\ (Nominal)$$

When the electronic potentiometer register value is set to DB7= 1

VEV=(1-(α/300))•VREG

α=0 : VEV = (1 – (0/300)) • 3.0V = 3.0V
α=63 : VEV = (1 – (63/300)) • 3.0V = 2.360V
α=127 : VEV = (1 – (127/300)) • 3.0V = 1.730V

When VREG = 3.0 V
The increment size is :

$$\Delta = \frac{3.0\ \text{V} - 1.730\ \text{V}}{127} = 10\ \text{mV (Nominal)}$$

* When using the voltage V1 adjustment internal resistors or the electronic potentiometer function, it is necessary to set at least the voltage adjustment circuit and the voltage follower circuits both in the operating state using the power control setting command. Also, when the voltage multiplier circuit is OFF, it is necessary to supply a voltage externally to the V_{OUT} pin.
* The pin VR is effective only when the voltage V1 adjustment internal resistors are not used (pin IRS = “L”). Leave this pin open when the voltage V1 adjustment internal resistors are being used (pin IRS = “H”).
* Since the input impedance of the pin VR is high, it is necessary to take noise countermeasures such as using short wiring length or a shielded wire .
* The supply current increases in proportion to the panel capacitance. When power consumption increases, the V_{OUT} level may fall. The voltage (V_{OUT} – V1) should be more than 3 V.

• LCD Drive voltage generator circuits
The voltage V1 is converted by resistive divider to produce V2, V3, V4, and V5 voltages. V2, V3, V4, and V5 voltages are impedance – converted by the voltage follower, and is supplied to the LCD voltage generator circuits. A bias ratio is chosen by the bias set command.

Table 15 Relationship between LCD bias set command and V2,V3,V4,V5

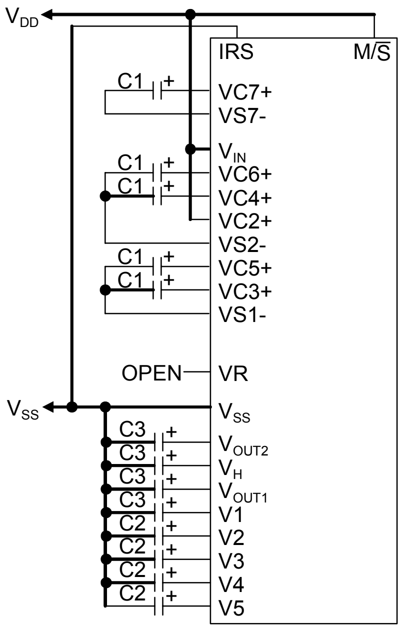
Voltage	LCD Bias Set Command Register Value (DB2, DB1, DB0)					
	(0, 0, 0) 1/4 bias	(0, 0, 1) 1/5 bias	(0, 1, 0) 1/6 bias	(0, 1, 1) 1/7 bias	(1, 0, 0) 1/8 bias	(1, 0, 1) 1/9 bias
V2	3/4•V1	4/5•V1	5/6•V1	6/7•V1	7/8•V1	8/9•V1
V3	2/4•V1	3/5•V1	4/6•V1	5/7•V1	6/8•V1	7/9•V1
V4	2/4•V1	2/5•V1	2/6•V1	2/7•V1	2/8•V1	2/9•V1
V5	1/4•V1	1/5•V1	1/6•V1	1/7•V1	1/8•V1	1/9•V1

• Application circuits

Fig. 13-1 to 13-6 show reference examples of power supply circuits.
(Two V1 pins are described in the following examples for explanation, but they are the same.)

Fig. 13-1 When all internal power supplies are used

VIN = VDD, 5-time voltage multiplication.
The internal V1 voltage adjustment resistor is used.



VIN = VDD, 5-time voltage multiplication.
The internal V1 voltage adjustment resistor is not used.

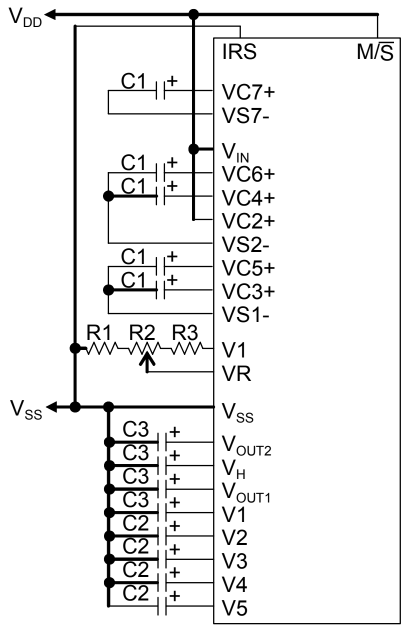


Fig. 13-2 When using the 1st voltage multiplier circuit, voltage adjustment circuit, and V/F circuit (2nd voltage multiplier circuit is stopped)

VIN = VDD, 5-time voltage multiplication.
The internal V1 voltage adjustment resistor is not used.

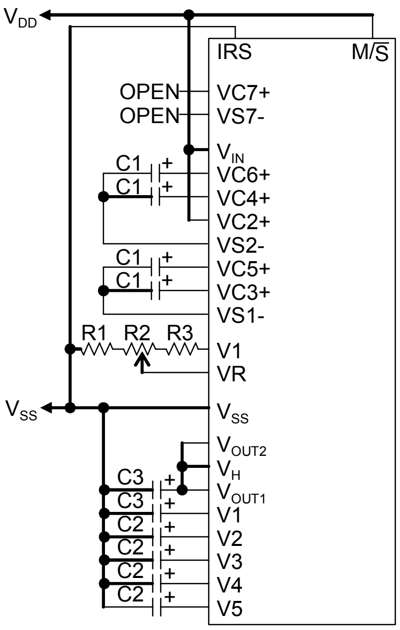


Fig. 13-3 When using the 2nd voltage multiplier circuit, voltage adjustment circuit, and V/F circuit (1st voltage multiplier circuit is stopped)

The voltage multiplier circuits are not used.
The internal V1 voltage adjustment resistor is used.

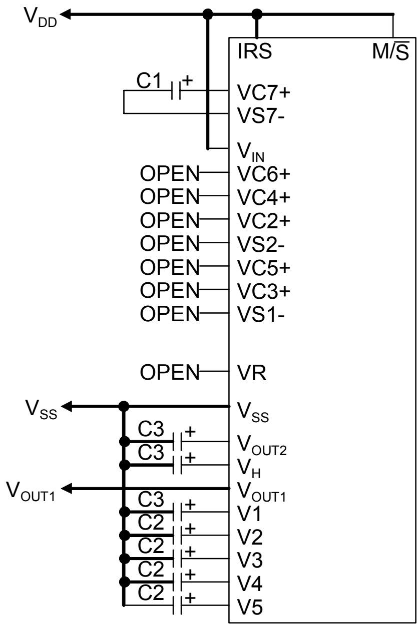


Fig. 13-4 When using only the voltage adjustment circuit and V/F circuit (The 1st and 2nd voltage multiplier circuits are stopped)

The voltage multiplier circuits are not used.
The internal V1 voltage adjustment resistor is used.

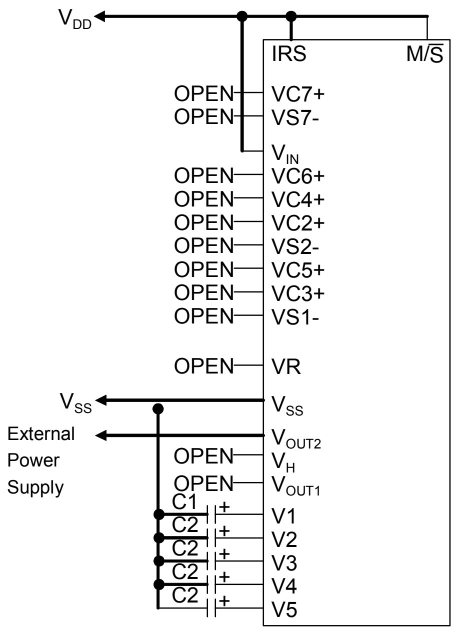


Fig. 13-5 When using only V/F circuit (The 1st and 2nd voltage multiplier circuits and the voltage adjustment circuit are stopped)

The voltage multiplier circuits are not used.
The internal V1 voltage adjustment resistor is used.

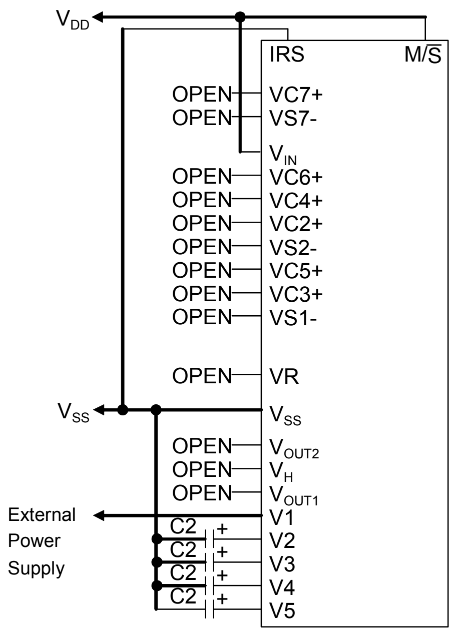
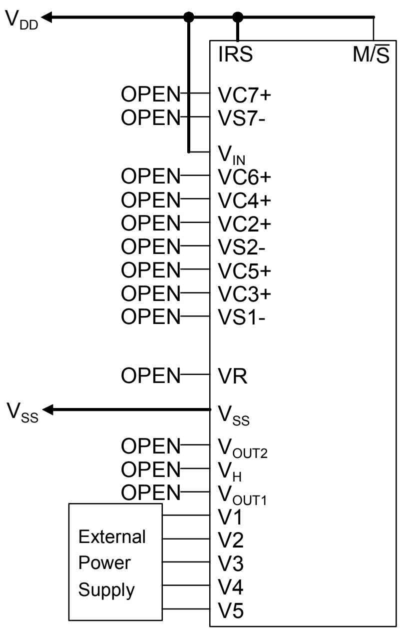


Fig. 13-6 When not using the internal power supply (all supplied from the external)

The voltage multiplier circuits are not used.
The internal V1 voltage adjustment resistor is used.



• Capacitor Setting Reference Values

The optimal values for the capacitors C1 and C2 shown in the reference examples of power supply circuits vary depending on the size of the liquid crystal panel.
Determine the capacitance by displaying a pattern with a heavy load and selecting a value that stabilizes the LCD drive voltage. Table 16 shows the setting reference values for capacitors.

Table 16 Capacitor Setting Reference Values

Symbol	Descriptions	Reference setting value [μF]
C1	Capacity for supply voltage regulation	1.0～4.7
C2	Liguid crystal drive voltage retaining(smoothing) capacitor	0.47～4.7
C3	Capacity for set-up circuits	1.0～4.7

If the LCD panel is so large that the satisfactory display quality cannot be obtained by changing the capacitor values, stop the internal power supply circuit, and supply the LCD drive voltage from the external.

• Notes on COG Mounting

When mounting the COG, there are resistance components caused by ITO wiring between the IC or external connecting parts (capacitor, resistor) and the power supply. These resistance components may degrade the liquid crystal display quality or may malfunction the IC. When designing a liquid crystal module, take the following three points into account and evaluate them under the practical prerequisites.

1, Trace resistance of voltage multiplying system pins
This IC's voltage multiplier circuits are switched with a transistor with very low ON resistance. In mounting the COG, ITO's trace resistance gets into the switching transistor in series and controls the voltage multiplication ability. Pay attention to the proper wiring to each capacitor, including making the ITO wiring as thick as possible.

2, Trace resistance of power supply pins
When current flow occurs momentarily as in case of the display switching, the supply voltage may drop momentarily in synchronization with the occurrence of current flow. If the ITO's wiring resistance to the power supply pin is high at this time, the supply voltage fluctuates greatly inside the IC and may malfunction the IC. Try to reduce the wiring impedance of the power supply line as much as possible to supply stabilized power to the IC.

3, Creation of module sample with changed sheet resistance
Evaluate the sample with the ITO trace resistance value changed, and select a sheet resistance material which has as much operating margin as possible.

4, Recommended ITO resistance value
VDD,VSS,VIN :≦ 50Ω
VS1-,VS2-,VC4+,VC5+,VC6+,VS3-,VC7+ : ≦ 50Ω
VOUT1,VOUT2:≦ 50Ω
VCH,VH,V1,V2,V3,V4,V5 : ≦ 100Ω
DB0～DB7,A0,$\overline{\text{CS1}}$,$\overline{\text{RD}}$,$\overline{\text{WR}}$:≦ 1kΩ
$\overline{\text{RES}}$,SVD2 : ≦ 10kΩ

• Examples of Settings for the Power Supply Circuit

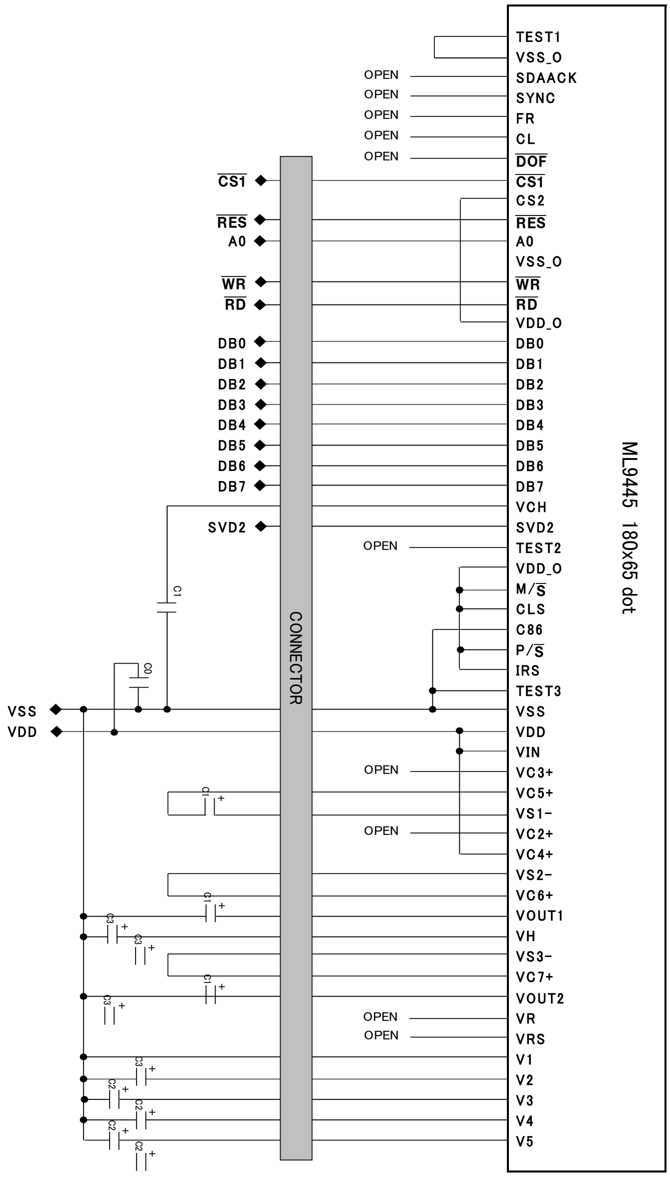
Setting example: Setting VDD=VIN=5V, all internal power supplies are used, V1 voltage=13.475V】

1st voltage multiplier circuit is used (3-time voltage multiplier) (see Figure 7-2)
2nd voltage multiplier circuit is used (see Figure 9)
Power control register: (DB4, DB3, DB2, DB1, DB0) = (1, 1, 1, 1)
Voltage V1 adjustment internal resistance ratio: (1+Rb/Ra) =5.5
  Voltage V1 adjustment internal resistance ratio register: (DB2, DB1, DB0) = (1, 1, 0)
The electronic potentiometer set: α=55
  Electronic potentiometer register: (DB7, DB6, DB5, DB4, DB3, DB2, DB1, DB0) = (1, 1, 0, 0, 1, 0, 0, 0)
Vout1output voltage 5×3=15V
Vout2output voltage 18V

$$V1output = (1 + (Rb/Ra)) \cdot (1 - (\alpha/300)) \cdot VREG$$
$$= 5.5 \times (1-55/300) \times 3$$
$$= 13.475V$$

Adjustment of 9.515V to 16.5V can be performed by setting change of electronic potentiometer register.

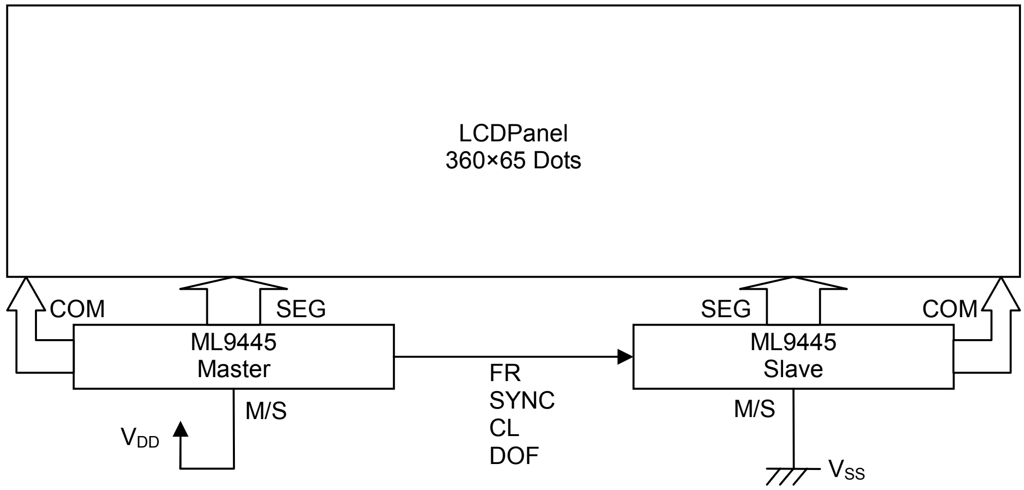
Application circuits



Master Operation: M/S="H"
Parallel Data Input: P/S="H"
80-Series MPU Interface: C86="L"
Internal Oscillation circuit: CLS="H"
V1 Adjusting - Internal Resistor is used : IRS="H"
1st voltage multiplier circuit is used (see Figure 7-2)
2nd voltage multiplier circuit is used
C0=0.1uF, C1=1.0uF, C2=1.0uF, C3=4.7uF

• Cascade Connection Example

It is possible to expand the display area by using the ML9445 in a multiple chip configuration.



* When the internal oscillator circuit is used.
* It is recommended to supply the LCD drive power supply from the external.
* It is possible to use the master-side internal power supply to supply the power to the slave. However, in this case, the required voltage may not be obtained due to the ITO trace resistance or the LCD panel load. Make a thorough evaluation before using this configuration.

• Initial setting

Note: If electric charge remains in smoothing capacitor connected between the LCD driver voltage output pins (V1 to V5) and the V_{SS} pin, a malfunction might occur: the display screen gets dark for an instant when powered on.
To avoid a malfunction at power-on, it is recommended to follow the flowchart in the "EXAMPLES OF SETTINGS FOR THE INSTRUCTIONS" section in page 63.

LIST OF OPERATION

No	Operation		DBn 7 6 5 4 3 2 1 0	A0	RD	WR	Comment
1	Display OFF		1 0 1 0 1 1 1 0	0	1	0	LCD Display: OFF when DB0 = 0 ON when DB0 = 1
	Display ON		1 0 1 0 1 1 1 1	0	1	0	
2	Display	Forward	1 0 1 0 0 1 1 0	0	1	0	Forward or reverse LCD display mode Forward when DB0 = 0 Reverse when DB0 = 1
		Reverse	1 0 1 0 0 1 1 1	0	1	0	
3	LCD All-on display	OFF(Normal display)	1 0 1 0 0 1 0 0	0	1	0	LCD Normal display when DB0 = 0 All-on display when DB0 = 1
		ON	1 0 1 0 0 1 0 1	0	1	0	
4	Common output state select		1 1 0 0 0 1 0 0	0	1	0	Selects the common output scanning direction. Forward when DB0 = 0 Reverse when DB0 = 1
			1 1 0 0 0 1 0 1	0	1	0	
5	Display start line set (2-byte command)		1 0 0 0 1 0 1 0	0	1	0	The display starting line address in the display RAM is set.
			* * address	0	1	0	
6	Page address set (2-byte command)		1 0 1 1 0 0 0 0 * * * address	0	1	0	The page address in the display RAM is set.
7	Column address set (upper bits)		0 0 0 1 address (upper bits)	0	1	0	The upper 4 bits of the column address in the display RAM is set.
	Column address set (lower bits)		0 0 0 0 address (lower bits)	0	1	0	The lower 4 bits of the column address in the display RAM is set.
8	Display data write		Write data	1	1	0	Writes data to the display data RAM.
9	Display data read		Read data	1	0	1	Reads data from the display data RAM.
10	Display data input direction select		1 0 0 0 0 1 0 0	0	1	0	Display RAM data input direction. Column direction when DB0=1 Page direction when DB0=1
			1 0 0 0 0 1 0 1	0	1	0	
11	ADC select	Forward	1 0 1 0 0 0 0 0	0	1	0	Correspondence to the segment output for the display data RAM address. Forward when DB0 = 0 Reverse when DB0 = 1
		Reverse	1 0 1 0 0 0 0 1	0	1	0	
12	n-line inversion drive register set (2-byte command)		0 0 1 1 0 0 0 0 * * * Invert line count	0	1	0	Line invert drive. Set the line count.
13	n-line inversion drive	OFF	1 1 1 0 0 1 0 0	0	1	0	Resets the line invert drive. n-line OFF when DB0 = 0 n-line ON when DB1 = 1
		ON	1 1 1 0 0 1 0 1	0	1	0	
14	Display Duty set (3-byte command)		0 1 1 0 1 1 0 1	0	1	0	Display duty set.
			* * Number of Duty	0	1	0	
			* * Start line	0	1	0	
15	Read-modify-write		1 1 1 0 0 0 0 0	0	1	0	Incrementing column address During a write: +1 During a read: 0
16	end		1 1 1 0 1 1 1 0	0	1	0	Releases the read-modify-write state.
17	Built-in OSC	OFF	1 0 1 0 1 0 1 0	0	1	0	Built-in oscillator circuit operation. OFF when DB0 = 0 ON when DB1 = 1
		ON	1 0 1 0 1 0 1 1	0	1	0	
18	Built-in oscillator frequency select		0 1 1 1 Frequency	0	1	0	Built-in oscillator frequency select.
19	Power control set (2-byte command)		0 0 1 0 1 0 0 0	0	1	0	Select built-in power supply operation state.
			* * * * State	0	1	0	

20	Voltage V1 adjustment internal resistance ratio set		0 0 1 0 0 Resistance ratio setting	0	1	0	Selects the internal resistor ratio.
No	Operation		DBn 7 6 5 4 3 2 1 0	A0	$\overline{RD}$	$\overline{WR}$	Comment
21	LCD bias set (2-byte command)		0 1 0 1 0 0 0 0	0	1	0	Sets the LCD drive voltage bias ratio.
			* * * * * bias	0	1	0	
22	Electronic volume set (2-byte command)		1 0 0 0 0 0 0 1	0	1	0	Sets data in the electronic potentiometer register to adjust the V1 output voltage.
			Electronic volume	0	1	0	
23	Discharge	OFF	1 1 1 0 1 0 1 0	0	1	0	Discharges power supply circuit connection capacitor. OFF when DB0 = 0 ON when DB1 = 1
		ON	1 1 1 0 1 0 1 1	0	1	0	
24	Power save	OFF	1 0 1 0 1 0 0 0	0	1	0	Power save OFF when DB0 = 0 ON when DB1 = 1
		ON	1 0 1 0 1 0 0 1	0	1	0	
25	Temperature gradient select		0 1 0 0 1 gradient	0	1	0	Setting of temperature gradient of LCD voltage.
26	Status read		* * * * * gradient	0	0	1	Issues the temperature gradient select bit.
27	Reset		1 1 1 0 0 0 1 0	0	1	0	Reset command
28	Temperature sensor	OFF	0 1 1 0 1 0 0 0	0	1	0	Temperature sensor OFF when DB0 = 0 ON when DB0 = 1
		ON	0 1 1 0 1 0 0 1	0	1	0	
29	Common output direction select		1 1 0 0 0 0 0 0	0	1	0	DB=0 : COM0→COM1→ →COM63
			1 1 0 0 0 0 0 1	0	1	0	DB=1 : COM0→COM32→COM33→→COM31→COM63
30	Multiplier clock frequency select (2-byte command)		0 1 0 1 0 1 0 1	0	1	0	Multiplier clock frequency select
			* * * * * * Frequency	0	1	0	
31	NOP		1 1 1 0 0 0 1 1	0	1	0	Non-operation command

*: Invalid data (input: Don’t care, output: Unknown)

DESCRIPTIONS OF OPERATION

Display ON/OFF (Write)

This is the command for controlling the turning on or off the LCD panel. The LCD display is turned on when a “1” is written in bit DB0 and is turned off when a “0” is written in this bit.

	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Display ON	0	1	0	1	0	1	1	1	1
Display OFF	0	1	0	1	0	1	1	1	0

Forward/Reverse Display Mode (Write)

It is possible to toggle the display on and off condition without changing the contents of the display data RAM. In this case, the contents of the display data RAM will be retained.

	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	RAM Data
Forward	0	1	0	1	0	0	1	1	0	Display on when “H”
Reverse	0	1	0	1	0	0	1	1	1	Display on when “L”

LCD Display All-on ON/OFF (Write)

Using this command, it is possible to forcibly turn ON all displays irrespective of the contents of the display data RAM. In this case, the contents of the display data RAM will be retained. Also, all displays can be in white in combination with a display inversion command.

	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
All-on display OFF (Normal display)	0	1	0	1	0	0	1	0	0
All-on display ON	0	1	0	1	0	0	1	0	1

The power save mode will be entered into when the Display all-on ON command is executed in the display OFF condition.

Common Output State Select (Write)

This command is used for selecting the scanning direction of the common output pins.

	Scanning direction	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Forward	COM0 → COM63	0	1	1	0	0	0	1	0	0
Reverse	COM63 → COM0	0	1	1	0	0	0	1	0	1

*: Invalid data

Display Start Line Set (2-byte command)

This command specifies the display starting line address in the display data RAM.
Normally, the topmost line in the display is specified using the display start line set command.
It is possible to scroll the display screen by dynamically changing the address using the display start line set command. This command is a 2-byte command to be used together with the Display Start Line Set Mode Set Command and Display Start Line Set Register Set Command. So, be sure to set the both commands continuously.

• Display Start Line Set Mode Set (Write)

When this command is input, the Display Start Line Set Command becomes valid. Once the display start line set mode is selected, any command other than the Display Start Line Set Command cannot be used. This status is released when any data is stored in the register by the Display Start Line Set Command.

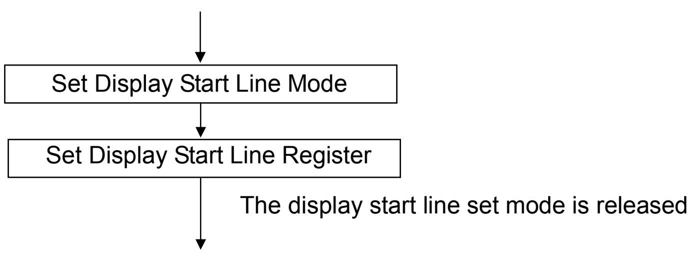
A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	0	0	1	0	1	0

• Display Start Line Set Register Set (Write)

Setting of data to low order 7 bits of the display start line register by this command allows specification of the display start line address of the display data RAM. In addition, the most significant bit is for data setting of COM output pins only for indicators (COMS), and the data of 80H for 0 and 81H for 1 is for indicators.
After the display start line register is set by inputting this command, the display start line mode is released.

Line address	COMS Data	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
00H	80H	0	0	0	0	0	0	0	0	0
01H		0	0	0	0	0	0	0	0	1
02H		0	0	0	0	0	0	0	1	0
03H		0	0	0	0	0	0	0	1	1
⋮		⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
7EH		0	0	1	1	1	1	1	1	0
7FH		0	0	1	1	1	1	1	1	1
00H	81H	0	1	0	0	0	0	0	0	0
01H		0	1	0	0	0	0	0	0	1
02H		0	1	0	0	0	0	0	1	0
03H		0	1	0	0	0	0	0	1	1
⋮		⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
7EH		0	1	1	1	1	1	1	1	0
7FH		0	1	1	1	1	1	1	1	1

Sequence of setting the Display Start Line



Page Address Set (2-byte command)

This command specifies the page address which corresponds to the lower address when accessing the display data RAM from the MPU side.
It is possible to access any required bit in the display data RAM by specifying the page address and the column address. This command is a 2-byte command to be used together with the Page Address Mode Set Command and Page Address Resister Set Command. So, be sure to set the both commands continuously.

• Page Address Mode Set (Write)

When this command is input, the Page Address Mode Set Command becomes valid. Once the Page Address Mode is selected, any command other than the Page Address Resister Set Command cannot be used. This status is released when any data is stored in the register by the Page Address Resister Set Command.

A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	1	0	0	0	0

• Page Address Register Set (Write)

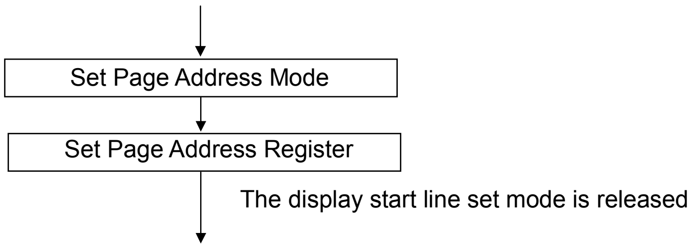
When a 5-bit data is set in the page address register by this command, the line address takes the following value. After the page address register is set by inputting this command, the display page address set mode is released.

Page address	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Page 0	0	*	*	*	0	0	0	0	0
Page 1	0	*	*	*	0	0	0	0	1
Page 3	0	*	*	*	0	0	0	1	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
Page 16	0	*	*	*	1	0	0	0	0
Page 17	0	*	*	*	1	0	0	0	1

*: Invalid data

Note: Do not specify values that do not exist as an address.

Sequence of setting the Page Address Register



Column Address Set (Write)

This command specifies the column address of the display data RAM. The column address is specified by successively writing the upper 4 bits and the lower 4 bits.

	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Upper bits	0	0	0	0	1	a7	a6	a5	a4
Lower bits	0	0	0	0	0	a3	a2	a1	a0

Column address	a7	a6	a5	a4	a3	a2	a1	a0
00H	0	0	0	0	0	0	0	0
01H	0	0	0	0	0	0	0	1
02H	0	0	0	0	0	0	1	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
B2H	1	0	1	1	0	0	1	0
B3H	1	0	1	1	0	0	1	1

Note: Do not specify values that do not exist as an address.

Display Data Write (Write)

This command writes an 8-bit data at the specified address of the display data RAM. After writing, column address or page address is automatically incremented +1 by the Display Data Input Direction Select command. This enables the MPU to write the display data continuously.

A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	Write data							

Display Data Read (Read)

This command read the 8-bit data from the specified address of the display data RAM. Since the column address is automatically incremented (by +1) after reading the data, the MPU can read successive display data from the display data RAM. Further, one dummy read operation is necessary immediately after setting the column data or page data. The display data cannot be read out when the serial interface is being used.

A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	Read data							

Display Data Input Direction Select (Write)

This command sets the direction where the display RAM address number is automatically incremented.

	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Column	0	1	0	0	0	0	1	0	0
Page	0	1	0	0	0	0	1	0	1

ADC Select (Segment driver direction select) (Write)

Using this command it is possible to reverse the relationship of correspondence between the column address of the display data RAM and the segment driver output. It is possible to reverse the sequence of the segment driver output pin by the command.

	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Forward	0	1	0	1	0	0	0	0	0
Reverse	0	1	0	1	0	0	0	0	1

n-line Inversion Drive Register Set (2-byte command)

This command sets the number of inversion lines of the liquid crystal AC drive to the register and starts line inversion drive. This command is a 2-byte command to be used together with the n-line inversion drive register mode set command and the n-line inversion drive register set command. So, be sure to set the both commands continuously.

• n-line Inversion Drive Register Mode Set (Write)

When this command is input, the n-line inversion drive register set command becomes valid.
Once the n-line inversion drive register mode is selected, any command other than the n-line inversion drive register set command cannot be used. This status is released when any data is stored in the register by the n-line inversion drive register set command.

A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	0	0	0	0

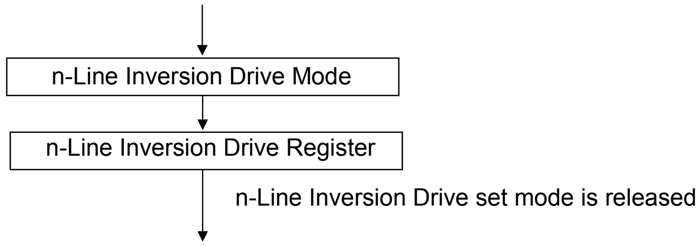
• n-line Inversion Drive Register Set (Write)

Setting of 5-bit data in the n-line inversion drive register by this command allows specification of the number of inversion lines. The n-line inversion drive register mode is released after the n-line inversion drive register is set by inputting this command.

Number of line reversal	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	*	*	*	*	0	0	0	0	0
2	*	*	*	*	0	0	0	0	1
3	*	*	*	*	0	0	0	1	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
31	*	*	*	*	1	1	1	1	0
32	*	*	*	*	1	1	1	1	1

*: Invalid data

Sequence of setting the Display Start Line



n-line Inversion Drive ON/OFF (Write)

This command provides ON/OFF control of n-line inverting drive.

	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
OFF	0	1	1	1	0	0	1	0	0
ON	0	1	1	1	0	0	1	0	1

Display Duty Set (3-byte command)

This command allows change display duty.
Setting of the start line and duty of common output allows display of arbitrary location and the number of lines. COM output only for indicators (COMS) is output always after end line output. In addition, if the built-in oscillator circuit is used, execute master clock division depending on the setting. 1/65 to 1/50 duty: No division, 1/49 to 1/34 duty: 2/3 division, 1/33 to 1/18: 1/2 division, 1/18 duty or less: 1/4 division
This command is a 3-byte command to be used in combination with the display duty mode set command, display duty register set command, start line register set command; and therefore be sure to use the three commands continuously.

• Display Duty Mode Set (Write)

When this command is input, the display duty register set command and start line register set command become valid. Once the display duty mode is selected, any command other than the display duty register set command/start line register set command cannot be used. This status is released when any data is stored in the register by the display duty register set command and start line register set command.

A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	1	1	0	1

• Display Duty Register Set (Write)

When a 6-bit data is set in the display duty register by this command, the display duty address takes the following value.

Display Duty	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1/3	0	*	*	0	0	0	0	0	*
1/4	0	*	*	0	0	0	0	1	0
1/5	0	*	*	0	0	0	0	1	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1/64	0	*	*	1	1	1	1	1	0
1/65	0	*	*	1	1	1	1	1	1

*: Invalid data

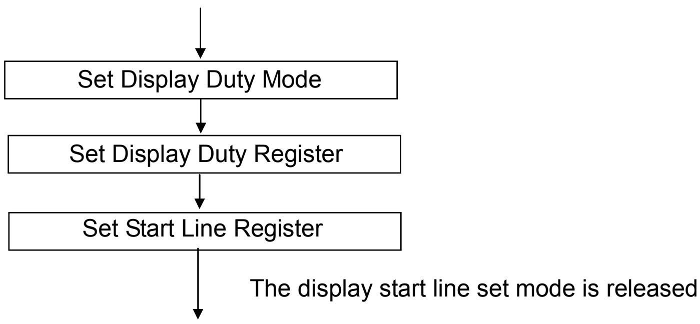
• Start Line Register Set (Write)

When a 6-bit data is set in the start line register by this command, the start line address takes the following value. When the status of common output is reversed, the commons in parentheses first will start. After the start line register is set by inputting this command, the display duty set mode is released.

Start Line	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
COM0 (COM63)	0	*	*	0	0	0	0	0	0
COM1 (COM62)	0	*	*	0	0	0	0	0	1
COM2 (COM61)	0	*	*	0	0	0	0	1	0
COM3 (COM60)	0	*	*	0	0	0	0	1	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
COM62 (COM1)	0	*	*	1	1	1	1	1	0
COM63 (COM0)	0	*	*	1	1	1	1	1	1

*: Invalid data

Sequence of setting the Display Duty Set Register



Read Modify Write (Write)

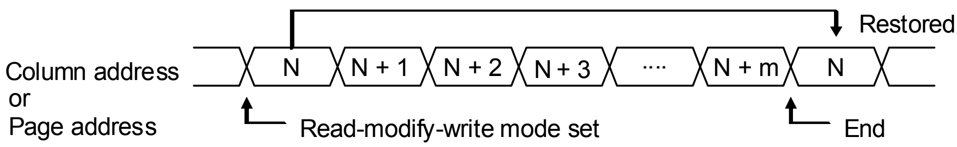
This command is used in combination with the end command. When this command is issued once, the page address and column address are not changed when the display data read command is issued, but is incremented (by +1) only when the display data write command is issued. (The incremental direction can be set by the display data input direction select command.) This condition is maintained until the end command is issued. When the end command is issued, the column address is restored to the address that was effective at the time the read modify write command was issued last. Using this function, it is possible to reduce the overhead on the MPU when repeatedly changing the data in special display area such as a blinking cursor.

A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	1	1	0	0	0	0	0

End (Write)

This command releases the read-modify-write mode and restores the page address and column address to the value at the beginning of the mode.

A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	1	1	0	1	1	1	0



Built-in Oscillator Circuit ON/OFF (Write)

This command starts the built-in oscillator circuit operation. It is enabled only in the master operation mode ($M/\overline{S}$ =HIGH) when built-in oscillator circuit is valid (CLS=HIGH).

	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
OFF	0	1	0	1	0	1	0	1	0
ON	0	1	0	1	0	1	0	1	1

Operation Clock Frequency Select (Write)

This command sets the dividing rate of the internal operation clock for the built-in oscillator frequency fosc. It is enabled only when the built-in oscillator circuit in ON. It is divided together with the display Duty set division. When the built-in oscillator circuit is OFF, the external clock f_{EXT} to be input to CL pin directly becomes the internal operation clock.

Ratio of dividing frequency	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1/4	0	0	1	1	1	0	0	0	0
1/4.5	0	0	1	1	1	0	0	0	1
1/5	0	0	1	1	1	0	0	1	0
1/5.5	0	0	1	1	1	0	0	1	1
1/6	0	0	1	1	1	0	1	0	0
1/7	0	0	1	1	1	0	1	0	1
1/8	0	0	1	1	1	0	1	1	0
1/10	0	0	1	1	1	0	1	1	1
1/12	0	0	1	1	1	1	0	0	0
1/14	0	0	1	1	1	1	0	0	1
1/16	0	0	1	1	1	1	0	1	0
1/18	0	0	1	1	1	1	0	1	1
1/20	0	0	1	1	1	1	1	0	0
1/24	0	0	1	1	1	1	1	0	1
1/28	0	0	1	1	1	1	1	1	0
1/32	0	0	1	1	1	1	1	1	1

Frame frequencies for typical numbers of display lines are listed below.

DB3	DB2	DB1	DB0	Frame Frequency [Hz]						
				65 Line	50 Line	49 Line	34 Line	33 Line	18 Line	17 Line
0	0	0	0	200	260	177	255	197	361	191
0	0	0	1	178	231	157	227	175	321	170
0	0	1	0	160	208	141	204	158	289	153
0	0	1	1	145	189	129	185	143	263	139
0	1	0	0	133	173	118	170	131	241	127
0	1	0	1	114	149	101	146	113	206	109
0	1	1	0	100	130	88	127	98	181	96
0	1	1	1	80	104	71	102	79	144	76
1	0	0	0	67	87	59	85	66	120	64
1	0	0	1	57	74	51	73	56	103	55
1	0	1	0	50	65	44	64	49	90	48
1	0	1	1	44	58	39	57	44	80	42
1	1	0	0	40	52	35	51	39	72	38
1	1	0	1	33	43	29	42	33	60	32
1	1	1	0	29	37	25	36	28	52	27
1	1	1	1	25	33	22	32	25	45	24

The table above shows the values at 25°C

The calculation formula for frame frequencies is shown below. It depends on the number of Duty sets.

Duty	LCD frame frequency (f_{FR})
1/65 to 1/50 duty	F_{OSC} /(16*n*L)
1/49 to 1/34 duty	F_{OSC} *(2/3) /(16*n*L)
1/33 to 1/18 duty	F_{OSC} *(1/2) /(16*n*L)
1/17 or less	F_{OSC} *(1/4) /(16*n*L)

Ratio of dividing frequency: n , Number of Display Line : L

Power Control Set (2-byte command)

This command set the functions of the power supply circuits. This command is a 2-byte command to be used together with the Power Control Mode Set Command and Power Control Register Set Command.

• Power Control Mode Set (Write)

When this command is issued, the power control register set command becomes effective. Once the power control mode is set, it is not possible to issue any command other than the power control register set command. This condition is released after data has been set in the register using the power control register set command.

A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	1	0	0	0

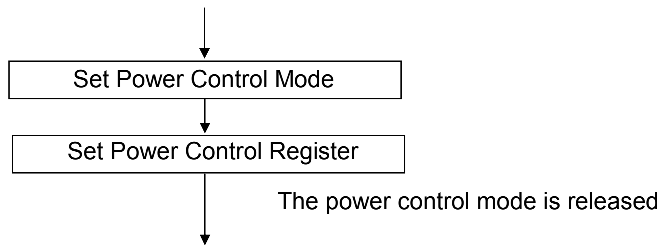
• Power Control Register Set (Write)

When a power supply circuit is set in the power control register by this command, the line address takes the following value. After the display start line is set by inputting this command, the power control set mode is released.

	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
2nd voltage multiplier circuit: OFF	0	*	*	*	*	0			
2nd voltage multiplier circuit: ON						1			
1st voltage multiplier circuit: OFF							0		
1st voltage multiplier circuit: ON							1		
Voltage adjustment circuit: OFF								0	
Voltage adjustment circuit: ON								1	
Voltage follower circuits: OFF									0
Voltage follower circuits: ON									1

*: Invalid data

Sequence of setting the Power Control Register



Voltage V1 Adjustment Internal Resistor Ratio Set

This command sets the ratios of the internal resistors for adjusting the voltage V1.

Resistor ratio	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
2.5	0	0	0	1	0	0	0	0	0
3.0	0	0	0	1	0	0	0	0	1
3.5	0	0	0	1	0	0	0	1	0
4.0	0	0	0	1	0	0	0	1	1
4.5	0	0	0	1	0	0	1	0	0
5.0	0	0	0	1	0	0	1	0	1
5.5	0	0	0	1	0	0	1	1	0
6.0	0	0	0	1	0	0	1	1	1

Note: Because this LSI has temperature gradient, V1 rises at lower temperatures. When using V1 gain of 6 times, adjust the built-in electronic potentiometer so that V1 does not exceed 18.5 V.

LCD Bias Set (2-byte command)

This command is used for selecting the bias ratio of the voltage necessary for driving the LCD device or panel. This command is a 2-byte command to be used together with the LCD Bias Set Command and LCD Bias Register Set Command.

• LCD Bias Mode Set (Write)

When this command is issued, the LCD bias register set command becomes effective. Once the LCD bias mode is set, it is not possible to issue any command other than the LCD bias register set command. This condition is released after data has been set in the register using the power LCD bias register set command.

A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0

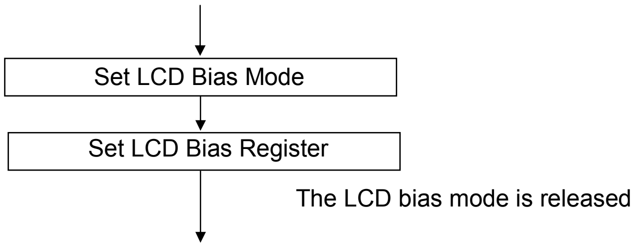
- LCD Bias Register Set (Write)

The bias ratio is set with setting of data to the LCD bias register with this command. After this command is input and the LCD bias register is set, the LCD bias mode is released.

LCD bias	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1/4 bias	0	*	*	*	*	*	0	0	0
1/5 bias	0	*	*	*	*	*	0	0	1
1/6 bias	0	*	*	*	*	*	0	1	0
1/7 bias	0	*	*	*	*	*	0	1	1
1/8 bias	0	*	*	*	*	*	1	0	0
1/9 bias	0	*	*	*	*	*	1	0	1

*: Invalid data
(1,1,0) and (1,1,1) settings are forbidden.

Sequence of setting the LCD Bias Register



Electronic Potentiometer (2-byte command)

This command is used for controlling the LCD drive voltage V1 output by the voltage adjustment circuit of the internal LCD power supply and for adjusting the intensity of the LCD display. This is a two-byte command consisting of the Electronic potentiometer mode set command and the Electronic potentiometer register set command, both of which should always be issued successively as a pair.

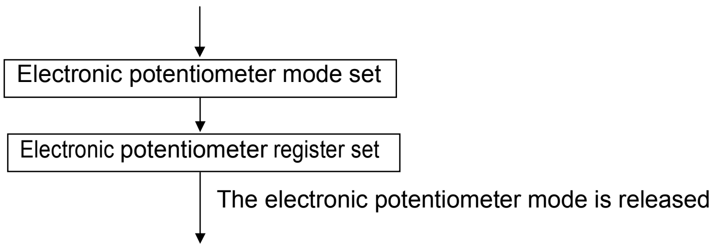
• Electronic potentiometer mode set (Write)
When this command is issued, the electronic potentiometer register set command becomes effective.
Once the electronic potentiometer mode is set, it is not possible to issue any command other than the Electronic potentiometer register set command. This condition is released after data has been set in the register using the Electronic potentiometer register set command.

A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	0	0	0	0	0	1

• Electronic potentiometer register set (Write)
By setting a 7-bit data in the electronic potentiometer register using this command, it is possible to set the LCD drive voltage V1 to one of the 128 voltage levels.
The electronic potentiometer mode is released after some data has been set in the electronic potentiometer register using this command.

α	ΔV	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
127		0	0	0	0	0	0	0	0	0
126		0	0	0	0	0	0	0	0	1
125		0	0	0	0	0	0	0	1	0
124	small	0	0	0	0	0	0	0	1	1
⋮		⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1		0	0	1	1	1	1	1	1	0
0		0	0	1	1	1	1	1	1	1
127		0	1	0	0	0	0	0	0	0
126		0	1	0	0	0	0	0	0	1
125		0	1	0	0	0	0	0	1	0
124	large	0	1	0	0	0	0	0	1	1
⋮		⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1		0	1	1	1	1	1	1	1	0
0		0	1	1	1	1	1	1	1	1

Sequence of setting the electronic potentiometer register:



Discharge ON/OFF (Write)

This command discharges the capacitors connected to the power supply circuit.

	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
OFF	0	1	1	1	0	1	0	1	0
ON	0	1	1	1	0	1	0	1	1

This command short circuits each liquid crystal potential (V1 to V5) and Vss. When voltage is supplied to each liquid crystal drive potential externally, be sure to turn off the external power before executing this command.

Power Save ON/OFF (Write)

This command establishes the power save mode, thereby ensuring a substantial reduction of current consumption.

	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
OFF	0	1	0	1	0	1	0	0	0
ON	0	1	0	1	0	1	0	0	1

In the power save status, the display data and operation status before power save activation are held, and the display data RAM can be accessed from MPU.

The power save OFF command is to release the power save status, and it returns to the status before the power save activation. If built-in power supply is used, it is turned on after the power save OFF command execution, and after a fixed time period for stabilization of the output voltage, the display operation is started.

The internal conditions in the power save mode are as follows:

(1) Stop of internal oscillator circuit.
(2) Stop of LCD power supply circuit.
(3) Stop of liquid crystal drive circuit (VSS level output is issued as the segment and common driver output).
(4) Operation of VCH generation circuit and temperature sensor circuit.

Temperature Gradient Set

This command sets the temperature gradient characteristics of the liquid crystal drive voltage output from the built-in power supply circuit from eight states to one state. The temperature gradient of the liquid crystal drive voltage can be set according to the liquid crystal temperature gradient to be used.

Temperature gradient [%/°C]	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0.00	0	0	1	0	0	1	0	0	0
-0.03	0	0	1	0	0	1	0	0	1
-0.06	0	0	1	0	0	1	0	1	0
-0.08	0	0	1	0	0	1	0	1	1
-0.10	0	0	1	0	0	1	1	0	0
-0.13	0	0	1	0	0	1	1	0	1
-0.15	0	0	1	0	0	1	1	1	0
-0.18	0	0	1	0	0	1	1	1	1

Status Read (Read)

This command reads out the temperature gradient select bit set on the register.

A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	*	*	*	*	*	T1	T2	T3

*: Invalid data

Reset (Write)

This command initializes the display start line number, column address, page address, common output state, voltage V1 adjustment internal resistor ratio and the electronic potentiometer function, and also releases the read-modify-write mode or the test mode. This command does not affect the contents of the display data RAM.
The reset operation is made after issuing the reset command.
The initialization after switching on the power is carried out by the reset signal input to the $\overline{\text{RES}}$ pin.

A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	1	1	0	0	0	1	0

Temperature Sensor ON/OFF (Write)

ON/OFF of a temperature sensor is specified with this command.

	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
OFF	0	0	1	1	0	1	0	0	0
ON	0	0	1	1	0	1	0	0	1

The temperature sensor circuit is controlled independently from Power Save Command.

Common Output Direction Select (Write)

This command sets the direction of the common output pin.

Direction	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Normal Type	0	1	1	0	0	0	1	0	0
Comb Type	0	1	1	0	0	0	1	0	1

Normal Type: COM0→COM1→ …. →COM63
Comb Type: COM0→COM32→COM1→COM33→ …. →COM31→COM63

Multiplier Clock Frequency Select (2-byte command)

This command selects the multiplier clock frequency of the 1st and 2nd voltage multiplier circuits. This command is a 2-byte command to be used together with the multiplier clock frequency select mode set command and the multiplier clock frequency select register set command. So, be sure to set the both commands continuously.

• Multiplier Clock Frequency Select mode set (Write)

When this command is input, the multiplier clock frequency select register set command becomes valid. Once the multiplier clock frequency select mode is selected, any command other than the multiplier clock frequency select register set command cannot be used. This status is released when any data is stored in the register by the multiplier clock frequency select register set command.

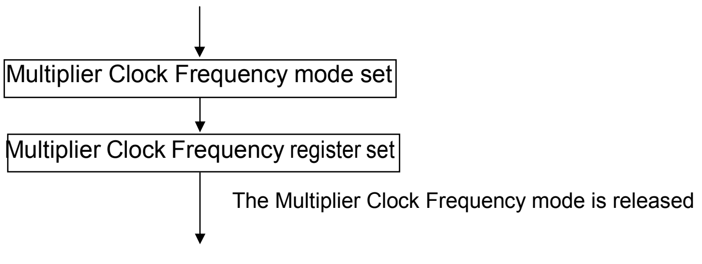
A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1

• Multiplier Clock Frequency register set (Write)

Setting of data in the multiplier clock frequency select register by this command allows specification of the multiplier clock frequency. The multiplier clock frequency select mode is released when the multiplier clock frequency select register is set by inputting this command.

Frequency		A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Internal Clock	External Clock									
fOSC/64	fEXT/8	0	0	0	0	0	0	0	0	0
fOSC/32	fEXT/4	0	0	0	0	0	0	0	0	1
fOSC/16	fEXT/2	0	0	0	0	0	0	0	1	*

Sequence of setting the multiplier clock frequency register:



NOP (Write)

This is a No Operation command.

A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	1	1	0	0	0	1	1

Initialized Condition Using the $\overline{RES}$ pin

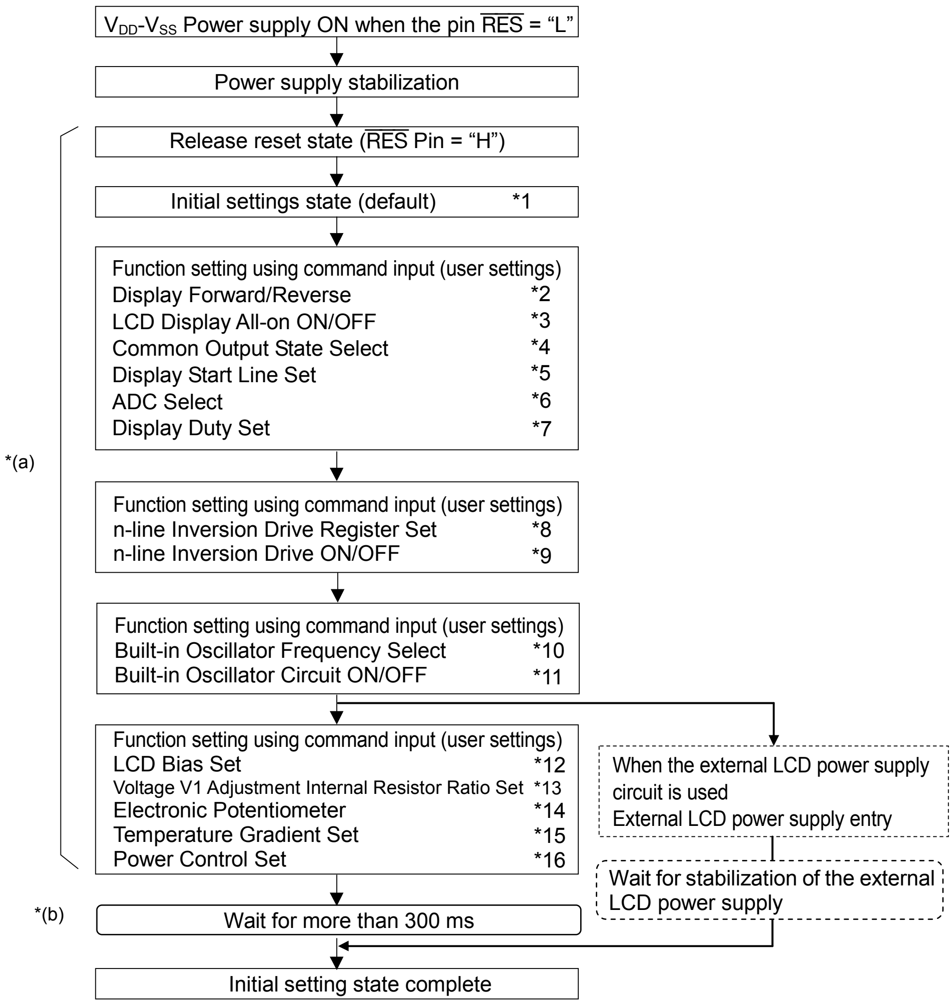
This LSI goes into the initialized condition when the $\overline{RES}$ input goes to the "L" level. The initialized condition consists of the following conditions.

(1) Display OFF
(2) Forward display mode
(3) All-on display off
(4) Common output state: Forward
(5) Display start line: Set to 1st line, Indicator address: Set to 80H
(6) Page address: Set to 0 page
(7) Column address: Set to 0 address
(8) Display data input direction: Column direction
(9) ADC select: Incremented (ADC command DB0 = "L")
(10) n-line inversion drive: OFF
(11) n-line reversal number register: (DB4, DB3, DB2, DB1, DB0) = (1, 0, 0, 0, 0)
(12) Display duty set: 1/65Duty, Start Line COM0
(13) Read-modify-write: OFF
(14) Built-in oscillation circuit: OFF
(15) Oscillation frequency register: (DB4, DB3, DB2, DB1, DB0) = (0, 0, 0, 0)
(16) Power control register: (DB4, DB3, DB2, DB1, DB0) = (0, 0, 0, 0)
(17) Voltage V1 adjustment internal resistor ratio register: (DB2, DB1, DB0) = (1, 0, 0)
(18) LCD Power supply bias ratio: 1/9 bias
(19) The electronic potentiometer register set mode is released.
Electronic potentiometer register: (DB5, DB4, DB3, DB2, DB1, DB0) = (1, 0, 0, 0, 0, 0)
(20) Discharge: OFF
(21) Power save: OFF
(22) Temperature gradient resistor: (DB2, DB1, DB0) = (0, 0, 0) (0.00%/°C)
(23) Register data in the serial interface: Clear
(24) Temperature sensor: OFF
(25) Common Output Direction: Normal
(26) Multiplier Clock Frequency: (DB1, DB0)=(0,0)

On the other hand, when the reset command is used, only the conditions (6) to (7), (13) above are set. As is shown in the "MPU Interface (example for reference)", the $\overline{RES}$ pin is connected to the Reset pin of the MPU and the initialization of this LSI is made simultaneously with the resetting of the MPU. This LSI always has to be reset using the $\overline{RES}$ pin at the time the power is switched ON. Also, excessive current can flow through this LSI when the control signal from the MPU is in the high impedance state. It is necessary to take measures to ensure that the input pins of this LSI do not go into the high impedance state after the power has been switched ON.

EXAMPLES OF SETTINGS FOR THE INSTRUCTIONS

Initial setup



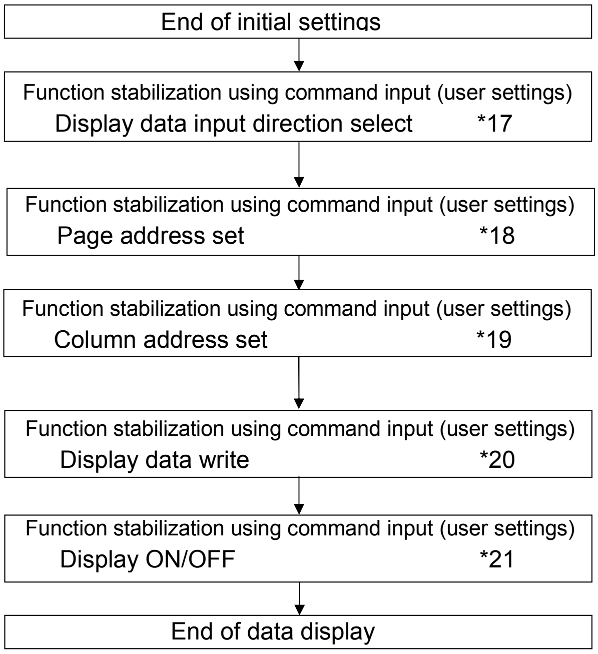
*(a): Carry out power control set within 5ms after releasing the reset state.
The 5ms duration changes depending on the panel characteristics and the value of the smoothing capacitor. We recommend verification of operation using an actual unit.

*(b): When trace resistance in COG mounting does not exist, wait for over 300 ms.
Since this value varies with trace resistance, V1, smoothing capacitors, or voltage multiplier capacitors in COG mounting, confirm operation on an actual circuit board when using this LSI.

Notes: Sections to be referred to
- *1: Functional description "Reset circuit"
- *2: Description of operation "Forward/Reverse Display Mode"
- *3: Description of operation "LCD Display All-on ON/OFF"
- *4: Description of operation "Common Output Status Select"
- *5: Description of operation "Display Start Line Set"
- *6: Description of operation "ADC Select"
- *7: Description of operation "Display Duty Set"
- *8: Description of operation "n-line Inversion Drive Register Set"

*9: Description of operation “n-line Inversion Drive ON/OFF”
*10: Description of operation “Built-in Oscillator Frequency Select”
*11: Description of operation “Built-in Oscillator Circuit ON/OFF”
*12: Description of operation “LCD Bias Set”
*13: Functional description “Power supply circuit”,
Operation description “Voltage V1 adjustment internal resistor ratio set”
*14: Functional description “Power supply circuit”,
Operation description “Electronic Potentiometer”
*15: Operation description “Temperature Gradient Set”
*16: Functional description “Power supply circuit”,
Operation description “Power Control set”

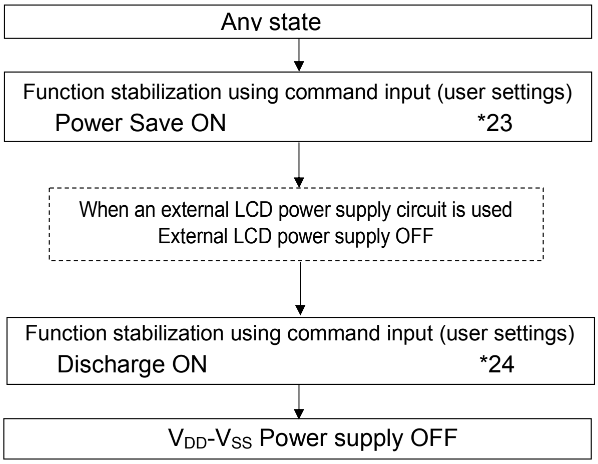
Data Display



Notes: Sections to be referred to

- *17: Description of operation “Display Data Input direction Select”
- *18: Description of operation “Page Address Set”
- *19: Description of operation “Column Address Set”
- *20: Description of operation “Display Data Write”
- *21: Description of operation “Display ON/OFF”

Power Supply OFF (*22)



Notes: Sections to be referred to

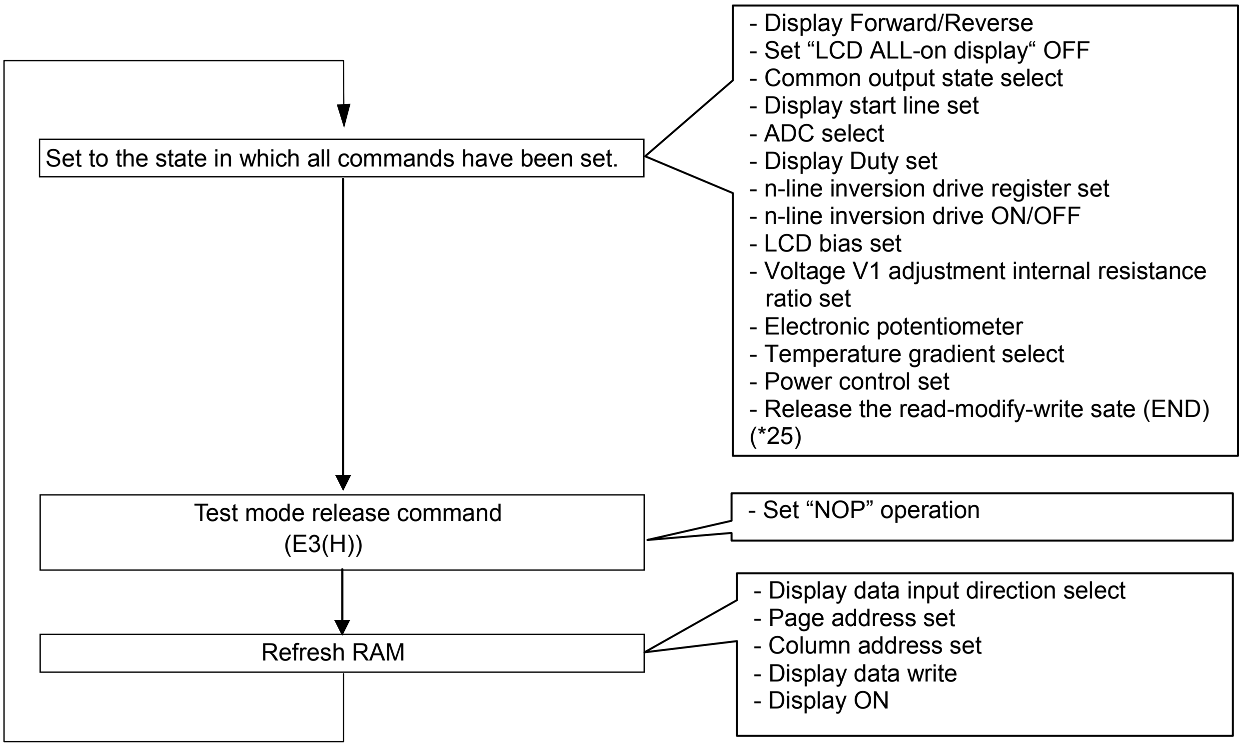
*22: The power supply of this LSI is switched OFF after switching OFF the internal power supply. Function description "Power supply circuit"
If the power supply of this LSI is switched OFF when the internal power supply is still ON, since the state of supplying power to the built-in LCD drive circuits continues for a short duration, it may affect the display quality of the LCD panel. Always follow the power supply switching OFF sequence.

*23: Description of operation "Power Save"

*24: Description of operation "Discharge"

Refresh

Although the ML9445 holds operation state by commands, excessive external noise might change the internal state.
On a chip-mounting and system level, it is necessary to take countermeasures against preventing noise from occurring. It is recommended to use the refresh sequence periodically to control sudden noise.

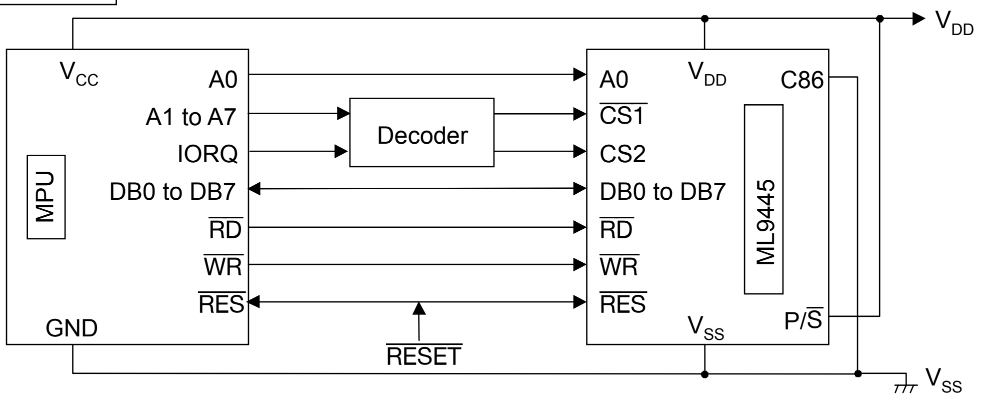


*25: Regardless of presence of setting of "Read-modify-write" command, please carry out "END" command.

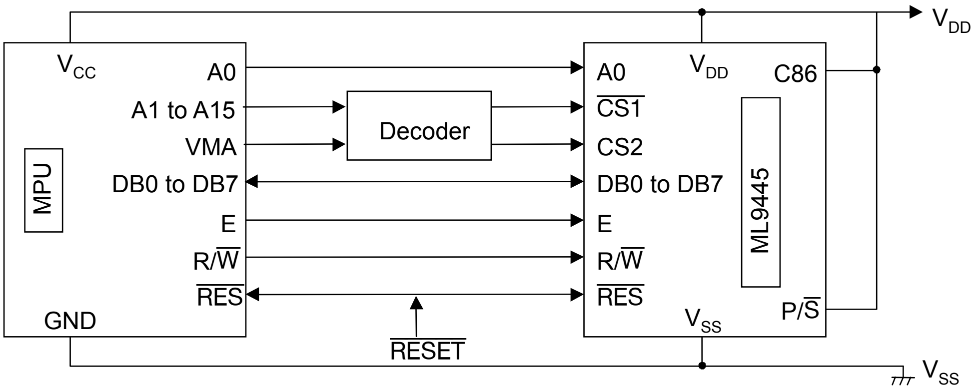
MPU INTERFACE

The ML9445 series ICs can be connected directly to the 80-series and 68-series MPUs.
Further, by using the serial interface, it is possible to operate the LSI with a minimum number of signal lines.
In addition, it is possible to expand the display area by using the ML9445 series LSIs in a multiple chip configuration. In this case, it is possible to select the individual LSI to be accessed using the chip select signals.

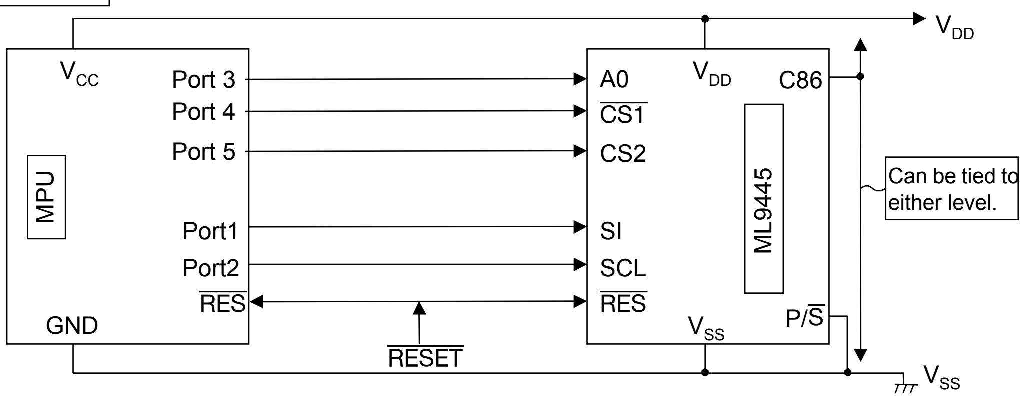
• 80-Series MPU



• 68-Series MPU



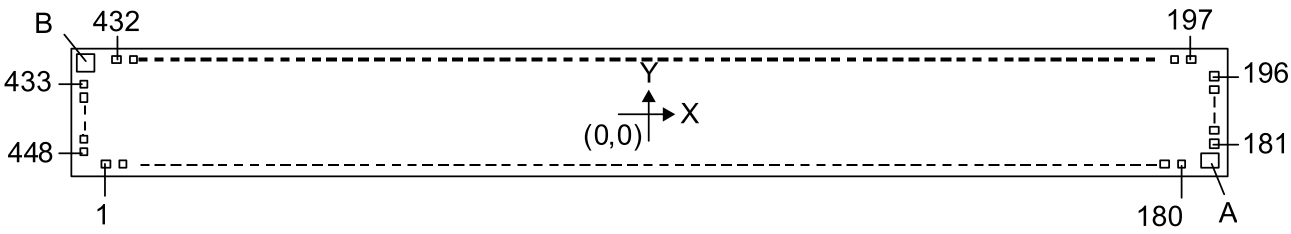
• Serial interface



PAD CONFIGURATION（ML9445）

Pad layout

Chip size　: 12.7 x 1.26 mm
Chip thickness : 400µm ±20µm

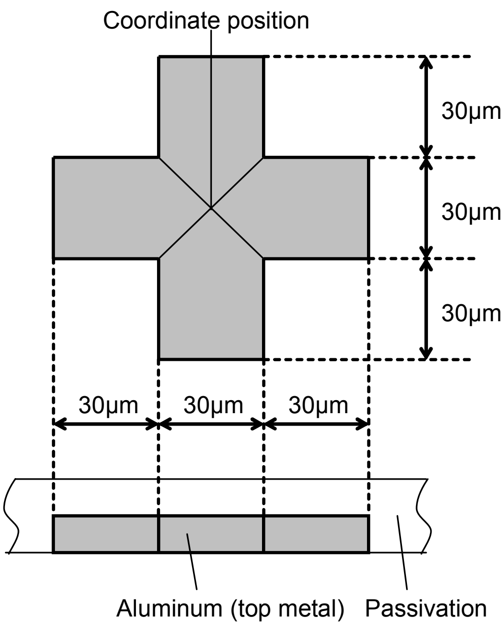


Bump and alignment mark dimensions (pattern face)

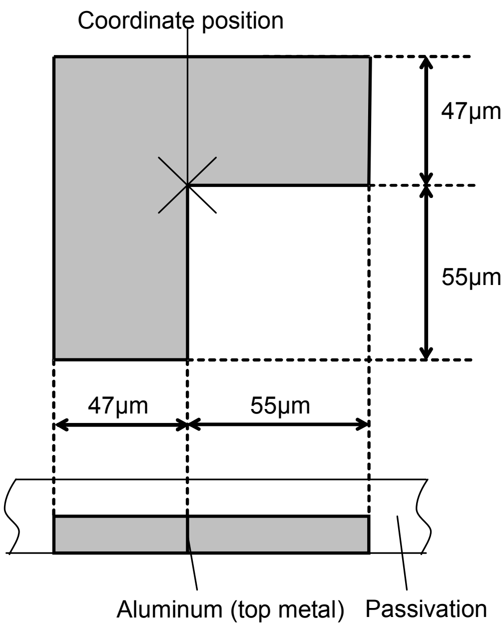
PAD No.1～180　: 35 µm×72 µm
PAD No.181～196　: 84 µm×30µm
PAD No.197～432　: 30 µm×84 µm
PAD No.433～448　: 84 µm×30 µm

Alignment marks A and B　: See below

[Mark A]



[Mark B]



Alignment marks	X-coordinate (µm)	Y-coordinate (µm)
Mark A	6215	-488
Mark B	-6228	508

Pad center coordinates

Pad number	Pad name	X-coordinate (µm)	Y-coordinate (µm)
1	DUMMY	-6059	-488
2	TEST1	-5979	-488
3	TEST1	-5919	-488
4	V_{SS}	-5839	-488
5	SDAACK	-5759	-488
6	SDAACK	-5699	-488
7	SYNC	-5619	-488
8	SYNC	-5559	-488
9	FR	-5479	-488
10	FR	-5419	-488
11	CL	-5339	-488
12	CL	-5279	-488
13	$\overline{DOF}$	-5199	-488
14	$\overline{DOF}$	-5139	-488
15	$\overline{CS1}$	-5059	-488
16	$\overline{CS1}$	-4999	-488
17	CS2	-4919	-488
18	CS2	-4859	-488
19	$\overline{RES}$	-4779	-488
20	$\overline{RES}$	-4719	-488
21	A0	-4639	-488
22	A0	-4579	-488
23	V_{SS}	-4499	-488
24	$\overline{WR}$	-4419	-488
25	$\overline{WR}$	-4359	-488
26	$\overline{RD}$	-4279	-488
27	$\overline{RD}$	-4219	-488
28	V_{DD}	-4139	-488
29	DB0	-4059	-488
30	DB0	-3999	-488
31	DB1	-3919	-488
32	DB1	-3859	-488
33	DB2	-3779	-488
34	DB2	-3719	-488
35	DB3	-3639	-488
36	DB3	-3579	-488
37	DB4	-3499	-488
38	DB4	-3439	-488
39	DB5	-3359	-488
40	DB5	-3299	-488

Pad number	Pad name	X-coordinate (µm)	Y-coordinate (µm)
41	DB6	-3193	-488
42	DB6	-3133	-488
43	DB7	-3001	-488
44	DB7	-2941	-488
45	VCH	-2838	-488
46	VCH	-2778	-488
47	VCH	-2718	-488
48	SVD2	-2615	-488
49	SVD2	-2555	-488
50	TEST2	-2475	-488
51	TEST2	-2415	-488
52	V_{DD}	-2335	-488
53	$M/\overline{S}$	-2255	-488
54	$M/\overline{S}$	-2195	-488
55	CLS	-2115	-488
56	CLS	-2055	-488
57	C86	-1975	-488
58	C86	-1915	-488
59	$P/\overline{S}$	-1835	-488
60	$P/\overline{S}$	-1775	-488
61	IRS	-1695	-488
62	IRS	-1635	-488
63	TEST3	-1555	-488
64	TEST3	-1495	-488
65	V_{SS}	-1391	-488
66	V_{SS}	-1331	-488
67	V_{SS}	-1271	-488
68	V_{SS}	-1211	-488
69	V_{SS}	-1151	-488
70	V_{SS}	-1091	-488
71	V_{SS}	-1031	-488
72	V_{SS}	-971	-488
73	V_{SS}	-911	-488
74	V_{SS}	-851	-488
75	V_{DD}	-771	-488
76	V_{DD}	-711	-488
77	V_{DD}	-651	-488
78	V_{DD}	-591	-488
79	V_{DD}	-531	-488
80	V_{DD}	-471	-488

Pad number	Pad name	X-coordinate (μm)	Y-coordinate (μm)
81	V_{DD}	-411	-488
82	V_{DD}	-351	-488
83	V_{IN}	-271	-488
84	V_{IN}	-211	-488
85	V_{IN}	-151	-488
86	V_{IN}	-91	-488
87	V_{IN}	-31	-488
88	V_{IN}	29	-488
89	V_{IN}	89	-488
90	V_{IN}	149	-488
91	DUMMY	229	-488
92	VC3+	309	-488
93	VC3+	369	-488
94	VC3+	429	-488
95	VC3+	489	-488
96	VC3+	549	-488
97	VC5+	629	-488
98	VC5+	689	-488
99	VC5+	749	-488
100	VC5+	809	-488
101	VC5+	869	-488
102	VS1-	949	-488
103	VS1-	1009	-488
104	VS1-	1069	-488
105	VS1-	1129	-488
106	VS1-	1189	-488
107	VS1-	1249	-488
108	VS1-	1309	-488
109	VC2+	1389	-488
110	VC2+	1449	-488
111	VC2+	1509	-488
112	VC2+	1569	-488
113	VC2+	1629	-488
114	VC4+	1709	-488
115	VC4+	1769	-488
116	VC4+	1829	-488
117	VC4+	1889	-488
118	VC4+	1949	-488
119	VS2-	2029	-488
120	VS2-	2089	-488
121	VS2-	2149	-488
122	VS2-	2209	-488
123	VS2-	2269	-488
124	VS2-	2329	-488
125	VS2-	2389	-488

Pad number	Pad name	X-coordinate (μm)	Y-coordinate (μm)
126	VC6+	2469	-488
127	VC6+	2529	-488
128	VC6+	2589	-488
129	VC6+	2649	-488
130	VC6+	2709	-488
131	V_{OUT1}	2789	-488
132	V_{OUT1}	2849	-488
133	V_{OUT1}	2909	-488
134	V_{OUT1}	2969	-488
135	DUMMY	3049	-488
136	DUMMY	3109	-488
137	V_H	3189	-488
138	V_H	3249	-488
139	V_H	3309	-488
140	V_H	3369	-488
141	VS3-	3449	-488
142	VS3-	3509	-488
143	VS3-	3569	-488
144	VS3-	3629	-488
145	VC7+	3709	-488
146	VC7+	3769	-488
147	VC7+	3829	-488
148	VC7+	3889	-488
149	V_{OUT2}	3969	-488
150	V_{OUT2}	4029	-488
151	V_{OUT2}	4089	-488
152	DUMMY	4169	-488
153	DUMMY	4229	-488
154	VR	4309	-488
155	VR	4369	-488
156	V_{RS}	4449	-488
157	V_{RS}	4509	-488
158	DUMMY	4589	-488
159	V1	4669	-488
160	V1	4729	-488
161	V1	4789	-488
162	V1	4849	-488
163	V2	4929	-488
164	V2	4989	-488
165	V2	5049	-488
166	V2	5109	-488
167	V3	5189	-488
168	V3	5249	-488
169	V3	5309	-488
170	V3	5369	-488

Pad number	Pad name	X-coordinate (µm)	Y-coordinate (µm)	Pad number	Pad name	X-coordinate (µm)	Y-coordinate (µm)
171	V4	5449	-488	216	COM7	5075	495
172	V4	5509	-488	217	COM6	5025	495
173	V4	5569	-488	218	COM5	4975	495
174	V4	5629	-488	219	COM4	4925	495
175	V5	5709	-488	220	COM3	4875	495
176	V5	5769	-488	221	COM2	4825	495
177	V5	5829	-488	222	COM1	4775	495
178	V5	5889	-488	223	COM0	4725	495
179	DUMMY	5969	-488	224	COMS0	4675	495
180	DUMMY	6049	-488	225	SEG0	4475	495
181	DUMMY	6215	-390	226	SEG1	4425	495
182	DUMMY	6215	-340	227	SEG2	4375	495
183	COM31	6215	-290	228	SEG3	4325	495
184	COM30	6215	-240	229	SEG4	4275	495
185	COM29	6215	-190	230	SEG5	4225	495
186	COM28	6215	-140	231	SEG6	4175	495
187	COM27	6215	-90	232	SEG7	4125	495
188	COM26	6215	-40	233	SEG8	4075	495
189	COM25	6215	10	234	SEG9	4025	495
190	COM24	6215	60	235	SEG10	3975	495
191	COM23	6215	110	236	SEG11	3925	495
192	COM22	6215	160	237	SEG12	3875	495
193	COM21	6215	210	238	SEG13	3825	495
194	DUMMY	6215	260	239	SEG14	3775	495
195	DUMMY	6215	310	240	SEG15	3725	495
196	DUMMY	6215	360	241	SEG16	3675	495
197	DUMMY	6025	495	242	SEG17	3625	495
198	DUMMY	5975	495	243	SEG18	3575	495
199	DUMMY	5925	495	244	SEG19	3525	495
200	DUMMY	5875	495	245	SEG20	3475	495
201	DUMMY	5825	495	246	SEG21	3425	495
202	DUMMY	5775	495	247	SEG22	3375	495
203	COM20	5725	495	248	SEG23	3325	495
204	COM19	5675	495	249	SEG24	3275	495
205	COM18	5625	495	250	SEG25	3225	495
206	COM17	5575	495	251	SEG26	3175	495
207	COM16	5525	495	252	SEG27	3125	495
208	COM15	5475	495	253	SEG28	3075	495
209	COM14	5425	495	254	SEG29	3025	495
210	COM13	5375	495	255	SEG30	2975	495
211	COM12	5325	495	256	SEG31	2925	495
212	COM11	5275	495	257	SEG32	2875	495
213	COM10	5225	495	258	SEG33	2825	495
214	COM9	5175	495	259	SEG34	2775	495
215	COM8	5125	495	260	SEG35	2725	495

Pad number	Pad name	X-coordinate (μm)	Y-coordinate (μm)	Pad number	Pad name	X-coordinate (μm)	Y-coordinate (μm)
261	SEG36	2675	495	306	SEG81	425	495
262	SEG37	2625	495	307	SEG82	375	495
263	SEG38	2575	495	308	SEG83	325	495
264	SEG39	2525	495	309	SEG84	275	495
265	SEG40	2475	495	310	SEG85	225	495
266	SEG41	2425	495	311	SEG86	175	495
267	SEG42	2375	495	312	SEG87	125	495
268	SEG43	2325	495	313	SEG88	75	495
269	SEG44	2275	495	314	SEG89	25	495
270	SEG45	2225	495	315	SEG90	-25	495
271	SEG46	2175	495	316	SEG91	-75	495
272	SEG47	2125	495	317	SEG92	-125	495
273	SEG48	2075	495	318	SEG93	-175	495
274	SEG49	2025	495	319	SEG94	-225	495
275	SEG50	1975	495	320	SEG95	-275	495
276	SEG51	1925	495	321	SEG96	-325	495
277	SEG52	1875	495	322	SEG97	-375	495
278	SEG53	1825	495	323	SEG98	-425	495
279	SEG54	1775	495	324	SEG99	-475	495
280	SEG55	1725	495	325	SEG100	-525	495
281	SEG56	1675	495	326	SEG101	-575	495
282	SEG57	1625	495	327	SEG102	-625	495
283	SEG58	1575	495	328	SEG103	-675	495
284	SEG59	1525	495	329	SEG104	-725	495
285	SEG60	1475	495	330	SEG105	-775	495
286	SEG61	1425	495	331	SEG106	-825	495
287	SEG62	1375	495	332	SEG107	-875	495
288	SEG63	1325	495	333	SEG108	-925	495
289	SEG64	1275	495	334	SEG109	-975	495
290	SEG65	1225	495	335	SEG110	-1025	495
291	SEG66	1175	495	336	SEG111	-1075	495
292	SEG67	1125	495	337	SEG112	-1125	495
293	SEG68	1075	495	338	SEG113	-1175	495
294	SEG69	1025	495	339	SEG114	-1225	495
295	SEG70	975	495	340	SEG115	-1275	495
296	SEG71	925	495	341	SEG116	-1325	495
297	SEG72	875	495	342	SEG117	-1375	495
298	SEG73	825	495	343	SEG118	-1425	495
299	SEG74	775	495	344	SEG119	-1475	495
300	SEG75	725	495	345	SEG120	-1525	495
301	SEG76	675	495	346	SEG121	-1575	495
302	SEG77	625	495	347	SEG122	-1625	495
303	SEG78	575	495	348	SEG123	-1675	495
304	SEG79	525	495	349	SEG124	-1725	495
305	SEG80	475	495	350	SEG125	-1775	495

Pad number	Pad name	X-coordinate (µm)	Y-coordinate (µm)
351	SEG126	-1825	495
352	SEG127	-1875	495
353	SEG128	-1925	495
354	SEG129	-1975	495
355	SEG130	-2025	495
356	SEG131	-2075	495
357	SEG132	-2125	495
358	SEG133	-2175	495
359	SEG134	-2225	495
360	SEG135	-2275	495
361	SEG136	-2325	495
362	SEG137	-2375	495
363	SEG138	-2425	495
364	SEG139	-2475	495
365	SEG140	-2525	495
366	SEG141	-2575	495
367	SEG142	-2625	495
368	SEG143	-2675	495
369	SEG144	-2725	495
370	SEG145	-2775	495
371	SEG146	-2825	495
372	SEG147	-2875	495
373	SEG148	-2925	495
374	SEG149	-2975	495
375	SEG150	-3025	495
376	SEG151	-3075	495
377	SEG152	-3125	495
378	SEG153	-3175	495
379	SEG154	-3225	495
380	SEG155	-3275	495
381	SEG156	-3325	495
382	SEG157	-3375	495
383	SEG158	-3425	495
384	SEG159	-3475	495
385	SEG160	-3525	495
386	SEG161	-3575	495
387	SEG162	-3625	495
388	SEG163	-3675	495
389	SEG164	-3725	495
390	SEG165	-3775	495
391	SEG166	-3825	495
392	SEG167	-3875	495
393	SEG168	-3925	495
394	SEG169	-3975	495
395	SEG170	-4025	495

Pad number	Pad name	X-coordinate (µm)	Y-coordinate (µm)
396	SEG171	-4075	495
397	SEG172	-4125	495
398	SEG173	-4175	495
399	SEG174	-4225	495
400	SEG175	-4275	495
401	SEG176	-4325	495
402	SEG177	-4375	495
403	SEG178	-4425	495
404	SEG179	-4475	495
405	COM32	-4675	495
406	COM33	-4725	495
407	COM34	-4775	495
408	COM35	-4825	495
409	COM36	-4875	495
410	COM37	-4925	495
411	COM38	-4975	495
412	COM39	-5025	495
413	COM40	-5075	495
414	COM41	-5125	495
415	COM42	-5175	495
416	COM43	-5225	495
417	COM44	-5275	495
418	COM45	-5325	495
419	COM46	-5375	495
420	COM47	-5425	495
421	COM48	-5475	495
422	COM49	-5525	495
423	COM50	-5575	495
424	COM51	-5625	495
425	COM52	-5675	495
426	COM53	-5725	495
427	DUMMY	-5775	495
428	DUMMY	-5825	495
429	DUMMY	-5875	495
430	DUMMY	-5925	495
431	DUMMY	-5975	495
432	DUMMY	-6025	495
433	DUMMY	-6215	360
434	DUMMY	-6215	310
435	DUMMY	-6215	260
436	COM54	-6215	210
437	COM55	-6215	160
438	COM56	-6215	110
439	COM57	-6215	60
440	COM58	-6215	10

Pad number	Pad name	X-coordinate (μm)	Y-coordinate (μm)	Pad number	Pad name	X-coordinate (μm)	Y-coordinate (μm)
441	COM59	-6215	-40				
442	COM60	-6215	-90				
443	COM61	-6215	-140				
444	COM62	-6215	-190				
445	COM63	-6215	-240				
446	COMS1	-6215	-290				
447	DUMMY	-6215	-340				
448	DUMMY	-6215	-390				

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL9445-01	Apr 27, 2012	–	–	Final edition 1
PEDL9445-02	Dec 20 ,2013	3	3	Add V1 (V_{BI})
		5	5	Add explanation of *6
		19	19	V_{RS} test pins →output pins
		33	33 to 35	Add explanation of power supply circuit
		34	36 to 37	Add explanation of 1st voltage multiplier circuits
		35	38	Add explanation of 2nd voltage multiplier circuits
		41 to 42	44 to 49	Add explanation of application circuits
		-	50	Add cascade connection example

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