1 INTRODUCTION

1.1 SUMMARY

The Rockwell RC96DPL/RC144DPL and RC96DPi/RC144DPi modems are high speed modem data pump families that support data rates up to 9600 or 14400 bps, fax operation up to 9600 or 14400 bps, and ADPCM voice coder/decoder, depending upon the model. The following models are available:

Model	Data	Fax	Voice
RC96DPL-D/RC96DPi-D	9.6 kbps	None	No
RC96DPL/RC96DPi	9.6 kbps	9.6 kbps	No
RCV96DPL/RCV96DPi	9.6 kbps	9.6 kbps	Yes
RC144DPL-D/RC144DPi-D	14.4 kbps	None	No
RC144DPL/RC144DPi	14.4 kbps	14.4 kbps	No
RCV144DPL/RCV144DPi	14.4 kbps	14.4 kbps	Yes

The RC96DPL/RC144DPL models are identical in operation to the corresponding RC96DPi/RC144DPi models, however, the RC96DPL/RC144DPL models consume less power and are also available in PQFP packages. All references to RC96DPL/RC144DPL or modem in this manual also apply to the RC96DPi/RC144DPi except as noted.

As a data modem, the modem can operate in 2-wire, full-duplex, synchronous/asynchronous modes at 14400 (RC144DPL family), 12000 (RC144DPL family), 9600, 7200, 4800, 2400, 1200, 600, 300, or 75 bps. Automode operates in accordance with EIA/TIA PN-2330 (Draft).

Internal HDLC support eliminates the need for an external serial input/output (SIO) device in the DTE for products incorporating error correction and T.30 protocols.

A 150 bps in-band secondary channel can operate concurrently with V.32 bis/V.32, allowing easy implementation of supporting applications such as network management.

Facsimile models fully support Group 3 send and receive.

The RCV96DPL and RCV144DPL models include a voice pass-through mode which allows the host to transmit and receive uncompressed audio signals. These models also include an Adaptive Differential Pulse Code Modulation (ADPCM) voice coder and decoder (codec). The full-duplex codec compresses and decompresses voice signals to allow efficient digital storage of voice messages. The codec operates at 28.8k, 21.6k, or 14.4k bps (4-bit, 3-bit, or 2-bit quantization, respectively) with a default 7.2 kHz programmable sample rate. Optional coder silence detection/deletion and decoder silence interpolation are included to achieve greater compression rates.

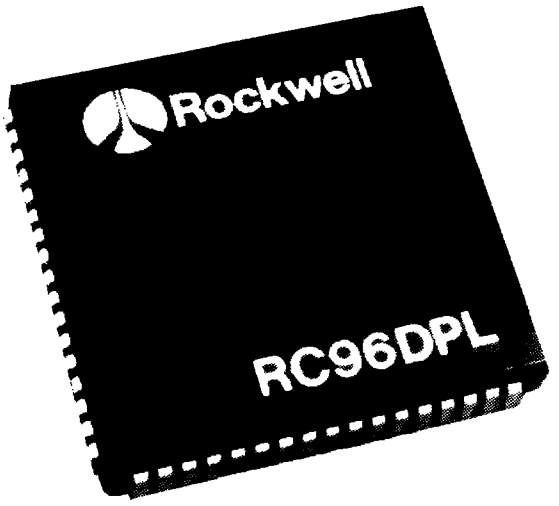
The RC96DPL-D and RC144DPL-D modem data pumps are identical to the the RC96DPL and RC144DPL models, respectively, except the fax modes are not supported.

The modem operates over the public switched telephone network (PSTN) through the appropriate line termination.

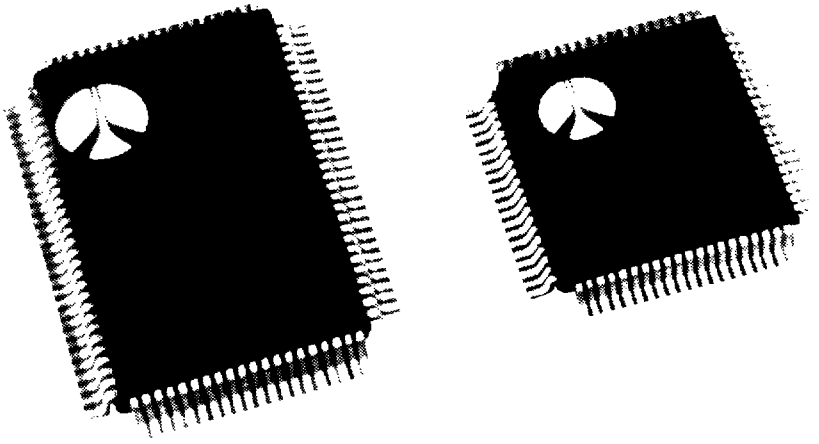
The RC96DPL/RC144DPL and RC96DPi/RC144DPi models are available in a single 68-pin plastic leaded chip carrier (PLCC). The RC96DPL/RC144DPL (not the RC96DPi/RC144DPi) is also available in two low-profile plastic quad flat packs (PQFPs).

1.2 FEATURES

- 2-wire full-duplex
  - — V.32 bis (RC144DPL family), V.32, V.22 bis, V.22, V.23, and V.21; Bell 212A and 103
- 2-wire half-duplex
  - —V.17 (RC144DPL and RCV144DPL), V.29, V.27 ter, V.26 bis, V.26 Alternative A, and V.21 channel 2
  - —Short train option in V.17 and V.27 ter
- Group 3 fax transmission/reception at 14400, 12000, 9600, 7200, 4800, or 2400 bps (model dependent)
- Serial synchronous and asynchronous data
- Parallel synchronous and asynchronous data
- Parallel synchronous SDLC/HDLC support
- In-band secondary channel
- Digital near and far end echo cancellation
- Bulk delay for satellite transmission
- Auto-dial and auto-answer
- TTL and CMOS compatible DTE interface
  - —CCITT V.24 (EIA/RS-232-D) (data/control)
  - —Microprocessor bus (data/configuration/control)
- Internal hybrid
- Dynamic range: –43 dBm to –9 dBm
- Compromise and automatic adaptive equalizers
- Voice pass-through mode (RCV96DPL/RCV144DPL)
- ADPCM voice mode (RCV96DPL/RCV144DPL)
- Adjustable speaker output to monitor received signal
- DTMF detection
- DMA support interrupt lines
- Two 8-byte FIFO data buffers for burst data transfer
- NRZI encoding/decoding
- Automatic mode selection
- 511 pattern generation/detection
- Diagnostic capability
- V.13 signalling
- V.54 inter-DCE signalling
- V.54 local analog and remote digital loopback
- Single +5VDC supply
  - —Normal mode:
    RC96DPL/RC144DPL: 390 mW (typical)
    RC96DPi/RC144DPi: 700 mW (typical)
  - —Sleep mode: 10 mW (typical)
- PLCC or PQFP packages
  - —Single 68-pin PLCC package [RC96DPL/RC144DPL and RC96DPi/RC144DPi]
  - — Two PQFPs (80 pin and 100 pin) [RC96DPL/RC144DPL only, not RC96DPi/RC144DPi)



a. Single 68-Pin PLCC



b. 100-Pin PQFP and 80-Pin PQFP

Figure 1-1. RC96DPL Modem Data Pump

1.3 TECHNICAL SPECIFICATIONS

Configurations and Rates

The selectable modem configurations, signaling rates, and data rates, are listed in Table 1-1.

Tone Generation

The modem can generate single or dual voice-band tones from 0 Hz to 4800 Hz with a resolution of 0.15 Hz and an accuracy of ±0.01%. Tones over 3000 Hz are attenuated. DTMF tone generation allows the modem to operate as a programmable DTMF dialer.

Data Encoding

The data encoding conforms to CCITT recommendation V.32 bis, V.32, V.17, V.29, V.27 ter, V.22 bis, V.22, V.23, or V.21, or is compatible with Bell 212A or 103, depending on the configuration (see Table 1-1).

Equalizers

Equalization functions are provided that improve performance when operating over poor quality lines.

Compromise Equalizer: A digital finite impulse response (FIR) filter in the transmitter provides compromise equalization. The filter taps can be changed in DSP RAM for varying line conditions. The default equalizer tap coefficients compensate for 75% of the amplitude distortion of an EIA B line and for 100% of the group delay distortion of an EIA 2 line. The filter can be enabled or disabled (CEQ bit).

Automatic Adaptive Equalizer: An automatic adaptive equalizer is provided in the receiver. The equalizer can be configured as either a T or a T/2 equalizer (EQT2 bit).

NOTE: Bit notations refer to data, control, and/or status bits in the modem interface memory (see Section 3).

Table 1-1. Configurations, Signaling Rates and Data Rates

Configuration	Modulation[1]	Carrier Frequency (Hz) ±0.01%	Data Rate (bps) ±0.01%	Baud (Symbols/Sec.)	Bits per Symbol		Constellation Points
					Data	TCM	
V.32 bis 14400 TCM[2]	TCM	1800	14400	2400	6	1	128
V.32 bis 12000 TCM[2]	TCM	1800	12000	2400	5	1	64
V.32 bis 9600 TCM[2]	TCM	1800	9600	2400	4	1	32
V.32 bis 7200 TCM[2]	TCM	1800	7200	2400	3	1	16
V.32 bis 4800[2]	QAM	1800	4800	2400	2	0	4
V.32 9600 TCM	TCM	1800	9600	2400	4	1	32
V.32 9600	QAM	1800	9600	2400	4	0	16
V.32 4800	QAM	1800	4800	2400	2	0	4
V.17 14400 TCM/V.33[3]	TCM	1700 or 1800	14400	2400	6	1	128
V.17 12000 TCM/V.33[3]	TCM	1700 or 1800	12000	2400	5	1	64
V.17 9600 TCM[3]	TCM	1700 or 1800	9600	2400	4	1	32
V.17 7200 TCM[3]	TCM	1700 or 1800	7200	2400	3	1	16
V.29 9600[4]	QAM	1700	9600	2400	4	0	16
V.29 7200[4]	QAM	1700	7200	2400	3	0	8
V.29 4800[4]	QAM	1700	4800	2400	2	0	4
V.27 4800[4]	DPSK	1800	4800	1600	3	0	8
V.27 2400[4]	DPSK	1800	2400	1200	2	0	4
V.26 bis 2400	DPSK	1800	2400	1200	2	0	4
V.26 bis 1200	DPSK	1800	1200	1200	1	0	4
V.26 A 2400	DPSK	1800	2400	1200	2	0	4
V.22 bis 2400	QAM	1200/2400	2400	600	4	0	16
V.22 bis 1200	DPSK	1200/2400	1200	600	2	0	4
V.22 1200	DPSK	1200/2400	1200	600	2	0	4
V.22 600	DPSK	1200/2400	600	600	1	0	4
Bell 212A	DPSK	1200/2400	1200	600	2	0	4
Bell 103	FSK	1170/2125	0–300	300	1	0	–
V.23 1200/75	FSK	1700/420	1200/75	1200	1	0	–
V.21	FSK	1080/1750	0–300	300	1	0	–
V.21 Channel 2[4]	FSK	1750	300	300	1	0	–
Tone Transmit	–	–	–	–	–	–	–

Notes: 1. Modulation legend: TCM: Trellis-Coded Modulation; QAM: Quadrature Amplitude Modulation; FSK: Frequency Shift Keying; DPSK: Differential Phase Shift Keying
2. 14400 bps models only.
3. 14400 bps models with fax support only.
4. Models with fax support only.

Transmitted Data Spectrum

When the compromise equalizer is disabled, the transmitter spectrum is shaped by raised cosine filter functions as follows:

Configuration	Raised Cosine Filter Function
V.32 bis/V.32, V.17, V.29	Square root of 12.5%
V.27 ter, V.26	Square root of 50%
V.22 bis/V.22, Bell 212A	Square root of 75%

RTS – CTS Response Time

The response times of CTS relative to a corresponding transition of RTS are listed in Table 1-2.

Transmit Level

The transmitter output level is selectable from 0 dBm to –15 dBm in 1 dB steps and is accurate to ±0.5 dB when used with an external hybrid. The output level can also be fine tuned to a value within a 1 dB step by changing a gain constant in RAM. The maximum V.32/V.32 bis transmit level for acceptable receive performance should not exceed –9 dBm.

Transmitter Timing

Transmitter timing is selectable between internal (±0.01%), external, or slave.

Scrambler/Descrambler

A self-synchronizing scrambler/descrambler is used in accordance with the selected configuration.

Answer Tone

The modem generates a 2100 Hz answer tone for 3.6 seconds at the beginning of the answer handshake when the NV25 bit is a zero (V.32 bis, V.32, V.22 bis, V.22, V.23, and V.21). The V.32 bis/V.32 answer tone has 180° phase reversals every 0.45 second to disable network echo cancellers.

Table 1-2. RTS-CTS Response Time

Configuration	RTS-CTS Response[1]		Turn-Off Sequence[3]
	Constant Carrier	Controlled Carrier	
V.32 bis, V.32	≤ 2 ms	N/A	N/A
V.33/V.17 Long	N/A	1393 ms[2]	15 ms[4]
V.33/V.17 Short	N/A	142 ms[2]	15 ms[4]
V.29	N/A	253 ms[2]	12 ms
V.27 4800 Long	N/A	708 ms[2]	7 ms[4]
V.27 4800 Short	N/A	50 ms[2]	7 ms[4]
V.27 2400 Long	N/A	943 ms[2]	10 ms[4]
V.27 2400 Short	N/A	67 ms[2]	10 ms[4]
V.26	N/A	60 ms	10 ms
V.22 bis, V.22, Bell 212A	≤ 2 ms	270 ms	N/A
V.21	500 ms	500 ms	N/A
V.23, Bell 103	210 ms	210 ms	N/A

Notes:

1. Times listed are CTS turn-on. The CTS OFF-to-ON response time is host programmable in DSP RAM.
2. Add echo protector tone duration plus 20 ms when echo protector tone is used during turn-on.
3. Turn-off sequence consists of transmission of remaining data and scrambled ones for controlled carrier operation. CTS turn-off is less than 2 ms for all configurations.
4. Plus 20 ms of no transmitted energy.

Receive Level

The modem satisfies performance requirements for received line signal levels from 0 dBm to –43 dBm measured at the Receiver Analog (RXA) input.

Receiver Timing

The timing recovery circuit can track a frequency error in the associated transmit timing source of ±0.035% (V.22 bis) or ±0.01% (other configurations).

Carrier Recovery

The carrier recovery circuit can track a ± 7 Hz frequency offset in the received carrier with less than a 0.2 dB degradation in bit error rate (BER).

Clamping

Received Data (RXD) is clamped to a constant mark whenever the Received Line Signal Detector ($\overline{\text{RLSD}}$) is off. $\overline{\text{RLSD}}$ can be clamped off (RLSDE bit).

Echo Canceller

A data echo canceller with near-end and far-end echo cancellation is included for 2-wire full-duplex V.32 bis/V.32 operation. The combined echo span of near and far cancellers is 35.8 ms. The proportion allotted to each end is automatically determined by the modem. The delay between near-end and far-end echoes can be up to 1.25 seconds. The canceller can compensate for ± 7 Hz frequency offset in the far-end echo. The echo canceller error signal may be monitored through modem interface memory.

ADPCM Voice Mode (RCV96DPL and RCV144DPL)

The ADPCM codec compresses and decompresses voice signals to allow efficient digital storage of voice messages. The codec operates at 28.8k, 21.6k, or 14.4k bps (4-bit, 3-bit, or 2-bit quantization, respectively) with a default 7.2 kHz programmable sample rate. Optional coder silence detection/deletion and decoder silence interpolation are included to achieve greater compression rates.

Transmit Voice. 16-bit compressed transmit voice can be sent to the modem ADPCM codec for decompression then to the digital-to-analog converter (DAC) by the host.

Receive Voice. 16-bit received voice samples from the modem analog-to-digital converter (ADC) can be sent to the ADPCM codec for compression, and then be read by the nost.

Voice Pass-Through Mode (RCV96DPL and RCV144DPL)

Transmit Voice. 16-bit transmit voice samples can be sent to the modem DAC from the host.

Receive Voice. 16-bit received voice samples from the modem ADC can be read by the host.

Data Formats

Serial Synchronous Data

Data rate: 14400, 12000, 9600, 7200, 4800, 2400, 1200, 600, or 300 bps ±0.01%.

Selectable clock: Internal, external, or slave.

Serial Asynchronous Data

Data rate: 14400, 12000, 9600, 7200, 4800, 2400, 1200, or 600 bps +1% (or +2.3%), -2.5%; 0-300 bps (V.21 and Bell 103). 1200/75 bps (V.23).

Bits per character: 7, 8, 9, 10, or 11.

Parallel Synchronous Data

Normal sync: 8-bit data for transmit and receive

Data rate: 14400, 12000, 9600, 7200, 4800, 2400, 1200, 600, or 300 bps ±0.01%.

SDLC/HDLC support:

Transmitter: Flag generation, 0 bit stuffing, CCITT CRC-16 or CRC-32 generation.

Receiver: Flag detection, 0 bit un-stuffing, CCITT CRC-16 or CRC-32 checking.

Parallel Asynchronous Data

Data rate: 14400, 12000, 9600, 7200, 4800, 2400, 1200, or 600 bps +1% (or 2.3%), -2.5%; 1200, 300, or 75 bps (FSK).

Data bits per character: 5, 6, 7, or 8.

Parity generation/checking: Odd, even, or 9th data bit.

Async/Sync and Sync/Async Conversion

An asynchronous-to-synchronous converter is provided in the transmitter and a synchronous-to-asynchronous converter is provided in the receiver. The converters operate in both serial and parallel modes. The asynchronous character format is 1 start bit, 5 to 8 data bits, an optional parity bit, and 1 or 2 stop bits. Valid character size, including all bits, is 7, 8, 9, 10, or 11 bits per character. Two ranges of signaling rates are provided:

- Basic range: +1% to -2.5%
- Extended overspeed range: +2.3% to -2.5%

When the transmitter's converter is operating at the basic signaling rate, no more than one stop bit will be deleted per 8 consecutive characters. When operating at the extended rate, no more than one stop bit will be deleted per 4 consecutive characters. Break handling is performed as described in V.14.

Asynchronous characters are accepted by the modem from the host on the TXD serial input in the serial data mode or the TBUFFER register in parallel data mode (determined by the TDPM bit; see Table 3-1). Asynchronous characters are issued on the RXD serial output and the RBUFFER register in both modes. To configure the converters, the host must set up interface memory bits EXOS, PEN, STB and WDSZ bits before setting ASYN.

V.54 Inter-DCE Signalling

V.54 inter-DCE signalling procedures in synchronous and asynchronous configurations are supported. Transmission and detection of the preparatory, acknowledgment, and termination phases as defined in V.54 are provided. Three control bits allow the host to send the appropriate bit patterns (V54T, V54A, and V54P bits). Three other control bits are used to enable one of three bit pattern detectors (V54TE, V54AE, and V54PE bits). A status bit indicates when the selected pattern detector has found the corresponding bit pattern (V54DT bit).

V.13 Remote RTS Signalling

V.13 remote RTS signalling is supported. Transmission and detection of signalling bit patterns in response to a change of state in the RTS bit or the RTS input signal are provided. The RRTSE bit enables V.13 signalling. The RTSDE bit enables detection of V.13 patterns. The RTSDT status bit indicates the state of the remote RTS signal. This feature may be used to clamp/unclamp the local RLSD and RXD signals in response to a change in the remote RTS signal in order to simulate controlled carrier operation in a constant carrier environment. The modem automatically clamps and unclamps RLSD.

Auto-Dialing and Auto-Answering Control

The host can perform auto-dialing and auto-answering. These functions include DTMF or pulse dialing, ringing detection and a comprehensive supervisory tone detection scheme. The major parameters are host programmable.

Supervisory Tone Detection

Three parallel tone detectors (A, B, and C) are provided for supervisory tone detection. The signal path to these detectors is separate from the main received signal path.

Each tone detector consists of two cascaded second order IIR biquad filters. The coefficients are host programmable. Each fourth order filter is followed by a level detector which has host programmable turn-on and turn-off thresholds allowing hysteresis. Tone detector C is preceded by a prefilter and squarer. This circuit is useful for detecting a tone with frequency equal to the difference between two tones that may be simultaneously present on the line. The squarer may be disabled by the SQDIS bit causing tone detector C to be an eighth order filter. The tone detectors are disabled in data mode.

The default bandwidths and thresholds of the tone detectors are as follows:

Tone Detector	Bandwidth	Turn-On Threshold	Turn-Off Threshold
A	245 – 650 Hz	-25 dBm	-31 dBm
B	360 – 440 Hz	-25 dBm	-31 dBm
C Prefilter	0 – 500 Hz	N/A	N/A
C	50 – 110 Hz	*	*

*Tone Detector C will detect a difference tone within its bandwidth when the two tones present are in the -1 dBm to -26 dBm range.

Auto Mode Selection

Automatic mode selection is available in V.32 bis/V.32 based on EIA/TIA PN-2330 (Draft). When enabled, the modem will determine the communication standard supported by the remote modem and configure itself according. Configurations supported are: V.32 bis, V.32, V.22 bis, V.22, Bell 212A, Bell 103, V.23, and V.21.

DTMF Detection

A DTMF tone pair can be detected and a corresponding code loaded into interface memory for access by the host (DTMFD and DTMFW bits). The 0–9, A–D, *, and # digits are supported. The received DTMF signal must be at least 6 dB above the local voice echo if DTMF detection is used while transmitting voice.

511 Pattern Generation/Detection

In a synchronous mode, a 511 pattern can be generated and detected (S511 bit). Use of this bit pattern during self test eliminates the need for external test equipment.

In-Band Secondary Channel

A full duplex in-band secondary channel is provided in V.32/V.32bis modes (except 4800 bps). Control bit SECEN (1A:0) enables and disables the secondary channel operation. The secondary channel operates in parallel data mode with independent transmit and receive interrupts and data buffers. The main channel may operate in parallel or serial mode. The secondary channel data rate is 150 bps. The rate is host programmable.

Transmit and Receive FIFO Data Buffers

Two 8-byte first-in first out (FIFO) data buffers allow the DTE/host to rapidly output up to 9 bytes of transmit data and input up to 9 bytes of accumulated received data. The receiver FIFO is always enabled. The transmitter FIFO is enabled by the FIFOEN control bit. TXHF and RXHF bits indicate the corresponding FIFO buffer half full (4 or more bytes loaded) status. TXFNE and RXFNE bits indicate the corresponding FIFO buffer not empty status. An interrupt mask register allows an interrupt request to be generated whenever the TXFNE, RXFNE, RXHF, or TXHF status bit changes state.

DMA Support Interrupt Request Lines

DMA support is available in synchronous, asynchronous and HDLC parallel data modes. Control bit DMAE (1A:4) enables and disables DMA support. When DMA support is enabled, the modem RI and DSR lines are assigned to Transmitter Request (TXRQ) and Receiver Request (RXRQ) hardware output interrupt request lines, respectively. The TXRQ and RXRQ signals follow the assertion of the TDBE and RDBF interrupt bits thus allowing the DTE/host to respond immediately to the interrupt request without masking out status bits to determine the interrupt source.

NRZI Encoding/Decoding

NRZI data encoding/decoding may be selected in synchronous and HDLC modes instead of the default NRZ (control bit NRZIEN). In NRZ encoding, a 1 is represented by a high level and a 0 is represented by a low level. In NRZI encoding, a 1 is represented by no change in level and a 0 is represented by a change in level.

CCITT CRC-32 Support

CCITT CRC-32 generation/checking may be selected in HDLC mode using DSP RAM access instead of the default CCITT CRC-16.

Caller ID Demodulation

Caller ID information can be demodulated in V.23 1200 receive configuration and presented to the host/DTE in serial (TXD) and parallel (RBUFFER) form.

Telephone Line Interface

Line Transformer Interface: Internal differential drivers allow direct connection to the line tranformer (see Section 2.2).

Relay Control: Direct control of the off-hook and talk/data relays is provided. Internal relay drivers allow direct connection to the off-hook and talk/data relays. The talk/data relay output can optionally be used for pulse dial.

Speaker Interface

A SPKR output is provided with on/off and volume control logic incorporated in the modem, requiring only an external amplifier to drive a loudspeaker.

2 HARDWARE INTERFACE

2.1 HARDWARE INTERFACE SIGNALS

The functional interconnect diagram (Figure 2-1) shows the typical modem connection in a system. In this diagram, any point that is active low is represented by a small circle at the signal point.

Edge triggered inputs are denoted by a small triangle (e.g., TDCLK). Open-Collector (open-source or open-drain) outputs are denoted by a small half-circle (e.g., $\overline{\text{RESET}}$). Active low signals are overscored (e.g., $\overline{\text{DTR}}$).

A clock intended to activate logic on its rising edge (low-to-high transition) is called active low (e.g., $\overline{\text{RDCLK}}$), while a clock intended to activate logic on its falling edge (high-to-low transition) is called active high, (e.g., TDCLK). When a clock input is associated with a small circle, the input activates on a falling edge. If no circle is shown, the input activates on a rising edge.

The modem pin assignments for the 68-pin PLCC are listed in Table 2-1 and are shown in Figure 2-2.

The modem pin assignments for the 100-pin and 80-pin PQFPs are listed in Table 2-2 and are shown in Figure 2-3.

The hardware interface signals are described in Table 2-3.

The digital and analog interface characteristics are defined in Tables 2-4 and 2-5.

The absolute maximum ratings are listed in Table 2-6.

The timing for DTE host microprocessor interface bus waveforms is shown in Table 2-7. The host bus waveforms are illustrated in Figure 2-4.

The DTE serial interface waveforms are illustrated in Figure 2-5.

Eye pattern diagnostic waveforms are illustrated in Figure 2-6.

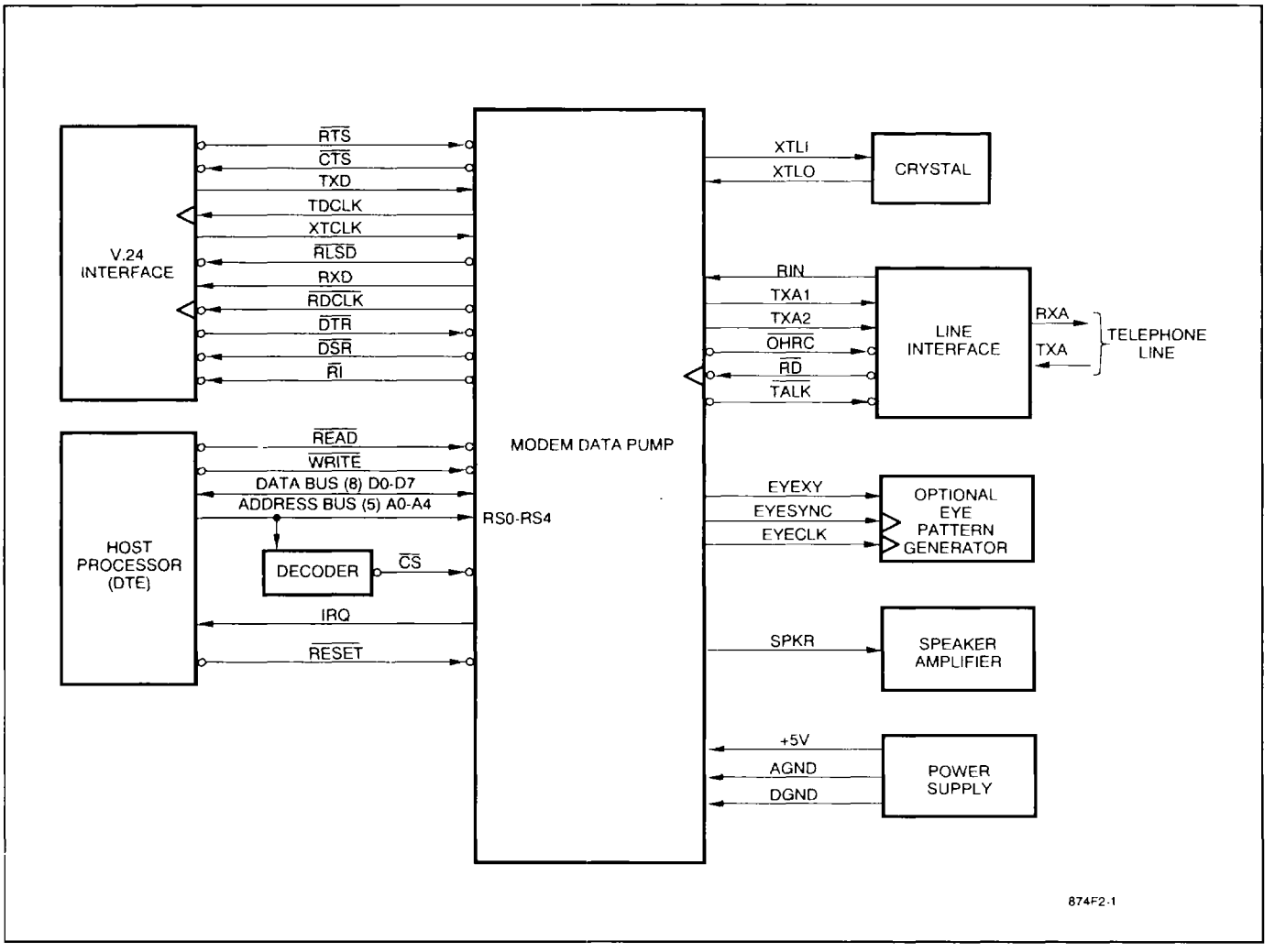


Figure 2-1. Modem Functional Interconnect

Table 2-1. Modem Pin Assignments - 68-Pin PLCC

Pin	Signal Label	Type	Interface
1	VREG[3]	MI	To GND thru 0.1 µF (Optional)
2	DSP_RESET	MI	Output to RES
3	IA_CLKIN	MI	Output to CLKIN
4	DSP_IRQ	MI	Input from IRQ
5	RI	OA	DTE Serial Interface
6	RD	IA	Line Interface
7	RTS	IA	DTE Serial Interface
8	IRQ	OA	Host Parallel Interface
9	D1	IA/OA	Host Parallel Interface
10	DGND1	GND	
11	+5VD1	PWR	
12	XTLI	I	Crystal/Clock Circuit
13	XTLO	O	Crystal/Clock Circuit
14	D0	IA/OA	Host Parallel Interface
15	D2	IA/OA	Host Parallel Interface
16	D3	IA/OA	Host Parallel Interface
17	D5	IA/OA	Host Parallel Interface
18	D7	IA/OA	Host Parallel Interface
19	DGND2	GND	
20	RS0	IA	Host Parallel Interface
21	+5VA	PWR	
22	AGND1	GND	
23	RIN	I(DA)	Line Interface
24	VC	MI	To GND through capacitors
25	VREF	MI	To VC through capacitors
26	TXA2	O(DD)	Line Interface
27	TXA1	O(DD)	Line Interface
28	TALK	OD	Line Interface
29	SPKR	O(DF)	Speaker Circuit
30	AGND2	GND	
31	OHRC	OD	Line Interface
32	POR	MI	Connect to RESET
33	CLKIN	MI	Output from IA_CLKIN
34	DTR	IA	DTE Serial Interface
35	RXD	OA	DTE Serial Interface
36	+5VD2	PWR	
37	CTS	OA	DTE Serial Interface
38	IRQ	MI	Output to DSP_IRQ
39	RES	MI	Input from DSP_RESET
40	DGND3	GND	
41	+5VD3	PWR	
42	RXOUT	MI	NC
43	DGND4	GND	
44	RMODE	MI	Connect to TMODE
45	TMODE	MI	Connect to RMODE
46	EYESYNC	OA	Eye Pattern Test Circuit
47	EYECLK	OA	Eye Pattern Test Circuit
48	EYEXY	OA	Eye Pattern Test Circuit
49	TXDAT	MI	NC
50	TDCLK	OA	DTE Serial Interface
51	RLSD	OA	DTE Serial Interface
52	RDCLK	OA	DTE Serial Interface
53	GP0	MI	Connect to EYESYNC
54	XTCLK	IA	DTE Serial Interface
55	DGND5	GND	
56	+5VD4	PWR	
57	TXD	IA	DTE Serial Interface
58	DSR	OA	DTE Serial Interface
59	RESET	OA	Host Parallel Interface

Table 2-1. Modem Pin Assignments - 68-Pin PLCC (Cont'd)

Pin	Signal Label	Type	Interface
60	READ	IA	Host Parallel Interface
61	WRITE	IA	Host Parallel Interface
62	CS	IA	Host Parallel Interface
63	RS4	IA	Host Parallel Interface
64	RS3	IA	Host Parallel Interface
65	RS2	IA	Host Parallel Interface
66	RS1	IA	Host Parallel Interface
67	D6	IA/OA	Host Parallel Interface
68	D4	IA/OA	Host Parallel Interface

Notes:

1. I/O types:
   MI = Modem interconnect.
   Digital input (IA, IB, etc.) and output (OA, OB, etc.).
   Analog input [I(DA)] and output [O(DD), O(DF), etc.].
2. NC = No external connection.
3. VREG pin can be NC; capacitor connection required for compatibility with future products.

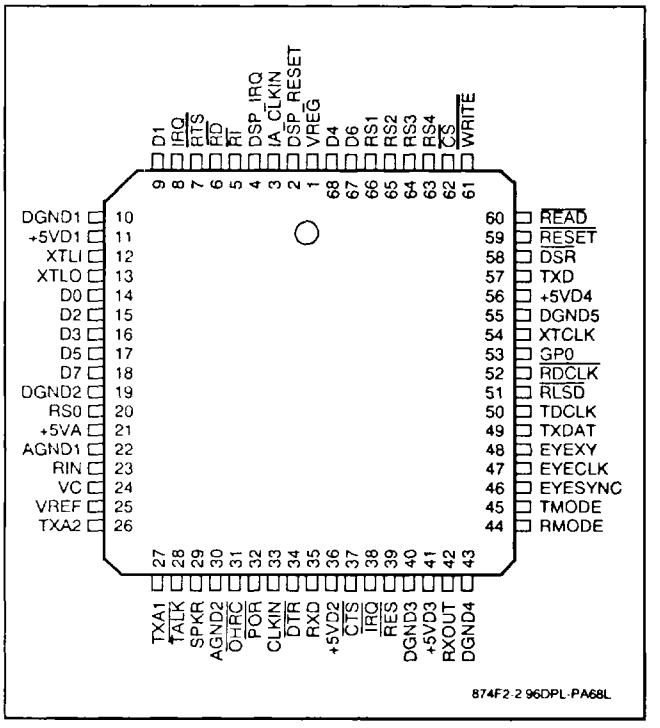


Figure 2-2. Pin Assignments- 68-Pin PLCC

Table 2-2a. Modem Pin Assignments - 100-Pin PQFP

Pin	Signal Label	Type	Interface
1	RS2	IA	Host Parallel Interface
2	RS3	IA	Host Parallel Interface
3	RS4	IA	Host Parallel Interface
4	CS	IA	Host Parallel Interface
5	WRITE	IA	Host Parallel Interface
6	READ	IA	Host Parallel Interface
7	CTS	OA	DTE Serial Interface
8	DTR	IA	DTE Serial Interface
9	TXD	IA	DTE Serial Interface
10	TDCLK	OA	DTE Serial Interface
11	RLSD	OA	DTE Serial Interface
12	TIRO2	MI	MD2: TIRO2
13	RXD	OA	DTE Serial Interface
14	RDCLK	OA	DTE Serial Interface
15	NC		
16	GND1	GND	
17	RXOUT	MI	MD2: SR3IN
18	RMODE	MI	MD1: TMODE/MD2: SR1IO
19	TSTROBE	MI	MD2: IA1CLK
20	TRESET	MI	MD2: SA1CLK
21	DGND1	GND	
22	NC		
23	TMODE	MI	MD1: RMODE/MD2: SR1IO
24	TXDAT	MI	MD2: SR4OUT
25	+5VA1	PWR	
26	TALK	OD	Line Interface
27	AGND1	GND	
28	TXA1	O(DD)	Line Interface
29	TXA2	O(DD)	Line Interface
30	DGND2	GND	
31	NC		
32	NC		
33	NC		
34	NC		
35	+5VA2	PWR	
36	SLEEP	MI	MD1: MD1_SLEEP
37	AGND2	GND	
38	RIN	I(DA)	Line Interface
39	VC	MI	To GND through capacitors
40	VREF	MI	To VC through capacitors
41	NC		
42	NC		
43	DGND3	GND	
44	SPKR	O(DF)	Speaker Circuit
45	+5VA3	PWR	
46	OHRC	OD	Line Interface
47	POR	MI	MD1: RESET
48	CLKIN	MI	MD1: MD1_CLKIN
49	NC		
50	A13	MI	MD2: RS4
51	NC		
52	DSR	OA	DTE Serial Interface
53	ES3	MI	MD2: CSP
54	RESET	IA	Host Parallel Interface
55	NC		
56	+5VD1	PWR	
57	AD0	MI	MD2: D0
58	AD1	MI	MD2: D1
59	AD2	MI	MD2: D2

Table 2-2a. Modem Pin Assignments - 100-Pin PQFP (Cont'd)

Pin	Signal Label	Type	Interface
60	AD3	MI	MD2: D3
61	AD4	MI	MD2: D4
62	AD5	MI	MD2: D5
63	AD6	MI	MD2: D6
64	AD7	MI	MD2: D7
65	A0	MI	MD2: RS0
66	GND2	GND	
67	A1	MI	MD2: RS1
68	A2	MI	MD2: RS2
69	A3	MI	MD2: RS3
70	MD1_SLEEP	MI	MD1: SLEEP
71	NC		
72	MD2_RESET	MI	MD2: RESETP
73	YCLK	MI	MD2: YCLK
74	XCLK	MI	MD2: XCLK
75	MD1_CLKIN	MI	MD1: CLKIN
76	MD2_IRQ	MI	MD2: IRQP
77	RI	OA	DTE Serial Interface
78	RD	IA	Line Interface
79	RTS	IA	DTE Serial Interface
80	GND3	GND	
81	GND4	GND	
82	IRQ	OA	Host Parallel Interface
83	WTP	MI	MD2: WTP
84	RDP	MI	MD2: RDP
85	NC		
86	+5VD2	PWR	
87	XTLI	I	Crystal/Clock Circuit
88	XTLO	O	Crystal/Clock Circuit
89	D0	IA/OA	Host Parallel Interface
90	D1	IA/OA	Host Parallel Interface
91	D2	IA/OA	Host Parallel Interface
92	D3	IA/OA	Host Parallel Interface
93	D4	IA/OA	Host Parallel Interface
94	D5	IA/OA	Host Parallel Interface
95	D6	IA/OA	Host Parallel Interface
96	D7	IA/OA	Host Parallel Interface
97	GND5	GND	
98	NC		
99	RS0	IA	Host Parallel Interface
100	RS1	IA	Host Parallel Interface

Notes:

1. I/O types:
   MI = Modem interconnect.
   Digital input (IA, IB, etc.) and output (OA, OB, etc.).
   Analog input [I(DA)] and output [O(DD), O(DF), etc.].
2. NC = no external connection.

Table 2-2b. Modem Pin Assignments - 80-Pin PQFP

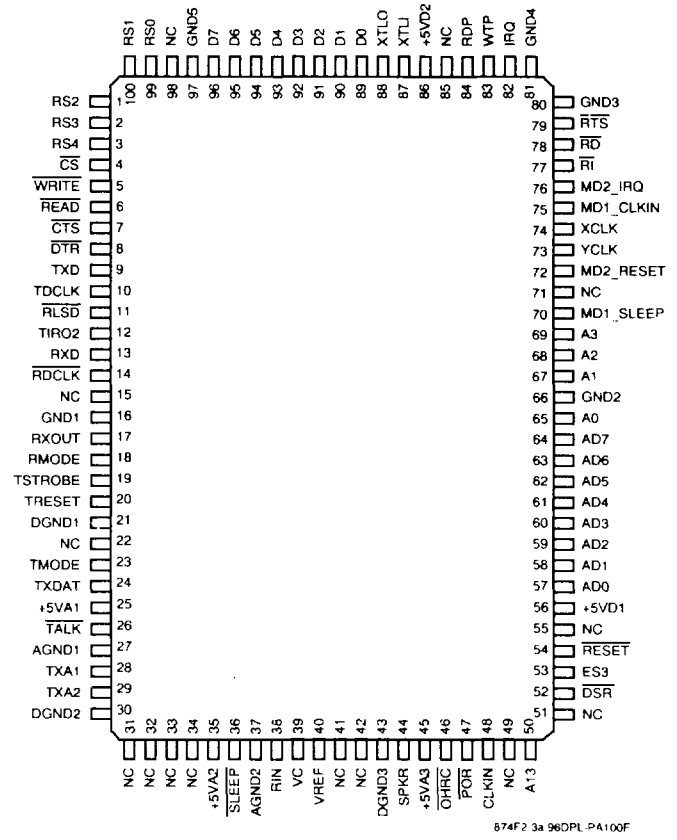
Pin	Signal Label	Type	Interface
1	EYESYNC	OA	Eye Pattern Test Circuit
2	NC		
3	NC		
4	NC		
5	IA1CLK	MI	MD1: TSTROBE
6	EYECLK	MI	Eye Pattern Test Circuit
7	SA1CLK	MI	MD1: TRESET
8	SR1IO	MI	MD1: TMODE
9	NC		
10	EYEXY	OA	Eye Pattern Test Circuit
11	DGND1	GND	
12	GP17	MI	Connect to DGND
13	GP16	MI	Connect to DGND
14	SR4OUT	MI	MD1: TXDAT
15	TDCLK	IA	DTE: Serial Interface
16	NC		
17	RLSD	IA	DTE: Serial Interface
18	RDCLK	IA	DTE: Serial Interface
19	GP0	MI	Connect to EYESYNC
20	XTCLK	IA	DTE: Serial Interface
21	NC		
22	TXD	IA	DTE: Serial Interface
23	TIRO2	MI	MD1: TIRO2
24	RS4	MI	MD1: A13
25	RS3	MI	MD1: A3
26	RS2	MI	MD1: A2
27	RS1	MI	MD1: A1
28	RS0	MI	MD1: A0
29	+5VD1	PWR	
30	+5VD2	PWR	
31	DGND2	GND	
32	DGND3	GND	
33	D7	MI	MD1: AD7
34	D6	MI	MD1: AD6
35	D5	MI	MD1: AD5
36	D4	MI	MD1: AD4
37	D3	MI	MD1: AD3
38	D2	MI	MD1: AD2
39	+5VD3	PWR	
40	NC		
41	+5VD4	PWR	
42	D1	MI	MD1: AD1
43	D0	MI	MD1: AD0
44	WRITEP	MI	MD1: WTP
45	CSP	MI	MD1: ES3
46	READP	MI	MD1: RDP
47	NC		
48	NC		
49	NC		
50	DGND4	GND	
51	NC		
52	+5VD5	PWR	
53	NC		
54	NC		
55	NC		
56	NC		
57	NC		
58	NC		

Table 2-2b. Modem Pin Assignments - 80-Pin PQFP

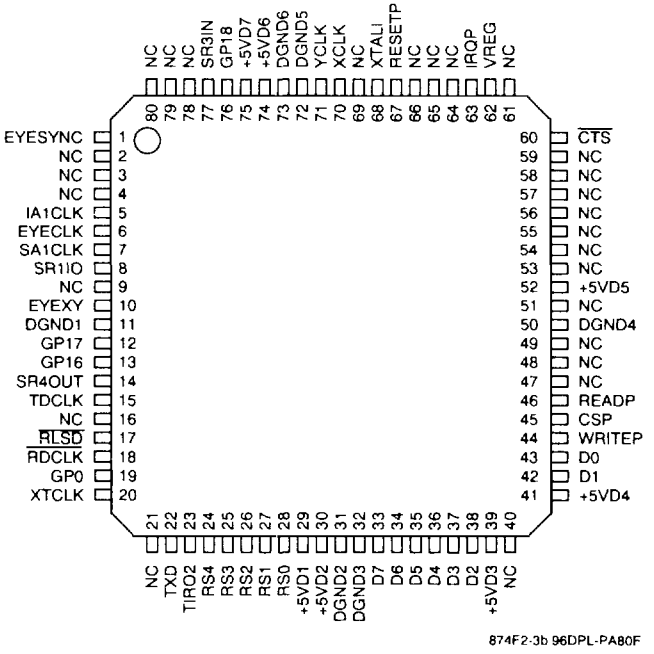
Pin	Signal Label	Type	Interface
59	NC		
60	CTS	MI	DTE: Serial Interface
61	NC		
62	VREG[3]	MI	To GND thru 0.1 µF (Optional)
63	IRQP	MI	MD1: MD2_IRQ
64	NC		
65	NC		
66	NC		
67	RESETP	MI	MD1: MD2_RESET
68	XTALI	I	Connect to DGND
69	NC		
70	XCLK	MI	MD1: XCLK
71	YCLK	MI	MD1: YCLK
72	DGND5	GND	
73	DGND6	GND	
74	+5VD6	PWR	
75	+5VD7	PWR	
76	GP18	MI	Connect to DGND
77	SR3IN	MI	MD1: RXOUT
78	NC		
79	NC		
80	NC		

Notes:

1. I/O types:
   MI = Modem interconnect
   Digital input (IA, IB, etc.) and output (OA, OB, etc.).
   Analog input [I(DA)] and output [O(DD), O(DF), etc.].
2. NC = no external connection.
3. VREG pin can be NC; capacitor connection required for compatibility with future products.



a. 100-Pin PQFP



b. 80-Pin PQFP

Figure 2-3. Pin Assignments - 100-Pin and 80-Pin PQFPs

Table 2-3. Hardware Interface Signal Definitions

Label	I/O Type	Signal/Definition
		OVERHEAD SIGNALS
XTLI XTLO	I O	**Crystal In and Crystal Out.** The modem must be connected to an external crystal circuit consisting of a 35.2512 MHz crystal, three capacitors, and an inductor, or to a square wave generator/sine wave oscillator.
$\overline{\text{RESET}}$	IA	**Reset.** $\overline{\text{RESET}}$ low holds the modem in the reset state. $\overline{\text{RESET}}$ going high releases the modem from the reset state and initiates normal operation using power turn-on (default) values. The modem is ready to use 500 ms after the low-to-high transition of $\overline{\text{RESET}}$. The reset sequence is re-initiated any time the +5V supply drops below +3.5V for more than 30 ms, or an external device drives $\overline{\text{RESET}}$ low for at least 3 µs. The reset sequence initializes the modem interface memory to default values (Table 3-1). **NOTE:** If the modem is used in applications where the supply voltage can drop below +4.75V but not low enough to cause a reset sequence (i.e., <3.5V), the host system should assert $\overline{\text{RESET}}$ upon supply voltage recovery to ensure proper modem initialization and operation.
+5VD	PWR	**+ 5V Digital Supply.** +5V ± 5%.
+5VA	PWR	**+ 5V Analog Supply.** +5V ± 5%.
DGND	GND	**Digital Ground.** Connect to ground.
AGND	GND	**Analog Ground.** Connect to ground.
		MICROPROCESSOR BUS Address, data, control, and interrupt hardware interface signals allow modem connection to an 8086-compatible microprocessor bus. With the addition of external logic, the interface can be made compatible with a wide variety of other microprocessors such as the 6502, 8086 or 68000. The microprocessor interface allows a microprocessor to change modem configuration, read or write channel and diagnostic data, and supervise modem operation by writing control bits and reading status bits.
D0–D7	IA/OB	**Data Lines.** Eight bidirectional data lines (D0–D7) provide parallel transfer of data between the host and the modem. The most significant bit is D7. Data direction is controlled by the Read Enable and Write Enable signals.
RS0–RS4	IA	**Register Select Lines.** The five active high register select lines (RS0–RS4) address interface memory registers within the modem interface memory. These lines are typically connected to the five least significant lines (A0–A4) of the address bus. The modem decodes RS0 through RS4 to address one of 32 internal interface memory registers (00–1F). The most significant address bit is RS4 while the least significant address bit is RS0. The selected register can be read from or written into via the 8-bit parallel data bus (D0–D7). The most significant data bit is D7 while the least significant data bit is D0.
$\overline{\text{CS}}$	IA	**Chip Select.** $\overline{\text{CS}}$ selects the modem for microprocessor bus operation. $\overline{\text{CS}}$ is typically generated by decoding host address bus lines.
$\overline{\text{READ}}$ $\overline{\text{WRITE}}$	IA IA	**Read Enable and Write Enable.** During a read cycle ($\overline{\text{READ}}$ asserted), data from the selected interface memory register is gated onto the data bus by means of three-state drivers in the modem. These drivers force the data lines high for a one bit, or low for a zero bit. When not being read, the three-state drivers assume their high-impedance (off) state. During a write cycle ($\overline{\text{WRITE}}$ asserted), data from the data bus is copied into the selected modem interface memory register, with high and low bus levels representing one and zero bit states, respectively.
IRQ	OA	**Interrupt Request.** The modem IRQ output may be connected to the host processor interrupt request input in order to interrupt host program execution for immediate modem service. The IRQ output can be enabled in the modem interface memory to indicate immediate change of conditions. The use of IRQ is optional depending upon modem application. The IRQ output is driven by a TTL-compatible CMOS driver.

Table 2-3. Hardware Interface Signal Definitions (Cont'd)

Label	I/O Type	Signal/Definition
		V.24 SERIAL INTERFACE
		Timing, data, control, and status signals provide a V.24-compatible serial interface. These signals are TTL compatible in order to drive the short wire lengths and circuits normally found within a printed circuit board, stand-alone modem enclosures, or equipment cabinets. For driving longer cables, these signals can be easily converted to EIA-232-D voltage levels.
TXD	IA	**Transmitted Data.** The modem obtains serial data to be transmitted from the local DTE on the Transmitted Data (TXD) input.
RXD	OA	**Received Data.** The modem presents received serial data to the local DTE on the Received Data (RXD) output.
$\overline{\text{RTS}}$	IA	**Request to Send.** Activating ($\overline{\text{RTS}}$) causes the modem to transmit data on TXD when $\overline{\text{CTS}}$ becomes active. The $\overline{\text{RTS}}$ pin is logically ORed with the RTS bit.
$\overline{\text{CTS}}$	OA	**Clear To Send. $\overline{\text{CTS}}$** active indicates to the local DTE that the modem will transmit any data present on TXD. CTS response times from an active condition of RTS are shown in Table 2.
$\overline{\text{RLSD}}$	OA	**Received Line Signal Detector.** $\overline{\text{RLSD}}$ active indicates to the local DTE that energy above the receive level threshold is present on the receiver input, and that the energy is not a training sequence. One of four $\overline{\text{RLSD}}$ receive level threshold options can be selected (RTH bits). A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold level and hysteresis action are measured with a modulated signal applied to the Receiver Analog (RXA) input. Note that performance may be degraded when the received signal level is less than –43 dBm. The $\overline{\text{RLSD}}$ on and off thresholds are host programmable in DSP RAM.
$\overline{\text{DTR}}$	IA	**Data Terminal Ready.** In V.32 bis, V.32, V.22 bis, V.22, or Bell 212A configuration, activating $\overline{\text{DTR}}$ initiates the handshake sequence, provided that the DATA bit is a 1. If in answer mode, the transmitter will immediately send answer tone. In V.21, V.23, or Bell 103 configuration, activating $\overline{\text{DTR}}$ causes the modem to enter the data state provided that the DATA bit is a 1. If in answer mode, the transmitter will immediately send answer tone. In these modes, if controlled carrier is enabled, carrier is controlled by RTS. During the data mode, deactivating $\overline{\text{DTR}}$ causes the transmitter and receiver to turn off and return to the idle state. The $\overline{\text{DTR}}$ input and the DTR control bit are logically ORed.
$\overline{\text{DSR}}$	OA	**Data Set Ready.** $\overline{\text{DSR}}$ ON indicates that the modem is in the data transfer state. $\overline{\text{DSR}}$ OFF indicates that the DTE is to disregard all signals appearing on the interchange circuits except Ring Indicator ($\overline{\text{RI}}$). $\overline{\text{DSR}}$ is OFF when the modem is in a test mode (i.e., local analog or remote digital loopback). The DSR status bit reflects the state of the $\overline{\text{DSR}}$ output.
$\overline{\text{RI}}$	OA	**Ring Indicator.** $\overline{\text{RI}}$ output follows the ringing signal present on the line with a low level (0V) during the ON time, and a high level (+5V) during the OFF time coincident with the ringing signal. The RI status bit reflects the state of the $\overline{\text{RI}}$ output.
TDCLK	OA	**Transmit Data Clock.** The modem outputs a synchronous Transmit Data Clock (TDCLK) for USRT timing. The TDCLK frequency is the data rate (±0.01%) with a duty cycle of 50 ±1%. The TDCLK source can be internal, external (input on XTCLK) or slave (to $\overline{\text{RDCLK}}$) as selected by TXCLK bits in interface memory.
XTCLK	IA	**External Transmit Clock.** In synchronous communication, an external transmit data clock can be connected to the modem XTCLK input. The clock supplied at XTCLK must exhibit the same characteristics as TDCLK. The XTCLK input is then reflected at the TDCLK output.
$\overline{\text{RDCLK}}$	OA	**Receive Data Clock.** The modem outputs a synchronous Receive Data Clock ($\overline{\text{RDCLK}}$) for USRT timing. The $\overline{\text{RDCLK}}$ frequency is the data rate (±0.01%) with a duty cycle of 50 ±1%. The $\overline{\text{RDCLK}}$ low-to-high transitions coincide with the center of the received data bits.

Table 2-3. Hardware Interface Signal Definitions (Cont'd)

Label	I/O Type	Signal/Definition
		LINE INTERFACE
TXA1 TXA2	O(DF)	**Transmit Analog 1 and 2.** The TXA1 and TXA2 outputs are differential outputs 180 degrees out of phase with each other. Each output can drive a 300 Ω load. Typical line interface circuits are shown in Figures 8-4 and 8-5. Future higher speed modems data pumps will require a hybrid interface such as shown in Figure 8-5 and will not support the interface shown in Figure 8-4. This should be considered when designing a printed circuit board for compatibility with future higher speed modem data pumps.
RIN	I(DA)	**Receive Analog.** RIN is a single-ended receive data input from the telephone line interface or an optional external hybrid circuit.
$\overline{RD}$	IA	**Ring Detect.** The $\overline{RD}$ input is monitored for pulses in the range of 15 Hz to 68 Hz. The frequency detection range may be changed by the host in DSP RAM. The circuit driving $\overline{RD}$ should be a 4N35 optoisolator or equivalent. The circuit driving $\overline{RD}$ should not respond to momentary bursts of ringing less than 125 ms in duration, or less than 40 VRMS (15 Hz to 68 Hz) across TIP and RING. Detected ring signals are reflected on the $\overline{RI}$ output signal as well as the RI bit.
$\overline{OHRC}$	OD	**Off-Hook Relay Control.** The $\overline{OHRC}$ output can directly drive a +5V reed relay coil with a minimum resistance of 360 ohms (13.9 mA max. @ 5.0V) and having a must-operate voltage of no greater than 4.0 Vdc. A clamp diode, such as a 1N4148, should be installed across the relay coil. An external transistor can be used to drive heavier loads (e.g., electro-mechanical relays). $\overline{OHRC}$ is controlled by the host setting the RA bit. In a typical application, $\overline{OHRC}$ is connected to the normally open Off-Hook relay. In this case, $\overline{OHRC}$ active closes the relay to connect the modem to the telephone line.
$\overline{TALK}$	OD	**Talk/Data Relay Control.** The $\overline{TALK}$ output can directly drive a +5V reed relay coil with a minimum resistance of 360 ohms (13.9 mA max. @ 5.0V) and having a must-operate voltage of no greater than 4.0 Vdc. A clamp diode, such as a 1N4148, should be installed across the relay coil. An external transistor can be used to drive heavier loads (e.g., electro-mechanical relays). $\overline{TALK}$ is controlled by the host setting the RB bit. In a typical application, $\overline{TALK}$ is connected to the normally closed Talk/Data relay. In this case, TALK active opens the relay to disconnect the handset from the telephone line.
		SPEAKER INTERFACE
SPKR	O(DF)	**Speaker Analog Output.** The SPKR output reflects the received analog input signal. The SPKR on/off and three levels of attenuation are controlled by bits in DSP RAM. When the speaker is turned off, the SPKR output is clamped to the voltage at the VC pin. The SPKR output can drive an impedance as low as 300 ohms. In a typical application, the SPKR output is an input to an external LM386 audio power amplifier.
		DIAGNOSTIC SIGNALS Three signals provide the timing and data necessary to create an oscilloscope quadrature eye pattern. The eye pattern is simply a display of the received baseband constellation. By observing this constellation, common line disturbances can usually be identified.
EYEXY	OA	**Serial Eye Pattern X/Y Output.** EYEXY is a serial output containing two 15-bit diagnostic words (EYEX and EYEY) for display on the oscilloscope X axis (EYEX) and Y axis (EYEY). EYEX is the first word clocked out; EYEY follows. Each word has 8-bits of significance. Each 15-bit data word is shifted out most significant bit first with the seven most significant bits set to zero. EYEXY is clocked by the rising edge of EYECLK. This serial digital data must be converted to parallel digital form by a serial-to-parallel converter and then to analog form by two digital-to-analog (D/A) converters.
EYECLK	OA	**Serial Eye Pattern Clock.** EYECLK is a 288 kHz output clock for use by the serial-to-parallel converters. The low-to-high transitions of RDCLK coincide with the low-to-high transitions of EYECLK. EYECLK, therefore, can be used as a receiver multiplexer clock.
EYESYNC	OA	**Serial Eye Pattern Strobe.** EYESYNC is a strobe for loading the D/A converters.

Table 2-3. Hardware Interface Signal Definitions (Cont'd)

Label	I/O Type	Signal/Definition
		REFERENCE SIGNALS AND MODEM INTERCONNECT - 68-PIN PLCC
VC	MI	**Low Voltage Reference.** Connect to analog ground through 10 µF (polarized, + terminal to VC) and 0.1 µF (ceramic) in parallel.
VREF	MI	**High Voltage Reference.** Connect to VC through 10 µF (polarized, + terminal to VREF) and 0.1 µF (ceramic) in parallel.
VREG	MI	**Voltage Regulator.** No connect. For pin compatibility with future modem data pumps, provide a printed circuit board connection to digital ground through 0.1 µF. This capacitor may be installed for this modem but is not required.
$\overline{\text{POR}}$	MI	**Power-On-Reset.** Connect to $\overline{\text{RESET}}$.
DSP_RESET	MI	**DSP Reset.** Connect to $\overline{\text{RES}}$.
$\overline{\text{RES}}$	MI	**Reset.** Connect to DSP_RESET.
DSP_IRQ	MI	**DSP Interrupt Request.** Connect to $\overline{\text{IRQ}}$.
$\overline{\text{IRQ}}$	MI	**Interrupt Request.** Connect to DSP_IRQ.
IA_CLKIN	MI	**IA Clock.** Connect to CLKIN.
CLKIN	MI	**Clock.** Connect to IA_CLKIN.
RMODE	MI	**Receiver Mode.** Connect to TMODE.
TMODE	MI	**Transmitter Mode.** Connect to RMODE.
		REFERENCE SIGNALS AND MODEM INTERCONNECT - 100-PIN PQFP (MD1) AND 80-PIN PQFP (MD2)
MD1: VC	MI	**Low Voltage Reference.** Connect to analog ground through 10 µF (polarized, + terminal to VC) and 0.1 µF (ceramic) in parallel.
MD1: VREF	MI	**High Voltage Reference.** Connect to VC through 10 µF (polarized, + terminal to VREF) and 0.1 µF (ceramic) in parallel.
MD2: VREG	MI	**Voltage Regulator.** No connect. For pin compatibility with future modem data pumps, provide a printed circuit board connection to digital ground through 0.1 µF. This capacitor may be installed for this modem but is not required.
MD1: $\overline{\text{POR}}$	MI	**Power-On-Reset.** Connect to MD1: $\overline{\text{RESET}}$.
MD1: MD2_RESET	MI	**DSP Reset.** Connect to MD2: RESETP.
MD1: MD2_IRQ	MI	**Interrupt Request.** Connect to MD2: IRQP.
MD1: MD1_CLKIN	MI	**IA Clock.** Connect to MD1: CLKIN.
MD1: CLKIN	MI	**Clock.** Connect to MD1: MD1_CLKIN.
MD1: MD1_SLEEP	MI	**Sleep.** Connect to MD1: $\overline{\text{SLEEP}}$.
MD1: $\overline{\text{SLEEP}}$	MI	**Sleep.** Connect to MD1: MD1_SLEEP.
MD1: AD0 - AD7	MI	**Data Lines.** Connect to MD2: D0 - D7.
MD1: A0 - A3, A13	MI	**Data Lines.** Connect to MD2: RS0 - RS4, respectively.
MD1: XCLK	MI	**X Clock.** Connect to MD2: XCLK.
MD1: YCLK	MI	**Y Clock.** Connect to MD2: YCLK.
MD1: RDP	MI	**Read.** Connect to MD2: READP.
MD1: WTP	MI	**Write.** Connect to MD2: WRITEP.
MD1: ES3	MI	**Chip Select.** Connect to MD2: CSP.
MD1: RMODE	MI	**Receiver Mode.** Connect to MD2: SR1IO.
MD1:TMODE	MI	**Transmitter Mode.** Connect to MD2: SR1IO.
MD1:TXDAT	MI	**Transmit Data.** Connect to MD2: SR4OUT.
MD1: RXOUT	MI	**Receive Data.** Connect to MD2: SR3IN.
MD1: TIRO2	MI	**Transmitter Data.** Connect to MD2: TIRO2.
MD1: TRESET	MI	**Transmitter Reset.** Connect to MD2: SA1CLK.
MD1: TSTROBE	MI	**Transmitter Stobe.** Connect to MD2: IA1CLK
MD2: GP0	MI	**Eye Sync.** Connect to MD2: EYESYNC.
MD2: XTALI	MI	**Crystal.** Connect to ground.
MD2: GP16-GP18	MI	**Not Used.** Connect to ground.

Table 2-4. Digital Interface Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input High Voltage	V_{IH}				Vdc	
Types IA and IB		2.0	–	V_{CC}		
Type ID		0.8(V_{CC})	–	V_{CC}		
Input High Current	I_{IH}	–	–	40	µA	V_{CC} = 5.25V, V_{IN} = 5.25V
Input Low Voltage	V_{IL}	0.3	–	0.8	Vdc	
Input Low Current	I_{IL}	–	–	400	µA	V_{CC} = 5.25V
Input Leakage Current	I_{IN}	–	–	±2.5	µA	V_{IN} = 0 to +5V, V_{CC} = 5.25V
Output High Voltage	V_{OH}				Vdc	
Type OA		3.5	–	–		I_{LOAD} = – 100 µA
Type OD		–	–	V_{CC}		I_{LOAD} = 0 mA
Output Low Voltage	V_{OL}				Vdc	
Type OA		–	–	0.4		I_{LOAD} = 1.6 mA
Type OB		–	-	0.4		I_{LOAD} = 0.8 mA
Type OD		–		0.75		I_{LOAD} = 15 mA
Three–State Input Current (Off)	I_{TSI}	–	–	±10	µA	V_{IN} = 0.4 to V_{CC} –1
Power Dissipation (RC96DPL/RC144DPL)	P_D				mW	
Normal mode		–	390	–		I = 78 mA, V_{CC} = 5.0V, T_A = 25°C
		–	–	525		I = 100 mA,V_{CC} = 5.25V, T_A = 0°C
		–	–	680		I = 130 mA,V_{CC} = 5.25V, T_A = -40°C
Sleep mode		–	10	–		I = 2 mA,V_{CC} = 5.0V, T_A = 25°C
		–	–	12.6		I = 2.4 mA,V_{CC} = 5.25V, T_A = 0°C
		–	–	16.3		I = 3.1 mA,V_{CC} = 5.25V, T_A = -40°C
Power Dissipation (RC96DPi/RC144DPi)	P_D				mW	
Normal mode		–	700	–		I = 140 mA, V_{CC} = 5.0V, T_A = 25°C
		–	–	925		I = 176 mA,V_{CC} = 5.25V, T_A = 0°C
		–	–	1050		I = 200 mA,V_{CC} = 5.25V, T_A = -40°C
Sleep mode		–	10	–		I = 2 mA,V_{CC} = 5.0V, T_A = 25°C
		–	–	12.6		I = 2.4 mA,V_{CC} = 5.25V, T_A = 0°C
		–	–	16.3		I = 3.1 mA,V_{CC} = 5.25V, T_A = -40°C

Table 2-5. Analog Interface Characteristics

Name	Type	Characteristic	Value
RIN	I (DA)	Input Impedance	> 70K Ω
		Voltage Range	2.5 ±1.6 V
TXA1, TXA2	O (DD)	Minimum Load	300 Ω
		Maximum Capacitive Load	0.01 µF
		Output Impedance	10 Ω
		Output Voltage	2.5 ± 1.6 V
		D.C. Offset	< 200 mV
SPKR	O (DF)	Minimum Load	300 Ω
		Maximum Capacitive Load	0.01 µF
		Output Impedance	10 Ω
		Output Voltage	2.5 ± 1.6 V
		D.C. Offset	< 20 mV

Table 2-6. Absolute Maximum Ratings

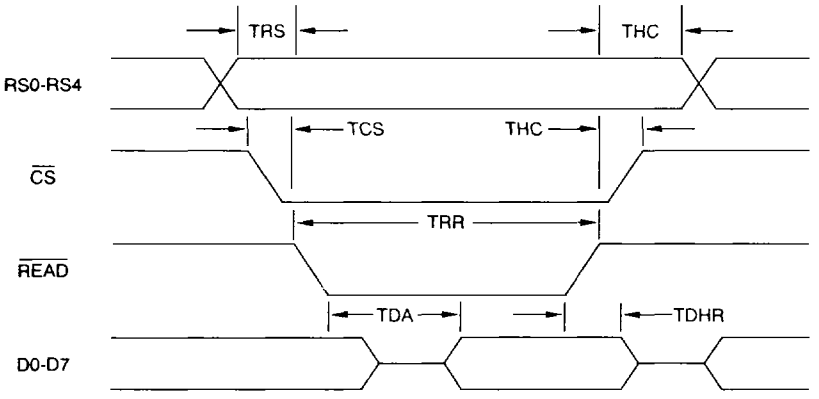
Parameter	Symbol	Limits	Units
Supply Voltage	V_{DD}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-0.5 to +5VD +0.5	V
Analog Inputs	V_{IN}	-0.3 to +5VA + 0.3	V
Voltage Applied to Outputs in High Impedance (Off) State	V_{HZ}	-0.5 to +5VD + 0.5	V
DC Input Clamp Current	I_{IK}	±20	mA
DC Output Clamp Current	I_{OK}	±20	mA
Static Discharge Voltage (25°C)	V_{ESD}	±3000	V
Latch-up Current (25°C)	I_{TRIG}	±200	mA
Operating Temperature Range	T_A		
Commercial		-0 to +70	°C
Industrial (E Model Number Suffix)		-40 to +85	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C

Table 2-7. Host Bus Interface Timing

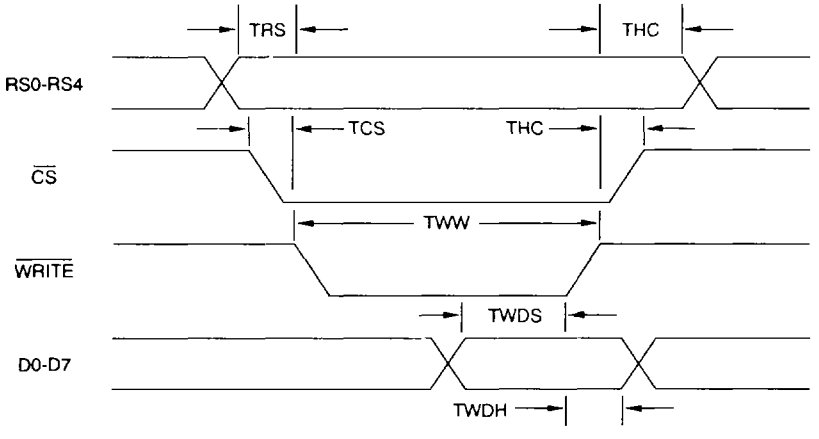
Parameter	Symbol	Min.	Max.	Units
a. Read				
Address Setup	TRS	10	–	ns
Chip Select Setup	TCS	0	–	ns
Control Hold	THC	10	–	ns
Read Data Access	TDA	-	35	ns
Read Data Hold	TDHR	10	–	ns
Read Pulse Width	TRR	45	–	ns

Table 2-7. Host Bus Interface Timing (Cont'd)

Parameter	Symbol	Min.	Max.	Units
b. Write				
Address Setup	TRS	10	–	ns
Chip Select Setup	TCS	0	–	ns
Control Hold	THC	10	–	ns
Write Data Setup	TWDS	10	–	ns
Write Data Hold	TWDH	10	–	ns
Write Pulse Width	TWW	45	–	ns



a. Host Bus Read



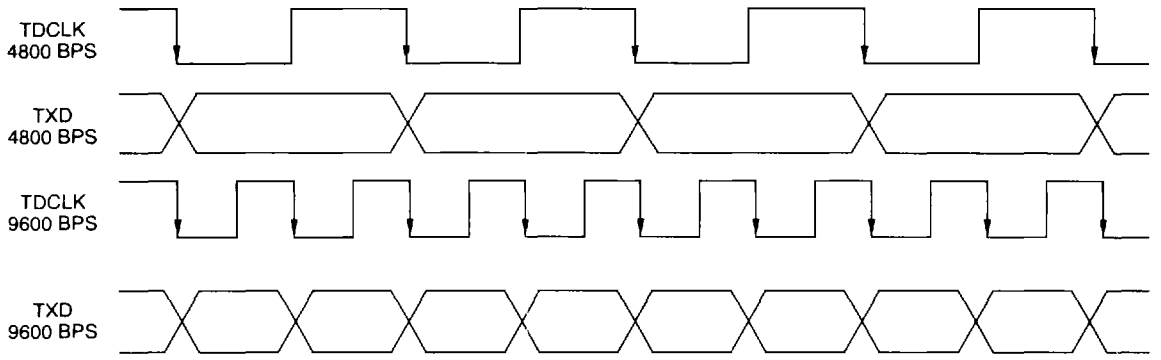
b. Host Bus Write

* A minimum delay of 3 times the YCLK cycle time (340 ns at 8.8 MHz) is required from the rising edge of WRITE to the falling edge of the next selected READ or WRITE.

A minimum delay of 20 ns is required from the rising edge of READ to the falling edge of the next selected READ or WRITE.

874F2-4

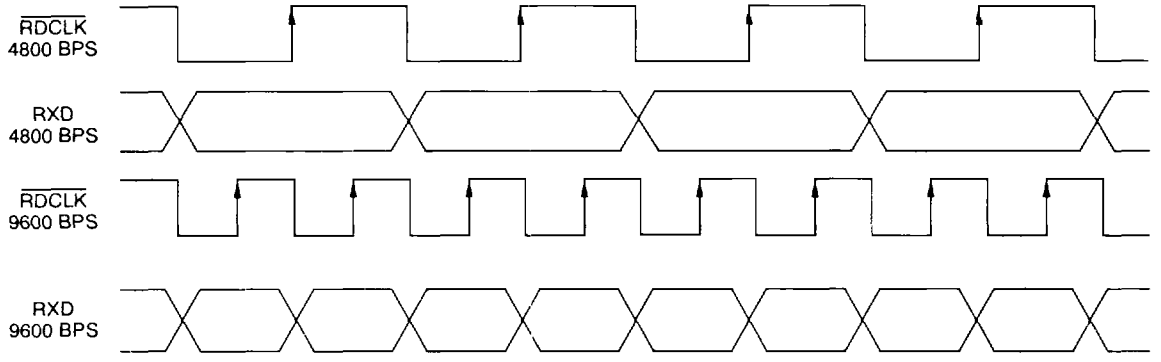
Figure 2-4. Host Bus Interface Waveforms



NOTE: THIS FIGURE IS VALID FOR SYNCHRONOUS MODE ONLY. THERE IS NO RELATIONSHIP BETWEEN TXD AND TDCLK IN ASYNCHRONOUS MODE.

a. Transmit

91643/858F24a



NOTE: THIS FIGURE IS VALID FOR SYNCHRONOUS MODE ONLY. THERE IS NO RELATIONSHIP BETWEEN RXD AND RDCLK IN ASYNCHRONOUS MODE

b. Receive

91643/858F24b

Figure 2-5. Serial Interface Waveforms

2.2 LINE TRANSFORMER REQUIREMENTS FOR V.32

V.32 bis/V.32 places high requirements upon the Data Access Arrangement (DAA) to the telephone line. V.32 bis/V.32 uses the same bandwidth for transmission of data in both directions. Any non-linear distortion generated by the DAA in the transmit direction (known as near-end echo) cannot be canceled by the modem's echo canceller and interferes with data reception. The designer must, therefore, ensure that the total harmonic distortion due to near-end echo at the RXA input to the modem is at least 30 dB below the minimum level of received signal at the same point.

Note that the major source of non-linear distortion in a DAA is the line transformer. Suitable line transformers are ETAL P2001 (–10 dB max.), MIDCOM 671-8236 (–10 dB max.), MIDCOM 671-8031 (0 dB max.), or equivalent.

When designing a DAA, the designer should take into account a worst case subscriber line, giving very poor matching to the DAA hybrid circuit and resulting in a large near-end echo. (To simulate worst case conditions it is suggested that an 1800 ohm resistor in series with a 0.47μF capacitor be used in place of the two-wire telephone line.)

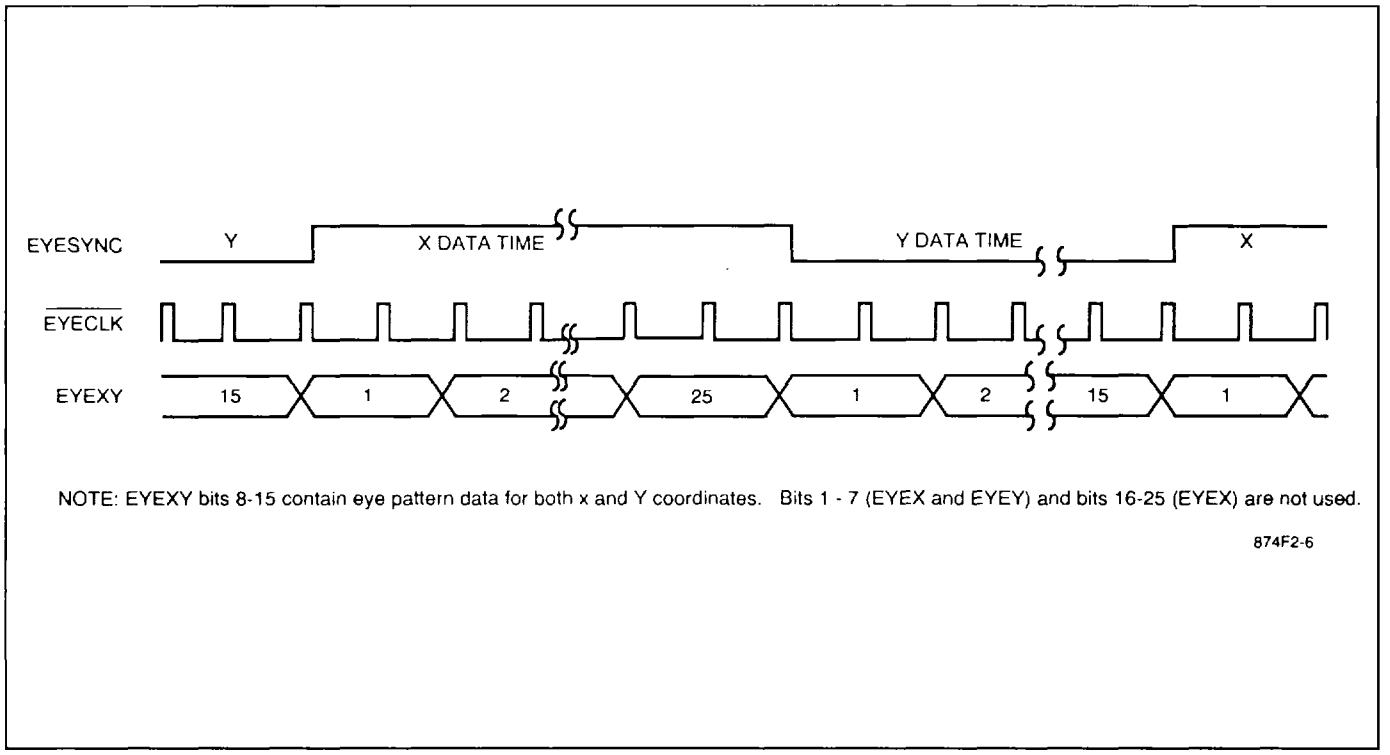


Figure 2-6. Eye Pattern Timing

3 SOFTWARE INTERFACE

Modem functions are implemented in firmware executing in the modem DSP.

3.1 INTERFACE MEMORY

The DSP communicates with the host processor by means of a dual-port, interface memory. The interface memory contains thirty-two 8-bit registers, labeled register 00 through 1F. Each register can be read from, or written into, by both the host and the DSP. The host communicates with the DSP interface memory via the microprocessor bus.

The host can control modem operation by writing control bits to DSP interface memory and writing parameter values to DSP RAM through the interface memory. The host can monitor modem operation by reading status bits from DSP interface memory and reading parameter values from DSP RAM through interface memory.

3.1.1 Interface Memory Map

An interface memory map of the 32 addressable registers in the modem is shown in Figure 3-1. These 8-bit registers may be read or written during any host read or write cycle. In order to operate on a single bit or a group of bits in a register, the host processor must read a register then mask out unwanted data. When writing a single bit or group of bits in a register, the host processor must perform a read-modify-write operation. That is, read the entire register, set or reset the necessary bits without altering the other register bits, then write the unaffected and modified bits back into the interface memory.

3.1.2 Interface Memory Bit Definitions

Table 3-1 defines the individual bits in the interface memory. In the Table 3-1 descriptions, bits in the interface memory are referred to using the format Z:Q. The register number is specified by Z (00 through 1F) and the bit number by Q (0 through 7, 0 = LSB).

Register	Bit							
	7	6	5	4	3	2	1	0
1F	NSIA	NCIA	—	NSIE	NEWS	NCIE	—	NEWC
1E	TDBIA	RDBIA	TDBIE	—	TDBE	RDBIE	—	RDBF
1D	MEACC	—	MEMW	MEMCR	MEMORY ACCESS ADDR HIGH B-8 (MEADDH)			
1C	MEMORY ACCESS ADDR LOW 7-0 (MEADDL)							
1B	EDET	DTDET	OTS	DTMFD	DTMFW			
1A	SFRES	RIEN	RION	DMAE	—	SCOBF	SCIBE	SECEN
19	MEMORY ACCESS DATA MSB F-8 (MEDAM)							
18	MEMORY ACCESS DATA LSB 7-0 (MEDAL)							
17	SECONDARY TRANSMIT BUFFER (SECTXB)/VOICE TRANSMIT LSB (VBUFTL)							
16	SECONDARY RECEIVE BUFFER (SECRXB)/VOICE RECEIVE LSB (VBUFRL)							
15	SLEEP	—	RDWK	HWRWK	AUTO	RREN	EXL3	EARC
14	ABCODE							
13	TLVL				RTH		TXCLK	
12	CONFIGURATION (CONF)							
11	BRKS	PARSL		TXV	RXV	V23HDX	TEOF	TXP
10	TRANSMIT BUFFER (TBUFFER)/VOICE TRANSMIT MSB (VBUFTM)							
0F	RLSD	FED	CTS	DSR	RI	TM	RTSDT	V54DT
0E	RTDET	BRKD	RREDT	V32BDT	SPEED			
0D	P2DET	PNDET	S1DET	SCR1	U1DET	SADET	TXFNE	HKAB
0C	AADET	ACDET	CADET	CCDET	SDET	SNDET	RXFNE	RSEQ
0B	TONEA	TONEB	TONEC	ATV25	ATBEL	—	V32DIS	EQMAT
0A	PNSUC	—	PE	FE	OE	CRCS/VSYNC	FLAGS	SYNCD
09	NV25	CC	DTMF	ORG	LL	DATA	RRTSE	DTR
08	ASYN	TPDM	V21S	V54T	V54A	V54P	RTRN	RTS
07	RDLE	RDL	L2ACT	DDIS	L3ACT	L4ACT	RA	MHLD
06	RTDIS	EXOS	CF17	HDLC	PEN	STB	WDSZ/DECBITS	
05	ECFZ	ECSQ	FECSQ	TXSQ	CEQ	TTDIS	STOFF	LECEN
04	RB	EQT2	V32BS	FIFOEN	EQFZ	NRZIEN	TOD	STRN
03	EPT	SEPT	—	RLSDE	ARC	SDIS	GTE	GTS
02	TDE	SQDIS	S511	—	RTSDE	V54TE	V54AE	V54PE
			DCDEN	CDEN	SDCDE	SCDE	CODBITS	
01	VOLUME		VPAUSE	—	—	TXHF	RXHF	RXP
00	RECEIVE BUFFER (RBUFFER)/VOICE RECEIVE MSB (VBUFRM)							

Note: — in the "Bit" columns indicates reserved for modem use only.

Figure 3-1. Modem Interface Memory Map

Table 3-1. Interface Memory Bit Definitions

Mnemonic	Location	Default	Name/Description
AADET	0C:7	–	**AA Detector.** When set, status bit AADET indicates that a V.32 bis/V.32 AA sequence has been detected. This bit is reset by the modem at the start of the CC sequence. This bit is not valid during rate renegotiation. (V.32 bis, V.32)
ABCODE	14:0–7	00	**Abort Code.** If the V.32 bis/V.32 handshake fails, status bit HKAB is set and an abort code is written into ABCODE. This code indicates the point in the handshake where the failure occurred. The abort code is not cleared by the modem but should be cleared by the host after it has been read. The abort codes and their meanings are listed in the table below. Refer to CCITT recommendations V.32 and V.32 bis for meanings of the signal mnemonics used. (V.32 bis, V.32) **Abort Code** — **Reason for Aborting** 01 — FED went off while waiting to get into round trip delay estimate. 10 — Unexpected E-sequence, do retrain. 81 — FED lost during round trip delay estimate. 82 — Lost track of AC/AA/CA/CC during round trip delay estimate. 84 — Timed out waiting for first S-sequence from ANS modem. 85 — Timed out waiting for second S-sequence from ANS modem. 86 — Timed out waiting for S-sequence from ORG modem. 8C — Lost FED during first TRN-sequence from ANS modem. 8D — Lost FED during second TRN-sequence from ANS modem. 8E — Lost FED during TRN-sequence from ORG modem. 90 — R1 not detected. 91 — R2 not detected. 92 — R3 not detected. 93 — R4/R5 not detected. 97 — E-sequence not detected.
ACDET	0C:6	–	**AC Detector.** Status bit ACDET = 1 indicates that a V.32 bis/V.32 AC sequence has been detected. This bit is reset by the modem when a CA sequence or an energy dropout is detected. This bit is not valid during rate renegotiation. Active when DTR = 1 and DATA = X or when DTR = 0 and DATA = 0. (V.32 bis, V.32)
ARC	03:3	1	**Automatic Rate Change Enable.** When control bit ARC is set, the modem will automatically condition itself to transmit data at the highest common rate negotiated during the V.32 bis/V.32 handshake. The host may specify the undefined bits in the rate sequence in DSP RAM. When ARC is reset, the modem cannot change from the rate it is configured to before beginning the handshake. However, it is possible for the host to interact with the rate sequences during the handshake and then set the transmitter configuration as desired. (V.32 bis, V.32) When control bit ARC is set, then setting the RTRN bit will cause the modem to send a rate change sequence rather than the normal retrain sequence. (V.22 bis) (See RTRN.)
ASYN	08:7	0	**Asynchronous/Synchronous.** When configuration bit ASYN is set, asynchronous mode is selected; when 0, synchronous mode is selected. When the ASYN bit changes from a 0 to a 1, the asynchronous to synchronous converter is configured according to the EXOS, PEN, STB and WDSZ bits at that time (EXOS, PEN, STB and WDSZ must be configured before ASYN changes from a 0 to a 1.) ASYN may be used to switch between synchronous and asynchronous modes only when RTS is OFF and TDBE = 1 in idle or data mode. Do not set this bit in V.21, V.23, or Bell 103 serial mode. Set this bit in V.21, V.23, or Bell 103 parallel mode. Note that the HDLC bit must be reset to 0 when ASYN is a 1. (V.32 bis, V.32, V.22 bis, V.22, Bell 212A)
ATBEL	0B:3	–	**Bell Answer Tone Detector.** When set, status bit ATBEL signifies that the modem receiver detected a 2225 Hz answer tone. The bit is set when the answer tone is detected, and is reset when the tone ends. ATBEL is active only when the DATA bit is reset and the modem is in originate mode. [Bell 212A, Bell 103, tone modes (CONF = 80h, 81h, or 83h)]

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
ATV25	0B:4	–	**V25 Answer Tone Detector.** When set, status bit ATV25 signifies that the modem receiver detected a 2100 Hz answer tone. The bit is set when the answer tone is detected, and is reset when the tone ends. ATV25 is only active when the DATA bit is reset before energy is present at RXA and the modem is in originate mode. [V.32 bis, V.32, V.22 bis, V.22, V.23, V.21, tone modes (CONF = 80h, 81h, or 83h)]
AUTO	15:3	0	**Automatic Mode Change Enable.** When control bit AUTO is set, the modem will automatically determine the communication standard of the remote modem and configure itself accordingly. (V.32 bis, V.32) The automode algorithm is based on the EIA/TIA PN-2330 specification. The possible operating modes are: V.32 bis/V.32, V.22 bis, V.22, Bell 212A, Bell 103, V.23 and V.21. Note that TONEB is not available for use by the host when automode function is used in answer mode To operate in automode, the modem must be configured to V.32 or V.32 bis in CONF, the AUTO bit must be set, and the DATA bit reset. Setting DTR or activating the DTR pin will then commence the handshake. The AUTO bit will reset and the DATA bit will set when the modem has determined the remote modem type. CONF will then contain the configuration code of the modem type found. It is recommended that the AUTO bit remain reset until answer tone has been detected when in originate mode. The automode function will select V.23 mode if the remote modem is configured for 1200 receive originate or 75 receive answer.
BRKD	0E:6	–	**Break Detected.** When set, status bit BRKD indicates the modem is receiving continuous space. When reset, continuous space is not being received.
BRKS	11:7	0	**Break Sequence.** When control bit BRKS is set in parallel asynchronous mode, the modem will send continuous space. When BRKS is reset, the modem will transmit parallel data from the TBUFFER. (This bit is valid only when TPDM = 1.)
CADET	0C:5	–	**CA Detector.** When set, status bit CADET indicates that a V.32 bis/V.32 CA sequence has been detected. This bit is reset by the modem when a AC sequence is detected. This bit is not valid during rate renegotiation. (V.32 bis, V.32)
CC	09:6	0	**Controlled Carrier.** When control bit CC is set, the modem operates in controlled carrier; when 0, the modem operates in constant carrier. Controlled carrier allows the modem transmitter to be controlled by the RTS pin or the RTS bit (see Table 1-2). When the RTS pin is asserted, or the RTS bit set, the transmitter immediately sends scrambled ones for 270 ms and then turns on the $\overline{\text{CTS}}$ signal and the CTS bit. (V.22 bis, V.22, V.23, Bell 212A)
CCDET	0C:4	–	**CC Detector.** When set, status bit CCDET indicates that a V.32 bis/V.32 CC sequence has been detected. This bit is reset by the modem when an energy dropout is detected. This bit is not valid during rate renegotiation. (V.32 bis, V.32)
CDEN	02:4	0	**Coder Enable.** When control bit CDEN is set in receive voice mode (CONF bits = 80, 81, 83, or 86, and RXV is set), the modem is in ADPCM receive mode and performs ADPCM coding. The coder output is placed into VBUFRM and VBUFRL voice receive buffer. (See CODBITS, RXV, and VSYNC.)
CEQ	05:3	1	**Compromise Equalizer Enable.** When control bit CEQ is set, the transmitter's digital compromise equalizer is inserted into the transmit path. This bandpass equalizer has host programmable taps in DSP RAM. CEQ should be reset during local analog loopback and in FSK modes to ensure uniform transmit levels for both mark and space frequencies. CEQ must be reset in ADPCM voice mode.
CF17	06:5	0	**Carrier Frequency 1700 Hz.** When a V.17 configuration is selected, control bit CF17 selects the carrier frequency (1 = 1700 Hz; 0 = 1800 Hz). Set NEWC to initiate the mode change. (V.17) The non-standard 1700 Hz option is provided for use with a secondary channel which is added at the high end of the band.

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
CODBITS	02:0-1	–	**Coder No. of Bits.** Defines the number of bits per sample (2, 3, or 4) used by the ADPCM coder in ADPCM receive mode (CONF = 80h, 81h, 83h, or 86h; CDEN = 1) (see CDEN): **Bit 1** **Bit 0** **Bits per Sample** 0 0 2 bits per sample 0 1 3 bits per sample 1 x 4 bits per sample
CONF	12:0–7	76	**Modem Configuration.** The CONF control bits select the modem configuration from the following: **Mode** **Data Rate** **CONF (Hex)** V.33 TCM 14400 31 V.33 TCM 12000 32 V.33 TCM 9600 34 V.33 TCM 7200 38 V.32 bis TCM 14400 76 V.32 bis TCM 12000 72 V.32 TCM 9600 74 V.32 9600 75 V.32 bis TCM 7200 78 V.32 4800 71 V.32 bis/V.32 clear down - 70 See Note 1. V.17 TCM 14400 B1 V.17 TCM 12000 B2 V.17 TCM 9600 B4 V.17 TCM 7200 B8 V.29 9600 14 V.29 7200 12 V.29 4800 11 V.27 ter 4800 02 V.27 ter 2400 01 V.26 bis 2400 08 V.26 bis 1200 04 V.26 A 2400 0C V.22 bis 2400 84 V.22 bis 1200 82 See Note 2. V.22 1200 52 V.22 600 51 V.21 0-300 A0 V.21 channel 2 300 A8 Bell 212A 1200 62 Bell 103 0-300 60 V.23 1200 TX/75 RX A4 V.23 75 TX/1200 RX A1 Transmit Single Tone — 80 See Notes 3 and 4. Transmit Dual Tone — 83 See Notes 3 and 4. Dialing/Calling Tone — 81 See Note 4. DTMF Receiver — 86 See Note 4. **NOTES:** 1. Configuration 70h transmits a V.32 bis/V.32 GSTN clear-down sequence. This may be sent during a retrain or a rate renegotiation. The remote modem will automatically detect the clear-down sequence and both modems will drop carrier at the end of the retrain or rate renegotiation. 2. Configuration 82h allows for possible fall forward to 2400 bps. 3. When single tone or dual tone mode is selected, the modem transmits one or two tones, respectively. The tone frequencies and levels are host programmable in DSP RAM. Single tone transmit uses the Dual Tone 1 frequency and level.

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
			NOTES (Cont'd): 4. Receive voice pass-through mode can run concurrently when RXV is set and CDEN is reset; transmit voice pass-through mode can run currently when TXV is set and DCDEN is reset. (See RXV and CDEN bits.) ADPCM receive mode can run concurrently when RXV is set and CDEN is set; transmit ADPCM mode can run concurrently when TXV is set and DCDEN is set. (See TXV and DCDEN bits.)
CRCS	0A:2	0	**CRC Sending**. When set, status bit CRCS indicates that the transmitter is sending the CRC (2 bytes) in HDLC (SDLC) mode. A 0 indicates that the CRC is not being sent. Either a 16-bit (default) or 32-bit CRC may be sent as selected by the CCITT CRC32 parameter in RAM (see parameter 52 in Section 4.4)
CTS	0F:5	–	**Clear To Send.** When set, status bit CTS indicates to the DTE that the training sequence has been completed and any data present at TXD (serial mode) or in TBUFFER (parallel mode) will be transmitted (see TPDM). CTS response times from an RTS ON or OFF transition after the modem has completed a handshake are shown in Table 2. The CTS OFF-to-ON response time is programmable in DSP RAM.
DATA	09:2	1	**Data.** When control bit DATA is reset, the modem is prevented from entering and proceeding with the handshake (start-up) sequence and will ignore all V.24 interface signals. This bit should be set by the host at a suitable time after completion of dialing or answering. Recommended procedure for originating a call in V.32 bis/V.32 using DATA: Reset both DATA and DTR. Establish a call. Detect answer tone using ATV25. After receiving answer tone for 1 second, set DTR. When ATV25 equals 0 AND ACDET equals 1, set DATA. The handshake will now proceed. **NOTE:** DATA should be set no later than 20 ms after detecting ACDET = 1 for compatibility with V.32 modems which send the minimum allowable AC length of 53.3 ms.
DCDEN	02:5	0	**Decoder Enable.** When control bit DCDEN is set in transmit voice mode (CONF bits = 80, 81, 83, or 86, and TXV is set), the modem is in ADPCM transmit mode and performs ADPCM decoding on the VBUFTM and VBUFTL voice transmit buffer contents. (See DECBITS and TXV.)
DDIS	07:4	0	**Descrambler Disable.** When control bit DDIS is set, the receiver's descrambler circuit is disabled; when reset, the descrambler circuit is enabled.
DECBITS	06:0-1	–	**Decoder No. of Bits.** Defines the number of bits per sample used by the ADPCM decoder in ADPCM transmit mode) (CONF = 80h, 81h, 83h, or 86h; DCDEN = 1): **1 0 Bits per Sample** 0 0 2 bits per sample 0 1 3 bits per sample 1 x 4 bits per sample
DMAE	1A:4	0	**DMA Signals Enabled.** When set to a 1, control bit DMAE converts the RI/ and DSR/ output lines to the TXRQ (Transmitter Request) and RXRQ (Receiver Request) output lines, respectively. TXRQ is a high active signal that follows the state of the TDBE bit and the RXRQ is a high active signal that follows the state of the RDBF bit. DMA is available in asynchronous, synchronous and HDLC modes. Bit FIFOEN must be set in asynchronous modes in order to obtain the RXRQ interrupt. (TPDM = 1)
DSR	0F:4	–	**Data Set Ready.** When set (ON), status bit DSR indicates that the modem is in the data transfer state. When reset (OFF), DSR indicates that the DTE is to disregard all signals appearing on the interchange circuits except $\overline{RI}$. DSR will switch to the OFF state when the modem is in a test mode.

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
DTDET	1B:6	–	**Dual Tone Detected.** When configured as a DTMF receiver (CONF = 86h), the modem sets status bit DTDET when a signal is received that satisfies all DTMF criteria except on-time, off-time, and cycle-time. The encoded DTMFW Output Word (1B:0-3) value is available when DTDET is set. If the received signal is a valid DTMF signal, then DTDET will be set following EDET is set. The DTDET bit is reset by the modem after DTMFD is set or if the received signal fails to satisfy any subsequent DTMF criteria.
DTMF	09:5	1	**DTMF Select.** When the modem is configured for dialing mode (CONF = 81h, the modem will dial using DTMF tones or pulses. When control bit DTMF is set, the modem will dial using DTMF tones. When DTMF is reset, the modem will dial using pulses. The DTMF bit can be changed during the dialing process to allow either tone or pulse dialing of consecutive digits. When in dialing mode, the data placed in the Transmit Data Buffer is treated as digits to be dialed. The number to be dialed must be represented by two hexadecimal digits (e.g., if a 9 is to be dialed, then a 09 must be written to the Transmit Data Buffer). Also, see TDBE bit. Dialing timing and power levels are host programmable in DSP RAM (Table 4-1). Pulse dialing defaults to the $\overline{\text{OHRC}}$ output. The pulse dialing output is controlled by bit 6 in RAM address 0D4h (0 = $\overline{\text{OHRC}}$ output; 1 = $\overline{\text{TALK}}$ output) when in dial mode. The output may be selected using RAM access method 1 (see Section 4).
DTMFD	1B:4	–	**DTMF Signal Detected.** When configured as a DTMF receiver (CONF = 86h), the modem sets status bit DTMFD when a DTMF signal has been detected that satisfies all specified DTMF detect criteria. The host must reset this bit after reading the DTMFW Output Word (1B:0-3), otherwise two or more detections of the same symbol may be missed by the host.
DTMFW	1B:0-3	–	**DTMF Output Word.** When the modem is configured as a DTMF receiver and a DTMF tone is present such that status bit DTDET is set by the modem, the encoded DTMF output is written into 1B:0-3. The DTMF symbol codes are: **DTMF Symbol / Encoded Output (Hex) / DTMF Symbol / Encoded Output (Hex)** 0 / 0 / 8 / 8 1 / 1 / 9 / 9 2 / 2 / * / A 3 / 3 / # / B 4 / 4 / A / C 5 / 5 / B / D 6 / 6 / C / E 7 / 7 / D / F
DTR	09:0	0	**Data Terminal Ready.** In V.32 bis/V.32, V.22/V.22 bis, and Bell 212A modes, setting control bit DTR initiates a handshake sequence, providing DATA bit is set. If in answer mode, the modem will immediately send answer tone. In V.21, V.23, and Bell 103 modes, DTR must be set for the modem to enter data state providing DATA bit is set. If in answer mode, the modem will send answer tone. In these configurations, if controlled carrier is selected, the carrier is controlled by the RTS pin or RTS bit. In V.21 channel 2 mode, DTR must be set in order to receive data. During the data mode, resetting DTR will cause the transmitter to turn off. The DTR bit parallels the operation of the hardware $\overline{\text{DTR}}$ control input. These inputs are ORed by the modem.

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
EARC	15:0	1	**Extended Automatic Rate.** When control bit EARC is set and V32BS is reset (and ARC is set), then rate changes to the proprietary V.32/12000 and V.32/7200 TCM configurations are allowed during the V.32 handshake. The modem will condition itself to transmit data at the highest common rate negotiated during the V.32 handshake. These rates include the proprietary 12000 and 7200 TCM configurations, if both calling and answering modems support these configurations. Setting EARC is not required for V.32 bis operation (i.e., when V32BS = 1). When EARC is reset, then rate changes are only allowed to standard V.32 bis/V.32 configurations. For example, if the modem is configured for V.32 bis/12000, it will not connect at 12000 bps if handshaking with a proprietary 12000 bps V.32 modem (not V.32 bis) unless the EARC bit is set. There are two methods for operating in the proprietary V.32/12000 and V.32/7200 TCM configurations. The first is to reset bits ARC, V32BS, and EARC. CONF should then be loaded for the required configuration. The modem will then only be able to connect in the configuration selected. Both calling and answering modems have to be configured the same way for a successful connection. The second method is to set bits ARC and EARC. CONF should be loaded as desired, but in this case rate negotiation takes place during the V.32 handshake. Use of this method allows fallback or fall-forward retrains in 2400 bps steps from 12000 bps to 4800 bps. In order to change the rate to a proprietary configuration, the modem uses two bits (B9 and B10) in the V.32 16-bit rate sequence that are undefined in CCITT Recommendation V.32. The host must set the NEWC bit after changing EARC. (V.32)
ECFZ	05:7	0	**Echo Canceller Freeze.** When control bit ECFZ is set, the updating of the echo canceller taps is inhibited. (V.32 bis, V.32)
ECSQ	05:6	0	**Echo Canceller Squelch.** When control bit ECSQ is set, the echo canceller output is forced to zero. (V.32 bis, V.32)
EDET	1B:7	–	**DTMF Early Detection.** When configured as a DTMF receiver (CONF = 86h), the modem sets status bit EDET after the DTMF signal energy is detected to indicate that the received signal is probably a DTMF signal. This bit is reset by the modem after DTMFD is set or if the received signal fails to satisfy any subsequent DTMF criteria.
EPT	03:7	0	**Echo Protector Tone Enable.** When control bit EPT is set, an unmodulated carrier is transmitted for 185 ms (SEPT = 0) or 30 ms (SEPT = 1) followed by 20 ms of no transmitted energy prior to the transmission of the training sequence. When EPT is reset, neither the echo protector tone nor the 20 ms of no energy are transmitted prior to the transmission of the training sequence. (V.17, V.29, V.27) The echo protector tone is typically used in V.27 ter and V.29 over dial-up lines. The tone is sent prior to the training sequence to ensure that the echo suppressors are pointing in the correct direction.
EQFZ	04:3	0	**Equalizer Freeze.** When control bit EQFZ is set, updating of the receiver's adaptive equalizer taps is inhibited.
EQMAT	0B:0	0	**EQM Above Threshold.** Status bit EQMAT indicates that the measured EQM is above (1) or not above (0) the threshold value programmed in DSP RAM.
EQT2	04:6	1	**Equalizer T/2 Spacing Select.** When control bit EQT2 is set, the receiver's adaptive equalizer is T/2 fractionally spaced. When EQT2 is reset, the equalizer is T spaced (T = 1 baud time). The use of T/2 is recommended in V.32 bis/V.32 over lines with severe amplitude distortion.
EXL3	15:1	0	**External Loop 3 Selector.** When control bits L3ACT and EXL3 are both set, the signal path for local analog loopback is external to the modem (by connecting TXA and RXA together). When L3ACT is set but EXL3 is reset, the local analog loop signal path is internal to the modem. (This bit is useful for measuring the transmit spectrum in V.32 and V.22 bis modes, without having to connect to a remote modem.) (See L3ACT.)

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
EXOS	06:6	0	**Extended Overspeed.** When control bit EXOS is set, Extended Overspeed mode is selected in the async-to-sync converter and in the sync-to-async converter. This bit must be configured appropriately before the ASYN bit changes from a 0 to a 1 for asynchronous mode. (V.32 bis, V.32, V.22 bis, V.22, Bell 212A)
FE	0A:4	0	**Framing Error.** When set, status bit FE indicates that more than 1 in 8 (or 1 in 4 for extended overspeed) characters were received without a Stop bit in asynchronous mode or an ABORT sequence was detected in SDLC/HDLC synchronous mode. When reset, no framing error is detected.
FECSQ	05:5	0	**Far Echo Canceller Squelch.** When control bit FECSQ is set, the output of the far-end echo canceller is forced to zero; the near-end echo canceller continues to operate normally. (V.32 bis, V.32) Squelching the far end echo canceller should only be done for testing purposes to manually characterize the far end echo.
FED	0F:6	–	**Fast Energy Detector.** When status bit FED is set, energy in the passband above the selected receiver threshold has been detected (see RTH). DTR must be on in order for FED to function in full duplex modes (DATA = 1).
FIFOEN	04:4	0	**Transmit FIFO Enable.** When control bit FIFOEN = 1, the host can input up to nine bytes of data through TBUFFER using the TDBE bit as a software interrupt or the TXRQ signal (DMAE = 1) as a DMA request interrupt. When the Transmit FIFO is enabled, the modem will service the host data within approximately 3 μs from the last data input until the FIFO is full. When FIFOEN = 0, the modem accepts host data at one-byte intervals. The Receive FIFO is always enabled. The host may wait up to nine byte-times before reading the data in RBUFFER. The modem will set bit OE upon receiving the tenth byte (causing the first data byte to be lost) if the host has not read the RBUFFER at least once during the preceding nine byte-times. The RDBF bit or RXRQ signal (DMAE = 1) signals the availability of receive data to the host. The modem will service the host within 3 μs from the last data output until the Receive FIFO is empty. (TPDM = 1)
FLAGS	0A:1	0	**Flag Sequence.** When set, status bit FLAGS indicates that the transmitter is sending the Flag sequence in SDLC/HDLC mode, or a constant mark in parallel asynchronous mode. When reset, FLAGS indicates that the transmitter is sending data.
GTE	03:1	0	**Guard Tone Enable.** When set, control bit GTE causes the specified guard tone to be transmitted (by the answering modem only) according to the state of the GTS bit. (V.22 bis, V.22)
GTS	03:0	0	**Guard Tone Select.** When set, control bit GTS selects the 550 Hz tone; when reset, GTE selects the 1800 Hz tone. The selected guard tone will be transmitted only when GTE is enabled. The host must set NEWC after changing the GTS bit. (V.22 bis, V.22)
HDLC	06:4	0	**HDLC Select.** When control bit HDLC is set, HDLC operation is enabled. When HDLC is reset, HDLC operation is disabled. The ASYN bit must be 0 and the TDBE bit must be 1 prior to setting HDLC to a 1. The HDLC bit is valid only in synchronous parallel data mode (ASYN = 0 and TPDM = 1). Not valid in FSK modes except V.21 channel 2. RTS must be off before switching in or out of HDLC mode while in DATA mode.
HKAB	0D:0	–	**Handshake Abort.** When set status bit HKAB indicates that the V.32 bis/V.32 handshake has failed. If transmitting, the transmitter remains in an abort state for 1 second after which HKAB is reset and the transmitter returns to idle mode. While in the abort state the transmitter output is silent. If receiving, the receiver remains in an abort state for 0.5 seconds after which HKAB is reset and the receiver returns to idle mode. At the same time an abort code is written into ABCODE (see ABCODE). (V.32 bis, V.32)

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
HWRWK	15:4	1	**Host Write Wake up.** When control bit HWRWK is set and the modem is in sleep mode, a host write to any register with the exception of 1D:0-7, will bring the modem out of sleep mode. (See SLEEP bit.)
L2ACT	07:5	0	**Loop 2 Activate.** When control bit L2ACT is set, the receiver's digital output is connected to the transmitter's digital input (locally activated remote digital loopback) in accordance with V.54. (Not valid in FSK modes.)
L3ACT	07:3	0	**Loop 3 Activate.** When control bit L3ACT is set, the transmitter's analog output is coupled internally to the receiver's analog input through an attenuator (local analog loopback) in accordance with CCITT Recommendation V.54. Optionally, the signal path for loop 3 can also be established externally to the modem (see EXL3). The modem may only be placed into loop 3 mode when in idle mode ($\overline{DTR}$ signal is OFF and the DTR bit is reset). NEWC must be set after any change in the L3ACT bit. The loopback is then completed (terminated) by asserting $\overline{DTR}$ signal ON (OFF) or setting the DTR bit. The transmitter's compromise equalizer should be disabled, by resetting CEQ, during local analog loopback.
L4ACT	07:2	0	**Loop 4 Activate.** Control bit L4ACT is used to cause the receiver's analog input to be connected internally to the transmitter's output (remote analog loopback) per V.54. (V.17, V29, V27). (Leased line device only.)
LECEN	05:0	1	**Listener Echo Canceller Enable.** When set , control bit LECEN enables the listener echo canceller in the receiver and reduces the transmit compromise equalizer from 40 taps to 5 taps. The use of this bit improves the V.32/V.32bis performance over lines exhibiting listener echo. The original 40-tap transmitter compromise equalizer may be manually restored by rewriting the coefficients into DSP RAM after LECEN has been reset or by performing a hardware or software power-on reset. NEWC must be set after changing the state of LECEN. (V.32, V.32bis)
LL	09:3	0	**Leased Line.** When control bit LL is set, the modem is in leased line operation; when 0, the modem is in switched line operation. When LL is set and the CC bit is reset, the modem immediately sends scrambled ones and goes into data mode. A retrain may be required after the initial connection. (V.22 bis, V.22) **NOTE:** Do not set LL for V.32 bis/V.32 leased line operation. Just set DTR = 1 and DATA = 1. The data pump will continuously send AA (originate) or AC (answer) pattern until the remote modem is detected. Note that the DATA bit need not be set until the remote AA or AC pattern has been detected. If desired, set the NV25 bit to prevent answer tone from being sent in answer mode.
MEACC	1D:7	0	**Memory Access Enable.** When control bit MEACC is set, the DSP accesses the RAM associated with the address in MEADDH and MEADDL. The MEMW bit determines if a read or write is performed. The DSP resets the MEACC upon RAM access completion.
MEADDL	1C:0–7	00	**Memory Access Address Low (7-0).** MEADDL contains the lower 8 bits (bits 7-0) of the address used to access modem RAM via the memory access data LSB (18) and MSB (19) registers. (See Table 3-2.)
MEADDH	1D:0–3	0	**Memory Access Address High (B-0).** MEADDH contains the upper 8 bits (bits B-8) of the address used to access modem RAM via the memory access data LSB (18) and MSB (19) registers. (See Table 4-1.)
MEDAL	18:0–7	00	**Memory Data LSB.** MEDAL is the least significant byte (bits 7-0) of the 16-bit data word used in reading or writing data locations in modem RAM.
MEDAM	19:0–7	00	**Memory Data MSB.** MEDAM is the most significant byte (bits F-8) of the 16-bit data word used in reading or writing data locations in modem RAM.

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
MEMCR	1D:4	0	**Memory Continuous Read.** When set to a 1, control bit MEMCR instructs the DSP to automatically update the data in MEDAM and MEDAL based on the RAM address in MEADDH and MEADDL. without the host having to set the MEACC bit. The modem will set the NEWS bit to a 1 when new data is available.
MEMW	1D:5	0	**Memory Write.** When MEMW is set and MEACC is set, the DSP copies data from the interface memory data registers MEDAL (18) and MEDAH (19) into the memory location addressed by MEADDL and MEADDH. When control bit MEMW is reset and MEACC is set, the DSP reads memory at the location addressed by MEADDL and MEADDH. The read data is stored into interface memory data registers MEDAL (18) and MEDAH (19).
MHLD	07:0	0	**Mark Hold.** When control bit MHLD is set, the transmitter's digital input data is clamped to a mark. When MHLD is reset, the transmitter's input is taken from TXD or TBUFFER (see TPDM).
NCIA	1F:6	–	**NEWC Interrupt Active.** When the new configuration chip 0 interrupt is enabled (NCIE is set) and a new configuration is implemented (NEWC is reset), the modem asserts IRQ and sets status bit NCIA to indicate that NEWC being reset caused the interrupt. NCIA and the interrupt request due to NEWC are cleared by the host writing a 0 into NCIE. (See NEWC and NCIE.)
NCIE	1F:2	0	**NEWC Interrupt Enable.** When control bit NCIE is set (interrupt enabled), the modem will assert IRQ and set NCIA when the NEWC bit is reset by the modem. When NCIE is reset (interrupt disabled), NEWC has no effect on IRQ or NCIA. (See NEWC and NCIA.)
NEWC	1F:0	0	**New Configuration.** Control bit NEWC must be set by the host after the host changes the configuration code in CONF (register 12), TLVL (13:4-7), RTH (13:2,3), LECEN (05:0), SFRES (1A:7), LL (09:3), L3ACT (07:3), ORG(09:4), GTS (03:0), GTE (03:1), EARC (15:0), CF17 (06:5), V32BS (04:5), V23HDX (11:2), TXV (11:4), RXV (11:3), SLEEP (15:7), V21S (08:5), or EQT2 (04:6) bits. This informs the modem to implement the new configuration. The modem resets the NEWC bit when the configuration change is implemented. A configuration change can also cause IRQ to be asserted. (See NCIE and NCIA.)
NEWS	1F:3	–	**New Status.** When set, status bit NEWS indicates that one or more status bits located in registers 0A–0F, 1A, or 1B have changed state, or a DSP RAM read or write has been completed. This bit can be reset only by the host. The host may mask the effect of individual status bits upon NEWS by writing a mask value to DSP RAM (see Function 17 in Section 4). When set, this bit can cause IRQ to be asserted. (See NSIE and NSIA.) **NOTE:** When read/modifying register 1F, set NEWS = 1 to ensure that the host does not reset NEWS after the modem DSP has set NEWS during read/modify. If NEWS = 0, setting NEWS to a 1 will not be accepted by the DSP and NEWS will remain a 0.
NRZIEN	04:2	0	**NRZI Enable.** When set, control bit NRZIEN enables NRZI transmitter encoding and receiver decoding in all synchronous and HDLC modes. When NRZIEN is reset, NRZ encoding and decoding is used.
NSIA	1F:7	–	**NEWS Interrupt Active.** When the new status interrupt is enabled (NSIE is set) and a change of status occurs (NEWS is set), the modem asserts IRQ and sets status bit NSIA to indicate that NEWS being set caused the interrupt. NSIA and the interrupt request due to NEWS are cleared when the host writes a 0 to NEWS. (See NEWS and NSIE.)
NSIE	1F:4	0	**NEWS Interrupt Enable.** When control bit NSIE is set (interrupt enabled), the modem will assert IRQ and set NSIA when NEWS is set by the modem. When NSIE is reset (interrupt disabled), NEWS has no effect on IRQ or NSIA. (See NEWS and NSIA.)
NV25	09:7	0	**No V.25 Answer Tone.** When control bit NV25 is set, the modem will not transmit the 2100 Hz CCITT answer tone when a handshake sequence is initiated and the modem is in answer mode. (V.32 bis, V.32, V.22 bis, V.22, V.23, V.21) (Not valid in AUTO mode.)

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
OE	0A:3	0	**Overrun Error.** When set, status bit OE indicates that the Receiver Data Buffer (RBUFFER) was loaded from the RXA input before the host read the old data from RBUFFER. When reset, RBUFFER was read before new receive data was loaded into RBUFFER. This is valid for both ASYNC mode (ASYN = 1) and SDLC/HDLC mode.
ORG	09:4	0	**Originate.** When configuration bit ORG is set, the modem is in originate mode; when reset, the modem is in answer mode. Since this is a configuration bit, the NEWC bit must be set after any change in the ORG bit.
OTS	1B:5	–	**DTMF On-Time Satisfied.** When configured as a DTMF receiver (CONF = 86h), the modem sets status bit OTS after the on-time criteria is satisfied. This bit is reset by the modem after DTMFD is set or if the received signal fails to satisfy the DTMF off-time criteria.
P2DET	0D:7	0	**P2 Sequence Detected.** When status bit P2DET is set, the modem is detecting the P2 portion of the training sequence. When P2DET is reset, P2 is not being detected. (V.17, V.29. V.27)
PARSL	11:5, 6	00	**Parity Select.** Control bits PARSL select the method by which parity is generated and checked during the asynchronous parallel data mode (ASYN = 1). The options are: **6 5 Parity Selected** 0 0 Stuff Parity ("9th Data Bit") (see TXP, RXP) 0 1 Space Parity 1 0 Even Parity 1 1 Odd Parity
PE	0A:5	0	**Parity Error.** When set, status bit PE indicates that a character with bad parity was received in the asynchronous mode, or bad CRC was detected in the SDLC/HDLC synchronous mode. When reset, a character with good parity was received.
PEN	06:3	0	**Parity Enable.** When control bit PEN is set, parity is enabled in asynchronous mode. This bit must be configured appropriately before the ASYN bit changes from a 0 to a 1 for asynchronous mode. (V.32 bis, V.32, V.22 bis, V.22, Bell 212A)
PNDET	0D:6	–	**PN Sequence Detected.** Status bit PNDET indicates that the PN portion of the training sequence is being detected (set) or is not being detected (reset). (V.17, V.29. V.27)
PNSUC	0A:7	–	**PN Success.** When status bit PNSUC is set, the modem has successfully trained at the end of the PN portion of the high speed training sequence. When PNSUC is reset, a successful training has not occurred. (V.17, V.29. V.27)
RA	07:1	0	**Relay A Activate.** When control bit RA is set, the $\overline{\text{OHRC}}$ output is active; when reset, the $\overline{\text{OHRC}}$ output is off (high).
RB	04:7	0	**Relay B Activate.** When control bit RB is set, the $\overline{\text{TALK}}$ output is active; when reset, the $\overline{\text{TALK}}$ output is off (high).
RBUFFER	00:0–7	–	**Receive Data Buffer.** The host obtains channel data from the modem receiver in the parallel data mode by reading a data byte from the RBUFFER. The RBUFFER contains the received data when the RDBF bit is set. (See RDBF, RDBIE, and RDBIA.)
RDBF	1E:0	–	**Receive Data Buffer Full.** When set, status bit RDBF signifies that the receiver wrote valid data into RBUFFER (register 00). This condition can also cause IRQ to be asserted. The host reading RBUFFER resets the RDBF and RDBIA bits. (See RDBIE and RDBIA.)
RDBIA	1E:6	–	**Receive Data Buffer Interrupt Active.** When the receive data buffer interrupt is enabled (RDBIE is set) and RBUFFER (register 00) is written to by the modem (RDBF is set), the modem asserts IRQ and sets RDBIA to indicate that RDBF being set caused the interrupt. The host reading RBUFFER resets the RDBIA bit and clears the interrupt request due to RDBF. (See RDBF and RDBIE.)
RDBIE	1E:2	0	**Receive Data Buffer Interrupt Enable.** When control bit RDBIE is set (interrupt enabled), the modem will assert IRQ and set the RDBIA bit when RDBF is set by the modem. When RDBIE is reset (interrupt disabled), RDBF has no effect on IRQ or RDBIA. (See RDBF and RDBIA.)

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
RDL	07:6	0	**Remote Digital Loopback.** When set, control bit RDL causes the modem to initiate a V.22 bis request for the remote modem to go into digital loopback; RXD is clamped to a mark and the CTS bit and $\overline{CTS}$ signal will be reset in the local modem until the loop is established. The RDLE bit should be set before setting the RDL bit. (V.22 bis, V.22, Bell 212A/1200)
RDLE	07:7	1	**Remote Digital Loopback Response Enable.** When set, control bit RDLE enables the modem to respond to another modem's V.22 bis remote digital loopback request, thus going into loopback. When this occurs, the modem clamps RXD to mark; resets the CTS, DSR and RLSD bits, and turns the $\overline{CTS}$, $\overline{DSR}$ and $\overline{RLSD}$ signals to logic 1. The TM bit is set to inform the host of the test status. When the RDLE bit is reset, no response will be generated. (V.22 bis)
RDWK	15:5	1	**Ring Detect Wake up.** When control bit RDWK is set and the modem is in sleep mode, an incoming ring signal on the $\overline{RD}$ pin will bring the modem out of sleep mode. The $\overline{RD}$ pin must be normally low for the RDWK function to work. (See SLEEP bit).
RI	0F:3	–	**Ring Indicator.** When set, status bit RI indicates that a ringing signal is being detected. Ringing is detected if pulses are present on the $\overline{RD}$ input in the 15 Hz–68 Hz frequency range. The RI bit follows the ringing signal with a 1 during the ON time and a 0 during the OFF time coincident with $\overline{RI}$ output signal. The decision bounds are host programmable in DSP RAM. This bit is valid only when DATA bit is reset and is not applicable in tone modes.
RIEN	1A:6	0	**RION Enable.** When control bit is a 1, the RI output will reflect the RION bit. When a 0, the RI output follows the ringing signal on the RD input.
RION	1A:5	0	**Ring Indicator On.** Control bit RION determines the state of the RI output when bit RIEN is set and the DATA bit is reset. When RION is a 1, the RI output is driven low and when RION is a 0, the RI output is driven high.
RLSD	0F:7	–	**Received Line Signal Detector.** When status bit RLSD is set, the modem has finished receiving the training sequence or has turned on due to detected energy above threshold, and is receiving data. RLSD is reset when the modem is in the idle state and during the reception of a training sequence. The RLSD threshold may be adjusted in DSP RAM.
RLSDE	03:4	1	**RLSD Enable.** When control bit RLSDE is set, the $\overline{RLSD}$ pin reflects the RLSD bit state. When RLSDE is reset, the $\overline{RLSD}$ pin is clamped OFF and data is clamped to a mark regardless of the state of the RLSD bit..
RREDT	0E:5	–	**Rate Renegotiation Detected.** When set, status bit indicates a V.32 bis rate renegotiation sequence has been detected. RREDT will remain on until the host resets it. (V.32 bis, V.32)
RREN	15:2	0	**Rate Renegotiation.** When the modem is in V.32 bis data mode and control bit RREN is set, a rate negotiation sequence is initiated. RREN resets as soon as the initiation is acknowledged. The RREN bit should be used only if both the local and remote modems are V.32 bis. The V32BDT bit may be monitored during the handshake to determine if the remote modem is V.32 or V.32 bis. Fallback or fall-forward rate renegotiations may be accomplished in V.32 bis mode as follows: 1. Change CONF to the required configuration code. Note that the mode cannot be changed, only the data rate within a given mode. **Do not** set the NEWC bit. 2. Ensure that ARC bit is set. 3. Set the RREN bit. If the remote modem can operate at the requested rate, the configuration will be changed by the modem to reflect the new rate after the rate renegotiation is completed. If the remote modem cannot operate at the new rate and there are no common rates between the two modems, the modem will send a cleardown sequence and turn off RLSD. The CONF register will contain 70h to indicate that a cleardown was accomplished. If the rate renegotiation fails due to line conditions, the modem will try to complete the rate change by means of a retrain.

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
RRTSE	09:1	0	**Remote RTS Signaling Enable.** When control bit RRTSE is set and both the RTS bit and the RTS pin are inactive, the transmitter will send a pattern (idle pattern) produced by scrambling a binary 1 with the polynomial $1+x^{-3}+x^{-7}$. If RTS is deactivated and immediately reactivated, the modem will send approximately 144 bits of idle pattern before acknowledging the reactivation of RTS. When RRTSE is set and the RTS bit or the RTS pin is activated, the transmitter will immediately send a pattern of 8 bits (turn-on pattern) produced by scrambling a binary 0 with the polynomial $1+x^{-3}+x^{-7}$ followed by the user data. CTS is automatically delayed until the end of the 8-bit turn-on pattern. The RTS-CTS delay may be increased to allow the modem to transmit a period of mark after the 8-bit turn-on pattern in order to give the remote modem ample time to detect the turn-on and unclamp the receive data line. When control bit RRTSE is reset, remote RTS signaling is disabled and the RTS bit and RTS pin operate normally. This bit is not valid in FSK modes.
RSEQ	0C:0	0	**Rate Sequence Received.** When status bit RSEQ is set, the 16-bit rate sequence included in the CCITT V.32 bis/V.32 start-up procedure has been received and is available in RAM. RSEQ will remain set until reset by the host. (V.32 bis, V.32)
RTDET	0E:7	–	**Retrain Detector.** When set, status bit RTDET indicates that a training sequence has been detected (V.32 bis, V.32 or V.22 bis). This bit parallels the operation of the following: **Mode** — **Detector Bit** V.32 Originate — ACDET V.32 Answer — AADET V.22 bis — S1DET
RTDIS	06:7	0	**Receiver Training Disable.** When control bit RTDIS is set, the modem is prevented from recognizing a training sequence and entering the training state. When RTDIS is reset, receiver training is enabled. (V.17, V.29, V.27)
RTH	13:2,3	0	**Receiver Threshold.** The RTH control bits select the receiver energy detector threshold according to the following codes: **RTH** — **RLSD ON** — **RLSD OFF** 0 — – 43 dBm — – 48 dBm 1 — – 33 dBm — – 38 dBm 2 — – 26 dBm — – 31 dBm 3 — – 16 dBm — – 21 dBm The thresholds are programmable in DSP RAM (see Section 4).
RTRN	08:1	0	**Retrain.** When the modem is in V.32 bis, V.32, or V.22 bis data mode, and control bit RTRN is set, a retrain sequence is initiated. RTRN resets as soon as the initiation is acknowledged. Fallback or fall-forward retrains may be accomplished in V.32 bis, V.32, or V.22 bis modes as follows: 1. Change CONF to the required configuration code. Note that the mode cannot be changed, only the data rate within a given mode. (For example, it is not possible to fallback from V.32 to V.22 bis.) **Do not** set the NEWC bit. 2. Ensure that ARC bit is set. 3. If it is desired to fallback or fall-forward to one of the proprietary V.32 configurations, ensure that EARC is set. 4. Finally, set the RTRN bit. If the remote modem can operate at the requested rate, the configuration will be changed by the modem to reflect the new rate after the retrain is completed. If the remote modem cannot operate at the new rate and there are no common rates between the two modems, the modem will send a cleardown sequence and turn off RLSD. The CONF register will contain 70h to indicate that a cleardown was accomplished. If the modem reconfigures from V.22 bis 2400 bps to V.22 1200 bps during a handshake or as a result of a retrain, the CONF register will contain 82h.

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
RTS	08:0	0	**Request to Send.** When control bit RTS is set, the modem transmits any data on TXD (TPDM = 0) or TBUFFER (TPDM = 1) when CTS becomes active. In V.22 bis, V.22, V.23, V.21, and Bell 103 constant carrier and in V.32 bis/V.32 modes, RTS controls data transmission and DTR controls the carrier. For ease of use, RTS can be turned ON at the same time as DTR. In V.22 bis controlled carrier mode, RTS independently controls the carrier when DTR is ON. When RTS is turned ON, the modem then transmits 270 ms of scrambled 1s before turning CTS ON. In V.21, V.23, V.23 HDX, and Bell 103 controlled carrier modes, RTS independently controls the carrier when DTR is ON. When RTS is turned ON, CTS is turned ON per Table 2. The RTS bit parallels the operation of the RTS hardware control input. These inputs are ORed by the modem. (See descriptions of CTS and DTR bits.)
RTSDE	02:3	0	**Remote RTS Pattern Detector Enable.** When control bit RTSDE is set, the remote RTS pattern detector is enabled. RTSDE is available in synchronous and asynchronous modes. This bit is not valid in FSK modes. (See RTSDT).
RTSDT	0F:1	–	**Remote RTS Pattern Detected.** When set, status bit RTSDT indicates that the remote RTS signal is ON, otherwise it indicates that the remote RTS signal is OFF. This status bit is valid only when RTSDE is set. This status bit should be initialized by the host upon setting RTSDE. The modem will automatically activate/de-activate the local RLSD signal in response to a change in the remote RTS signal. Detection is available in synchronous and asynchronous modes. This bit is not valid in FSK modes.
RXHF	01:01	–	**Receiver FIFO Half Full.** When set, status bit RXHF indicates that there are 4 or more bytes in the 8-byte Receiver FIFO buffer. When reset, RXHF indicates that there are less than 4 bytes in the Receiver FIFO buffer. (TPDM = 1, FIFOEN = 1) An interrupt mask is available to allow an interrupt request to be generated when RXHF is set (see Function 17 in Section 4).
RXFNE	0C:1	-	**Receiver FIFO Not Empty.** When set, status bit RXFNE indicates that the receiver FIFO contains one or more bytes of data. When reset, bit RXFNE indicates that the receiver FIFO is empty. (TPDM = 1, FIFOEN = 1)
RXP	01:0	0	**Received Parity Bit.** This status bit is only valid when parity is enabled (PEN = 1), and word size is set for 8 bits per character (WDSZ = 11). In this case, the parity bit received (or ninth data bit) will be available at this location. The host must read this bit before reading the received data buffer (RBUFFER).
RXV	11:3	0	**Receive Voice.** When control bit RXV is set and CDEN bit is reset, receive voice pass-through mode is selected which allows the host to directly access to the A/D converter. The host can obtain 16-bit voice samples from VBUFRM and VBUFRL at the selected sample rate (7200 Hz default). VBUFRM and VBUFRL reflect the receive voice sample when bit RDBF is set. When control bit RXV is set and CDEN bit is set, the ADPCM coder is selected instead of receive voice pass-through mode. Sixteen data bits are received in VBUFRM and VBUFRL at the selected sample rate (7200 Hz default) and at the selected receive bits per sample (see CODBITS, CDEN, and VSYNC). Receive voice pass-through mode or ADPCM receive is available in tone modes only (CONF = 80h, 81h, 83h, or 86h). **Note:** Reading VBUFRM clears RDBF, therefore, VBUFRL (if used) must be read before VBUFRM.

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
S1DET	0D:5	–	**S1 Detector.** When set, status bit S1DET indicates that a V.22 bis S1 sequence has been detected. This bit is reset by the modem at the end of the S1 sequence. (V.22 bis)
S511	02:5	0	**Send 511.** When set, control bit S511 instructs the modem to generate and transmit a 511 pattern in the current configuration. If bit V54T, V54P, or V54A is set while bit S511 is set, the 511 pattern will be temporarily interrupted in order to transmit the chosen V54 sequence. For the modem to detect the 511 pattern, the host must first set up the sync time-out counter at address 0A5h using RAM access method 1 (see 4.2). The most significant bit enables or disables the 511 detection (1 = on) and bits 0-6 represent the sync time-out in byte times. A value of FFh in this location will enable the 511 detection and allow the maximum sync time-out. The 16-bit value read from address 0A7h contains the error count. Bits V54TE, V54PE, and V54AE must be reset in order for the 511 detection to function. (Synchronous modes only.)
SADET	0D:2	–	**Scrambled Alternating Sequence Detector.** When set, status bit SADET indicates that scrambled alternating data is being received. This bit is intended to be used for the automatic rate change sequence. (See ARC.) This bit is reset at the end of the alternating sequence. (V.22 bis)
SCDE	02:2	0	**Silence Coder Enable.** When control bit SCDE is set and the ADPCM coder is enabled in ADPCM receive mode (see CDEN), the modem performs silence detection and deletion.
SCIBE	1A:1	–	**Secondary Channel Input Buffer Empty.** When set, status bit SCIBE indicates that the secondary channel transmit buffer (SECTXB) is empty and ready for the next byte. The host must reset SCIBE after writing a new byte in SECTXB. See SECEN. (V.32 bis, V.32)
SCOBF	1A:2	–	**Secondary Channel Output Buffer Full.** When set, status bit SCOBF indicates that the secondary channel receive buffer (SECRXB) is full. The host must reset SCOBF after reading SECRXB. See SECEN. (V.32 bis, V.32)
SCR1	0D:4	–	**Scrambled Ones Detector.** When set, status bit SCR1 indicates that V.22 bis scrambled 1s have been detected during handshake. This bit is reset at the end of the scrambled 1s sequence. (V.22 bis, V.22, Bell 212)
SDCDE	02:3	0	**Silence Decoder Enable.** When control bit SDCDE is set ADPCM transmit mode (see DCDEN), the modem performs silence interpolation.
SDET	0C:3	–	**S Detector.** When set, status bit SDET indicates that a V.32 bis/V.32 S sequence has been detected. This bit is reset by the modem at the end of the S sequence. (V.32 bis, V.32)
SDIS	03:2	0	**Scrambler Disable.** When control bit SDIS is set, the transmitter scrambler circuit is disabled; when reset, the scrambler circuit is enabled.
SECEN	1A:0	0	**Secondary Channel Enable.** When control bit SECEN is set the secondary channel is enabled. When SECEN is reset the secondary channel is disabled. Bit SECEN may be set in idle mode or during the V.32 bis/V.32 handshake prior to RLSD turning on. The secondary channel may be turned on or off in data mode by setting or resetting the SECEN bit and performing a retrain. (V.32 bis, V.32) (Not supported at 4800 bps.)
SECRXB	16:0-7	–	**Secondary Receive Buffer.** The host obtains secondary channel data from the modem receiver by reading a data byte from the SECRXB. The SECRXB reflects the receive data when bit SCOBF is set. SECRXB is also used in voice mode (see RXV). (V.32 bis, V.32)
SECTXB	17:0-7	–	**Secondary Transmit Buffer.** The host conveys secondary channel output data to the transmitter by writing a data byte to the SECTXB. The SECTXB is ready for a new data byte when bit SCIBE is set. SECTXB is also used in voice mode (see TXV). (V.32 bis, V.32)
SEPT	03:6	0	**Short Echo Protector Tone.** When control bit SEPT is set, the echo protector tone duration is 30 ms; when reset, the echo protector tone duration is 185 ms. (V.17, V.29, V.27)
SFRES	1A:7	0	**Soft Reset.** When control bit SFRES is set to a 1, the modem will perform power-on reset processing. Bit SFRES will automatically be reset to a 0 by the modem upon completion of the reset processing. NEWC must be set to initiate the reset.

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
SLEEP	15:7	0	**Sleep Mode.** When control bit SLEEP is set, the modem is placed in sleep mode for reduced power consumption and the SLEEP pin is driven low. The modem can be awakened only if bit RDWK and/or HWRWK is set. If both RDWK and HWRWK are reset, only a power-on-reset will bring the modem out of sleep mode. The modem is reset upon wake up.
SNDET	0C:2	–	**S Negative Detector.** When set, status bit SNDET indicates that a V.32 bis/V.32 $\overline{S}$ sequence has been detected. This bit is reset at the end of the $\overline{S}$ sequence. (V.32 bis, V.32)
SPEED	0E:0–3	–	**Speed Indication.** The SPEED status bits indicate the receiver's data rate at the completion of a handshake. **Data Rate / SPEED (Hex)** 0–300: 0 600: 1 1200: 2 2400: 3 4800: 4 7200: 8 9600: 5 12000: 6 14400: 7
SQDIS	02:6	0	**Squarer Disable (Tone Detector C).** When control bit SQDIS is set, the squarer in front of tone detector C is disabled; when reset, the squarer is enabled. Disabling the squarer cascades the prefilter and filter C creating an 8th-order filter.
STB	06:2	0	**Stop Bit Number.** When control bit STB is reset, one stop bit is selected in asynchronous mode; when set, two stop bits are selected. This bit must be configured appropriately before the ASYN bit changes from a 0 to a 1 for asynchronous mode. (V.32 bis, V.32, V.22 bis, V.22, Bell 212A)
STOFF	05:1	0	**Soft Turn Off.** When control bit STOFF is set, the transmitter sends a tone at the end of a transmission in V.23, V.21, and Bell 103 configurations. This tone is detected as a mark frequency at the receiver. The soft turn off tone frequencies and durations are as follows: **Configuration / Frequency (Hz) / Duration (ms)** V.23/1200: 900 Hz, 7 ms V.21 Originate: 880 Hz, 30 ms V.21 Answer: 1550 Hz, 30 ms Bell 103 Originate: 1370 Hz, 30 ms Bell 103 Answer: 2325 Hz, 30 ms
STRN	04:0	0	**Short Train Select.** When a V.17 or V.27 configuration is selected in CONF, control bit STRN selects the training mode (1 = short train; 0 = long train). (V.17, V.27) STRN may be set only after the completion of a successful long train. STRN may be set or reset during data mode (RLSD on) or anytime before the start of the following training sequence. Setting STRN will inhibit the equalizer taps from being reset during the following short train thus allowing for a fast adaptation. A short train may be received only when STRN is set. Once STRN is set, the DATA bit must remain set and the only allowable configuration between V.17 and V.27 that will not alter the taps is V.21 Channel 2. (V.17, V.27)
SYNCD	0A:0	0	**Sync Pattern Detected.** When set, status bit SYNCD indicates that SDLC/HDLC flags (7E pattern) are being detected. When reset, the 7E pattern is not being detected. This bit is valid only in SDLC/HDLC mode (HDLC = 1). When HDLC = 0 and the modem is configured for V.17, V.29, or V.27, the SYNCD bit can be used by the host to detect V.21 Channel 2 flags. This is especially useful in fax modes where the modem must determine if the carrier is PSK or FSK.
TBUFFER	10:0–7	00	**Transmit Data Buffer.** The host conveys output data to the transmitter in the parallel mode by writing a data byte to the TBUFFER. Parallel data mode is available in both synchronous and asynchronous modes. The data is transmitted bit 0 first (see TDBE). **NOTE:** Do not read TBUFFER during data mode.

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
TDE	02:7	1	**Tone Detectors Enable.** When control bit TDE is set, tone detectors A, B, and C are enabled; when reset, tone detectors are disabled. TDE must be reset in ADPCM voice mode.
TDBE	1E:3	–	**Transmit Data Buffer Empty.** When set, status bit TDBE signifies that the modem has read TBUFFER (register 10) and the host can write new data into TBUFFER. This condition can also cause IRQ to be asserted. The host writing to TBUFFER resets the TDBE and TDBIA bits. If the host does not write new data into TBUFFER, the modem sends mark. TDBE must be a 1 before switching between synchronous, asynchronous, or HDLC modes. CTS must be on **before** data is loaded into TBUFFER. (See TDBIE and TDBIA.)
TDBIA	1E:7	–	**Transmit Data Buffer Interrupt Active.** When the transmit data buffer interrupt is enabled (TDBIE is set) and register 10 is empty (TDBE is set), the modem asserts IRQ and sets status bit TDBIA to indicate that TDBE being set caused the interrupt. The host writing to register 10 resets the TDBIA bit and clears the interrupt request due to TDBE. (See TDBIE and TDBE.)
TDBIE	1E:5	0	**Transmit Data Buffer Interrupt Enable.** When control bit TDBIE is set (interrupt enabled), the modem will assert IRQ and set the TDBIA bit when TDBE is set by the modem. When TDBIE is reset (interrupt disabled), TDBE has no effect on IRQ or TDBIA. (See TDBE and TDBIA.)
TEOF	11:1	0	**HDLC Transmit End of Frame.** When operating in HDLC with FIFOEN = 1, the host must set control bit TEOF to inform the transmitter that the corresponding data is the last byte in a frame. TEOF must be set prior to loading the last byte in TBUFFER. The modem will automatically reset TEOF. (HDLC = 1, TPDM = 1, FIFOEN = 1)
TLVL	13:4–7	9	**Transmit Level.** The TLVL code selects the transmitter analog output level at the TXA pin as follows: **TLVL Code (Hex) — TX Output Level (dBm ±0.5 dB)** 0 — –0.0 1 — –1.0 2 — –2.0 3 — –3.0 4 — –4.0 5 — –5.0 6 — –6.0 7 — –7.0 8 — –8.0 9 — –9.0 A — –10.0 B — –11.0 C — –12.0 D — –13.0 E — –14.0 F — –15.0 The host can fine tune the transmit level to a value lying within a 1 dB step by changing a value in DSP RAM.
TM	0F:2	–	**Test Mode.** When set, status bit TM indicates that the modem is in RDL test mode. (V.22 bis, V.22, Bell 212A)
TOD	04:1	0	**Train on Data.** When set, control bit TOD enables the train-on-data algorithm to converge the equalizer if the signal quality degrades. A BER of 10^{-3} for 0.5 seconds initiates the train-on-data. When TOD is reset, the modem can still recognize an incoming training sequence. (V.32 bis, V.32, V.17, V.29, V.27)
TONEA	0B:7	–	**Tone A Detected.** When set, status bit TONEA indicates that energy is present on the line within the tone detector A passband and above its threshold. The bandpass filter coefficients are host programmable in DSP RAM.
TONEB	0B:6	–	**Tone B Detected.** When set, status bit TONEB indicates that energy is present on the line within the tone detector B passband and above its threshold. The bandpass filter coefficients are host programmable in DSP RAM.

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
TONEC	0B:5	–	**Tone C Detected.** When set, status bit TONEC indicates that energy is present on the line within the tone detector C passband and above its threshold. The bandpass filter coefficients are host programmable in DSP RAM. The TONEC filter is preceded by a squarer in order to facilitate detection of difference tones. This squarer may be disabled with the SQDIS bit (see SQDIS bit).
TPDM	08:6	0	**Transmitter Parallel Data Mode.** When control bit TPDM is set, the modem accepts data for transmission from the TBUFFER (register 10) rather than the TXD input. (See TDBE and RTS.) **Note:** The TPDM bit must be set to a 1 in HDLC mode (HDLC bit = 1).
TTDIS	05:2	0	**Transmitter Training Disable.** When control bit TTDIS is set, the transmitter does not generate the training sequence at the start of transmission. With training disabled, the RTS/CTS delay is less than two baud times. (V.17, V.29, V.27)
TXCLK	13:0,1	0	**Transmit Clock Select.** The TXCLK control bits designate the origin of the transmitter data clock. **TXCLK** — **Transmit Clock** 0 — Internal 2 — External (XTCLK) 3 — Slave ($\overline{\text{RDCLK}}$) When the external clock is selected, an external clock **must** be supplied to the XTCLK input pin. The external clock signal must have a duty cycle of 50% and must be within ± 0.01% of the nominal TDCLK frequency (the actual frequency of TDCLK as measured when internal clock is selected). TDCLK will be phase locked to XTCLK when the external clock option is selected. When the slave clock is selected, the transmitter clock (TDCLK) is phase locked to the receiver clock ($\overline{\text{RDCLK}}$).
TXHF	01:02	–	**Transmitter FIFO Half Full.** When set, status bit TXHF indicates that there are four or more bytes in the 8-byte Transmitter FIFO buffer. When reset, TXHF indicates that there are less than four bytes in the Transmitter FIFO buffer. (TPDM = 1, FIFOEN = 1) An interrupt mask is available to allow an interrupt request to be generated when TXHF is set (see Function 17 in Section 4).
TXFNE	0D:1	-	**Transmitter FIFO Not Empty.** When set, status bit TXFNE indicates that the transmitter FIFO contains one or more bytes of data. When reset, bit TXFNE indicates that the transmitter FIFO is empty. (TPDM = 1, FIFOEN = 1)
TXP	11:0	0	**Transmit Parity Bit (or 9th Data Bit).** Control bit TXP contains the stuffed parity bit (or ninth data bit) for transmission when parity is enabled (PEN = 1), stuff parity is selected (PARSL = 00), and word size is set for 8 bits per character (WDSZ = 11). The host must load the stuffed parity bit (or 9th data bit) into TXP before loading the other 8 bits of data in TBUFFER.
TXSQ	05:4	0	**Transmitter Squelch.** When control bit TXSQ is set, the transmitter analog output is squelched. All other transmitter functions continue as normal. When TXSQ is reset, the transmitter output functions normally. This bit is useful in 2-wire configurations where it is necessary to measure the spectrum and transmit level of a transmitter. Setting the TXSQ bit turns off the transmitter so that only one of the two carriers is present. After TXSQ is reset, a retrain should be sent to reestablish the data transfer.

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
TXV	11:4	0	**Transmit Voice.** When control bit TXV is set and DCDEN bit is reset, transmit voice pass-through mode is selected which allows the host to directly access to the D/A converter. The host may convey 16-bit voice samples to VBUFTM and VBUFTL at the selected sample rate (7200 Hz default). The modem is ready for a new voice sample when bit TDBE is set. When control bit TXV is set and DCDEN bit is set, the ADPCM decoder is enabled instead of transmit voice pass-through mode. Sixteen data bits can be sent to VBUFTM and VBUFTL at the selected sample rate (7200 Hz default) and at the transmit bits per sample (see DECBITS and DCDEN). The modem is ready for a new voice sample when bit TDBE is set. Transmit voice pass-through mode or ADPCM transmit mode is available in tone modes only. (CONF = 80h, 81h, 83h, or 86h) **Note:** Writing to VBUFTM clears TDBE, therefore, VBUFTL (if used) must be written to before VBUFTM.
U1DET	0D:3	–	**Unscrambled 1s Detector.** When set, status bit U1DET indicates that V.22 bis unscrambled 1s sequence has been detected. This bit is reset by the modem at the end of the unscrambled 1s sequence. U1DET is not active when DATA is reset. (V.22 bis)
V21S	08:5	0	**V21 Synchronous.** When configuration bit V21S is set and the configuration (CONF) is set for V.21, the V.21 synchronous mode is selected. In V.21 synchronous mode, a synchronous transmit clock is provided on the TDCLK pin and a synchronous receive clock is provided on the RDCLK pin. During transmit, synchronous data may be applied in either serial or parallel form depending on the TPDM bit. During receive, synchronous data is output in both serial or parallel form. When V21S is reset and CONF is set for V.21, the V.21 asynchronous mode is selected.
V23HDX	11:2	0	**V.23 Half Duplex.** When control bit V23HDX is set, the modem operates in V.23 /1200 half duplex. The transmitter and receiver must be set to the same V.23 configuration, 1200 bps (CONF = A4h). Carrier is under RTS control and DTR must be on. The RTS-CTS delay is adjustable in RAM.
V32BDT	0E:4	–	**V.32 bis Rate Sequence Detected.** Status bit V32BDT is set when a V.32 bis rate sequence is detected. If V32BDT remains reset at the end of training, the V.32 bis rate sequence was not detected (i.e., the V.32 standard rate sequence was present). If V32BDT is set, rate changes may be accomplished by use of RREN or RTRN. If V32BDT is reset, rate changes can occur only by use of RTRN. (V.32 bis, V.32)
V32BS	04:5	1	**V.32 bis Select.** When a V.32 or V.32 bis configuration is selected (in CONF) and control bit V32BS is set, the modem operates in accordance with V.32 bis. Control bit V32BS selects the operating mode (1 = V.32 bis; 0 = V.32). If the modem is configured for 14400 bps, V32BS must be set. After setting or resetting V32BS, set NEWC to initiate the mode change. The use of the EARC bit is pertinent only when V32BS is reset. (V.32 bis)
V32DIS	0B:1	–	**V.32 Disconnect Detect.** When set, status bit V32DIS indicates that a line disconnection has occurred in V.32 bis/V.32 and the modem has synchronized on to it's own transmit signal (i.e., EQM acceptable and RLSD still on). The host may then issue a retrain to confirm the disconnection and subsequently drop the line if a response is not detected. (NOTE: If RLSD turns off or EQM increases to an unacceptable value due to a disconnection, bit V32DIS will not turn on.) Bit V32DIS will remain set until reset by the host. (V.32 bis, V.32)
V54A	08:3	0	**V.54 Acknowledgment Signaling.** When control bit V54A is set, and provided that CTS is ON, the transmitter will send a pattern of 1948 bits produced by scrambling a binary 1 with the polynomial $1+x^{-4}+x^{-7}$ in accordance with CCITT Recommendation V.54. The transmission will be at the modem data signaling rate. When transmission of the signaling pattern is complete, V54A is automatically reset by the modem. V.54 signaling pattern detection is available in both synchronous and asynchronous modes. (Not valid in FSK modes.)

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
V54AE	02:1	0	**V.54 Acknowledgment Phase Detector Enable.** When control bit V54AE is set, the V.54 acknowledgment phase detector is enabled in the receiver. V.54 signaling pattern detection is available in both synchronous and asynchronous modes. (See V54DT). (Not valid in FSK modes.)
V54DT	0F:0	0	**V.54 Pattern Detected.** When set, status bit V54DT indicates that one of the three V.54 patterns is being detected. Only one of the three detector enabling bits (V54PE, V54AE or V54TE) must be set by the host at any given time. V54DT should be reset by the host after detection. V.54 signaling pattern detection is available in both synchronous and asynchronous modes. (Not valid in FSK modes.)
V54P	08:2	0	**V.54 Preparatory Signaling.** When control bit V54P is set, and provided that CTS is ON, the transmitter will send a pattern of 2048 bits produced by scrambling a binary 0 with the polynomial $1+x^{-4}+x^{-7}$ in accordance with CCITT Recommendation V.54. The transmission will be at the modem data signaling rate. When the transmission of the signaling pattern is complete, V54P is automatically reset by the modem. V.54 signaling pattern detection is available in both synchronous and asynchronous modes. (Not valid in FSK modes.)
V54PE	02:0	**0**	**V.54 Preparatory Phase Detector Enable.** When control bit V54PE is set, the V.54 preparatory phase detector is enabled in the receiver. V.54 signaling pattern detection is available in both synchronous and asynchronous modes. (See V54DT). (Not valid in FSK modes.)
V54T	08:4	0	**V.54 Termination Signaling.** When control bit V54T is set, and provided that CTS is ON, the transmitter will send a pattern of 8192 bits produced by scrambling a binary 1 with the polynomial $1+x^{-4}+x^{-7}$ followed by 64 binary 1s in accordance with CCITT Recommendation V.54. The transmission will be at the modem signaling rate. When transmission of the signaling pattern is complete, V54T is automatically reset by the DSP. V.54 signaling pattern detection is available in both synchronous and asynchronous modes. (Not valid in FSK modes.)
V54TE	02:2	0	**V.54 Termination Phase Detector Enable.** When control bit V54TE is set, the V.54 termination phase detector is enabled in the receiver. V.54 signaling pattern detection is available in both synchronous and asynchronous modes. (See V54DT). (Not valid in FSK modes.)
VBUFTL	17:0-7	–	**Voice Buffer Transmit Least Significant Byte (LSB).** The host sends the least significant byte of the transmit voice sample to the modem transmitter by writing a byte to VBUFTL. (See TXV.) (ADPCM only.)
VBUFTM	10:0-7	–	**Voice Buffer Transmit Most Significant Byte (MSB).** The host sends the most significant byte of the transmit voice sample to the modem transmitter by writing a byte to VBUFTM. By setting TDBIE, the host can enable the assertion of IRQ upon the setting of TDBIA when VBUFTM is written. (See TXV.) (ADPCM only.)
VBUFRL	16:0-7	–	**Voice Buffer Receive Least Significant Byte (LSB).** The host obtains the least significant byte of the receive voice sample from the modem receiver by reading a byte from VBUFRL. (See RXV) (ADPCM only.)
VBUFRM	00:0-7	–	**Voice Buffer Receive Most Significant Byte (MSB).** The host obtains the most significant byte of the receive voice sample from the modem receiver by reading a byte from VBUFRM. By setting RDBIE, the host can enable the assertion of IRQ upon the setting of RDBIA when VBUFRM is read. (See RXV) (ADPCM only.)
VOLUME	01:6,7	0	**Volume Control.** The encoded VOLUME control bits select speaker off or one of three volume attentuation levels (at RIN) as follows: **7 6 Description** 0 0 Speaker off 1 0 Speaker attentuation = 0 dB (high volume) 0 1 Speaker attentuation = 6 dB (medium volume) 1 1 Speaker attentuation = 12 dB (low volume)

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
VPAUSE	01:5	0	**Voice Pause.** Control bit VPAUSE enables (1) or disables (0) the voice "pause." When VPAUSE is enabled, voice data is not output to the host.
VSYNC	0A:2	–	**Voice Sync.** VSYNC and RDBF are used to indicate when valid received voice samples are available in VBUFRM and VBUFRL. When RDBF is set the first time after status bit VSYNC is set, the contents of VBUFRM and VBUFRL must be read and discarded. When RDBF is set the second time after status bit VSYNC is set, the **first** valid received ADPCM voice sample is available in VBUFRM and VBUFRL. **This first valid received ADPCM voice sample (both bytes) must be read and saved for proper operation of the ADPCM decoder during subsequent playback.** Subsequent received ADPCM voice samples are available in VBUFRM and VBUFRL when RDBF is set regardless of the state of VSYNC. The VSYNC bit will remain set until being reset by the host. (ADPCM only.)
WDSZ	06:0,1	0	**Data Word Size.** The WDSZ field sets the number of data bits per character in asynchronous mode as follows (V.32 bis, V.32, V.22 bis, V.22, Bell 212A): **Data Bits/Character** — **WDSZ (Hex)** 5 — 0 6 — 1 7 — 2 8 — 3 This bit must be configured appropriately before the ASYN bit changes from a 0 to a 1 for asynchronous mode.

3.2 SOFTWARE INTERFACE CONSIDERATIONS

3.2.1 Interrupt Request Handling

DSP interface memory registers 00, 10, 1E, and 1F have unique hardware connections to the interrupt logic. Register 00 is the Receive Buffer (RBUFFER) and register 10 is the Transmit Buffer (TBUFFER). Registers 1E and 1F hold interrupt flag, interrupt enable, and interrupt active bits. When a condition occurs that satisfies an interrupt criteria, the corresponding interrupt flag bit is set. This interrupt flag can be reported to the host either by the host polling the interrupt flag bits (i.e., not using IRQ) or by being interrupted by IRQ. When an interrupt enable bit is a 1, IRQ is asserted and the appropriate interrupt active bit set to a 1 when the corresponding interrupt condition occurs.

The basic sources for IRQ generation are status change detected (status bits in registers 0A through 0F, maskable in DSP RAM), configuration change implemented, receive buffer full and transmit buffer empty. Each source is individually maskable. Table 3-2 identifies the interrupt sources and describes the interrupt clearing procedures.

3.2.2 Auto Dial Procedure

The host auto dial procedure is the same as outputting data to be transmitted using TBUFFER (Figure 3-2). The modem timing accounts for the DTMF tone duration and amplitude, and inter-digit delay. These dialing parameters are host programmable in DSP RAM.

Calling tone on/off times are also programmable in DSP RAM. Calling tone levels are controlled by the Transmit Level bits (TLVL).

The levels of the high band and low band DTMF tones may be modified by the host in DSP RAM. The level of the high band DTMF tone should be 2 dB greater than the level of the low band DTMF tone. Transmit Level bits (TLVL) do not affect DTMF levels.

The auto dialer default parameters are given in Table 3-3.

3.2.3 Auto Mode Selection

Figures 3-3 and 3-4 show the flowcharts corresponding to the DSP algorithm used in supporting originating and answering automode (AUTO 15:3), respectively.

Table 3-3. Auto Dialer Default Values

Parameter	*Default Value*
DTMF Tone Duration	92 ms
DTMF Interdigit Delay	72 ms
DTMF Total Output Power Level	0 dBm
DTMF Low Band Power Level	–4 dBm
DTMF High Band Power Level	–2 dBm
Pulse Relay Make Time	36 ms
Pulse Relay Break Time	64 ms
Pulse Interdigit Delay	750 ms
Calling Tone On Time	500 ms
Calling Tone Off Time	2 s

Table 3-2. Interrupt Request Bits

Interrupt Active Bit	Interrupt Enable Bit	Interrupt Flag Bit	Interrupt Condition Description	Interrupt Clear Procedure
NSIA	NSIE	NEWS	New status detected (NEWS transitioned from a 0 to 1) a. RAM read or RAM write occurred b. Status bit changed in register 0A through 0F	Host writes a 0 into NEWS (Clears NSIA to a 0)
NCIA	NCIE	NEWC	New configuration implemented by DSP (NEWC transitioned from a 1 to a 0)	Host writes a 0 into NCIE (Clears NCIA to a 0)
TDBIA	TDBIE	TDBE	TBUFFER is empty and can be written (TDBE transitioned from a 0 to a 1)	Host writes toTBUFFER (register 10:0-7) (Clears TDBE and TDBIA to 0)
RDBIA	RDBIE	RDBF	RBUFFER is full and can be read (RDBF transitioned from a 0 to a 1)	Host reads RBUFFER (register 00:0-7) (Clears RDBF and RDBIA to 0)

Dial Digits/Tone Pairs

Hex	Dial Digit	Tone Pairs	
		Tone 1	Tone 2
00	0	941	1336
01	1	697	1209
02	2	697	1336
03	3	697	1477
04	4	770	1209
05	5	770	1336
06	6	770	1477
07	7	852	1209
08	8	852	1336
09	9	852	1477
0A	*	941	1209
0B	#	941	1477
0C	A	697	1633
0D	B	770	1633
0E	C	852	1633
0F	D	941	1633
10	1300 Hz Calling Tone		
11	1100 Hz Calling Tone		

NOTE: Calling tone is continuously transmitted with the appropriate on-off time until NEWC is set or FFh is written into TBUFFER.

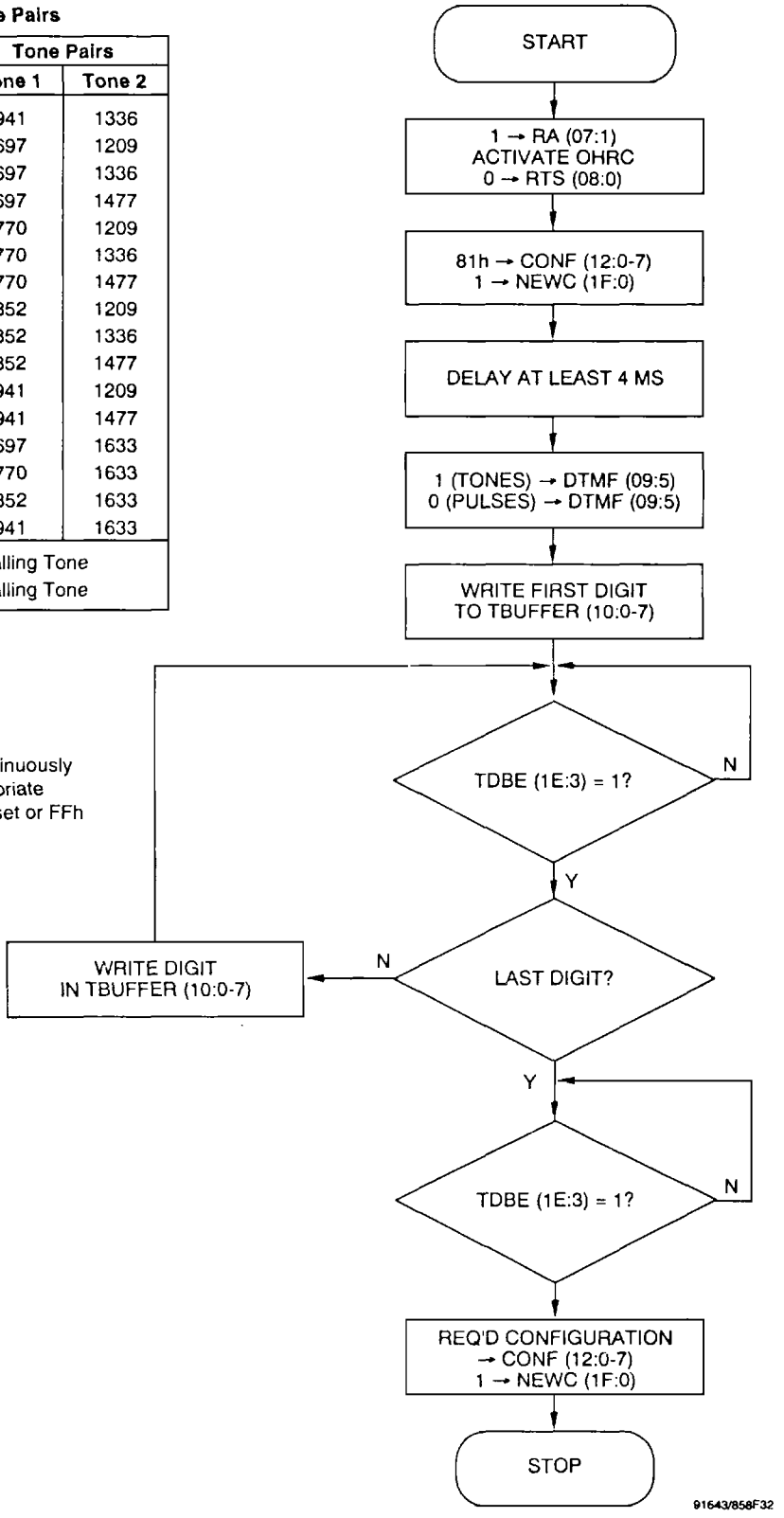


Figure 3-2. Auto Dial Sequence and Dial Digits

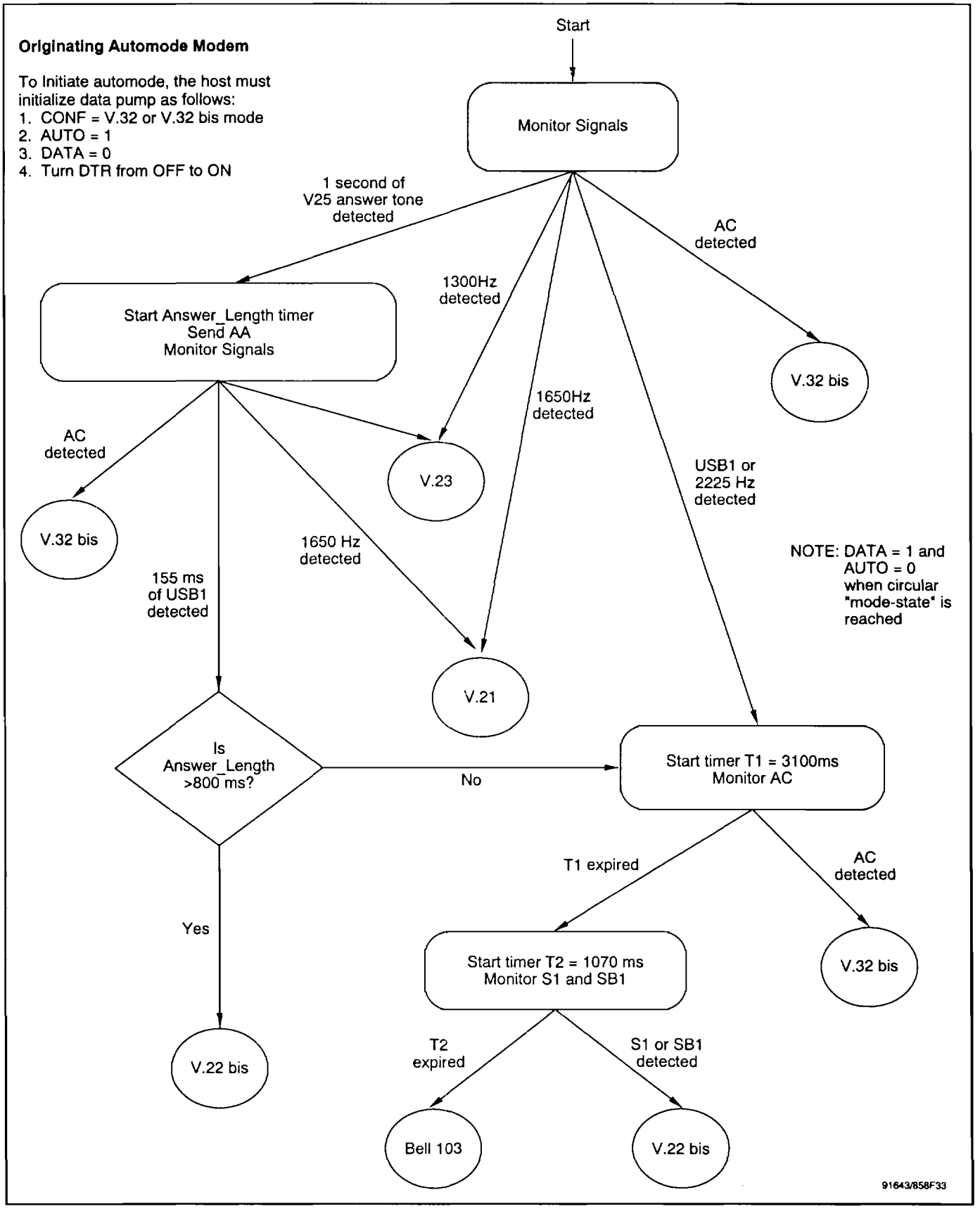


Figure 3-3. Host Flowchart - Originating Automode

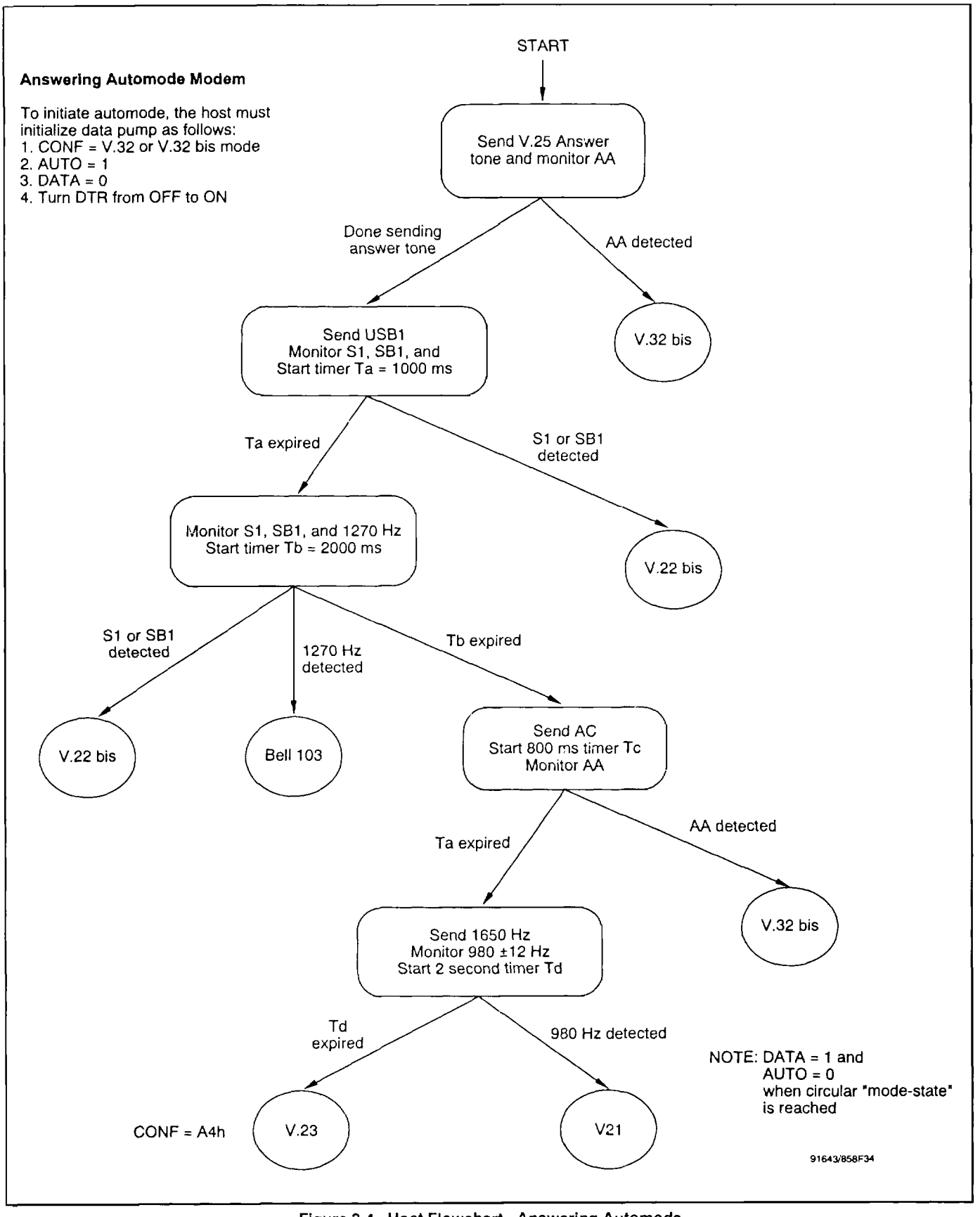


Figure 3-4. Host Flowchart - Answering Automode

4 DSP RAM ACCESS

The DSP contains a 16-bit wide random access memory (RAM). The host processor can access (read or write) the RAM through a 12-bit memory address in registers 1D and 1C.

4.1 INTERFACE MEMORY ACCESS TO DSP RAM

The interface memory acts as an intermediary during host to DSP RAM or DSP RAM to host data exchanges. The address stored in interface memory RAM address registers MEADDH and MEADDL by the host is the DSP RAM address for data access. The data is transferred through data registers MEDAM and MEDAL.

One or two bytes (1 byte = 8 bits) are transferred between DSP RAM and DSP interface memory once each device cycle. The DSP operates at a 7200 Hz sample rate.

The RAM access bit (MEACC) in the interface memory instructs the DSP to access the RAM. The transfer is initiated by the host setting the MEACC bit. The DSP tests this bit each sample period.

RAM can be accessed using one of four methods:

1. 8-bit read - 8-bit write.
2. 16-bit read - 8-bit write.
3. 16-bit read - 16-bit write.
4. 16-bit read only (modem diagnostics).

Parameters transferred under the first method have only 8 bits of significance. The data is written to and read from MEDAL. Data in MEDAM is ignored.

Parameters transferred using the second method have 16 bits of significance but can be written only 8 bits at a time. These parameters have two access codes associated with them, one for the least significant 8-bits and one for the most significant 8 bits. The host need read only the low address to obtain both the most significant and the least significant bytes of the data if the two access codes are in consecutive order.

Parameters transferred using the third method involve 16-bit read or write operations using one access code.

Finally, all diagnostic read operations using the fourth method use only one access code. Data is read from MEDAM and MEDAL.

The parameters available in DSP RAM are listed in Table 4-1.

4.2 HOST DSP READ AND WRITE PROCEDURES

DSP RAM Write Procedure

1. Set MEMW to inform the DSP that a RAM write will occur when MEACC is set.
2. Load the RAM address into the MEADDH and MEADDL registers.
3. Write the desired data into the interface memory RAM data registers MEDAM and/or MEDAL.
4. Set MEACC to signal the DSP to perform the RAM write.
5. When the DSP has transferred the contents of the interface memory RAM data registers into RAM, the DSP resets the MEACC bit and sets the NEWS bit to indicate DSP RAM write completion. If the NSIE bit is a 1, IRQ is asserted and NSIA is set to inform the host that setting of the NEWS bit is the source of the interrupt request.
6. At the completion of IRQ servicing, write a 0 into the NEWS bit to clear the NSIA bit and to negate IRQ if no other interrupt requests are pending.

DSP RAM Read Procedure

1. Reset MEMW to inform the DSP that a RAM read will occur when MEACC is set.
2. Load the RAM address code into the MEADDH and MEADDL registers.
3. Set MEACC to signal the DSP to perform the RAM read.
4. When the DSP has transferred the contents of RAM into the interface memory RAM data registers MEDAM and/or MEDAL, the DSP resets the MEACC bit and sets the NEWS bit to indicate DSP RAM read completion. If the NSIE bit is a 1, IRQ is asserted and NSIA is set to inform the host that setting of the NEWS bit is the source of the interrupt request.
6. At the completion of IRQ servicing, write a 0 into the NEWS bit to clear the NSIA bit and to negate IRQ if no other interrupt requests are pending.

4.3 RAM READ AND WRITE EXAMPLES

Figure 4-1 shows a flowchart of a procedure to change the DTMF tone duration using method 1.

Figure 4-2 shows a flowchart of a procedure to change the RTS-CTS delay using method 2.

Figure 4-3 shows a flowchart of a procedure to change the THRESHU value for TONEA using method 3.

Figure 4-4 shows a flowchart of a procedure to read EQM using method 4.

Table 4-1. Interface Memory RAM Addresses

No.	Function	Method	Address (Hex)
1	Transmitter Compromise Equalizer		
	First Coefficient Tap	3	AE8
	Last Coefficient Tap	3	AD0
	Number of Taps	3	B47
2	Rate Sequence		
	Received R	4	208
	Received E	4	20A
	Transmitted R	2	204, 205 (see Note 1)
	Transmitted E	2	206, 207 (see Note 1)
	V.32/V.32 bis R1 Mask	2	2C0, 2C1 (see Note 1)
	V.32/V.32 bis R2 Mask	2	2C2, 2C3 (see Note 1)
	V.32 bis R4 Mask	2	2C4, 2C5 (see Note 1)
	V.32 bis R5 Mask	2	2C6, 2C7 (see Note 1)
	V.33 R33 Mask	2	2C8, 2C9 (see Note 1)
3	DTMF Tone Duration	2	218, 2DB (see Note 1)
4	DTMF Interdigit Delay	2	219, 2DC(see Note 1)
5	DTMF Low Band Power Level	2	29B, 29C (see Note 1)
6	DTMF High Band Power Level	2	29D, 29E (see Note 1)
7	Pulse Relay Make Time	1	22C
8	Pulse Relay Break Time	1	21C
9	Pulse Interdigit Delay	2	21A, 21B
10	Calling Tone On Time	2	290, 2D9 (see Note 1)
11	Calling Tone Off Time	2	291, 2DA (see Note 1)
12	Transmitter Output Level Gain (G) and Offset (O)		
	Transmitter Output Level Gain (G) for Non- FSK Modes	3	A48
	Transmitter Output Level Gain (G) for FSK Modes	3	B57
	Transmitter Output Level Offset (O)	1	2CD
13	Dual Tone 1 Frequency	2	280, 281 (see Note 1)
14	Dual Tone 2 Frequency	2	282, 283 (see Note 1)
15	Dual Tone 1 Power Level	2	284, 285 (see Note 1)
16	Dual Tone 2 Power Level	2	286, 287 (see Note 1)
17	New Status Bit (NEWS)		
	Masking Register for 01	1	247
	Masking Register for 0A and 0B	2	246, 245
	Masking Register for 0C and 0D	2	244, 243
	Masking Register for 0E and 0F	2	242, 241
	Masking Register for 1A and 1B	2	27D, 27C
18	Total Span of Echo Cancellor	Read only	236
19	Echo Canceller Dividing Point	Read only	235
20	Far End Echo Canceller Center Tap Position	Read only	233
21	Echo Canceller Error	4	84D
22	Far End Echo Frequency Offset	4	852
23	Far End Echo Level	4	B52
24	CTS OFF-to-ON Response Time (RTS–CTS Delay)	2	202, 203 (see Note 1)
25	Answer Tone Length	2	228, 229 (see Note 1)
26	Silence after Answer Tone	2	22A, 22B (see Note 1)

Table 4-1. Interface Memory RAM Addresses (Cont'd)

No.	Function	Method	Address (Hex)
27	Tone Detector A Bandpass Filter Coefficients	3	See Table 4-6
28	Tone Detector B Bandpass Filter Coefficients	3	See Table 4-6
29	Tone Detector C Bandpass Filter Coefficients	3	See Table 4-6
30	V.23 Receiver Compromise Equalizer		
	Coefficients Tap 1	3	BF7
	Coefficients Tap 40	3	BD0
31	RLSD Turn-Off Threshold	3	A04
	RLSD Drop Out Timer	2	270, 271
32	RLSD Turn-On Threshold	3	A05
	RTH Offset RTH0	2	2D0, 2D1 (see Note 1)
	RTH Offset RTH1	2	2D2, 2D3 (see Note 1)
	RTH Offset RTH2	2	2D4, 2D5 (see Note 1)
	RTH Offset RTH3	2	2D6, 2D7 (see Note 1)
33	Received Signal Samples	4	800
34	V32 PN Length	2	288, 289 (see Note 1)
35	Low Pass Filter Output (X,Y)	4	801, 901 (see Note 2)
36	AGC Gain Word	4	A00
37	Round Trip Far Echo Delay	4	239
38	Equalizer Input (T) (X,Y)	4	A28,B28 (see Note 2)
39	Equalizer Input (T/2) (X,Y)	4	A14,B14 (see Note 2)
40	Equalizer Tap Coefficients:		
	First Coefficient Tap (X,Y)	4	A8F, B8F (see Note 2)
	Last Coefficient Tap (X,Y)	4	A60, B60 (see Note 2)
41	Rotated Equalizer Output (Received Point) (X,Y)	4	A19, B19 (see Note 2)
42	Decision Point (Ideal Point) (X,Y)	4	80F, 90F (see Note 2)
43	Equalizer Error (X,Y)	4	A2A, B2A (see Note 2)
44	Equalizer Rotation Angle	4	812
45	Equalizer Frequency Correction	4	811
46	Eye Quality Monitor (EQM)	4	20C
47	Maximum Period of Valid Ring Signal	1	21F
48	Minimum Period of Valid Ring Signal	1	21E
49	Phase Jitter Frequency	4	80E
50	Phase Jitter Amplitude	4	80D
51	Guard Tone Level	3	B46
52	CCITT CRC 32 Select	1	0B3
53	Secondary Channel Speed Select		
	Transmitter	1	28E
	Receiver	1	28B
54	ADC Speech Sample Scaling Parameter, ADCS (ADPCM)	3	BD1
55	White Noise Output Scaling Parameter, RANOISE (ADPCM)	3	A35
56	Minimum Silence Magnitude Threshold, MTHRESH (ADPCM)	3	A36
57	Detecting Silence in Speech Parameter, SILSPE (ADPCM)	3	B37
58	Detecting Speech in Silence Parameter, SPESIL (ADPCM)	3	B38
59	Minimum Silence Magnitude Adaptation Parameter, MADAPT (ADPCM)	3	B39

Table 4-1. Interface Memory RAM Addresses (Cont'd)

No.	Function	Method	Address (Hex)
60	Minimum On Time (DTMF)	3	A78
61	Minimum Off Time (DTMF)	3	878
62	Minimum Cycle Time (DTMF)	3	978
63	Minimum Dropout Time (DTMF)	3	B78
64	Maximum Speech Energy (DTMF	3	A77
65	Frequency Deviation, Low Group (DTMF)	3	876
66	Frequency Deviation, High Group (DTMF)	3	A76
67	Negative Twist Control, TWIST4 (DTMF)	3	977
68	Positive Twist Control, TWIST8 (DTMF)	3	877
69	Maximum Energy Hit Time (DTMF)	3	A67

Notes:
1. High address = MSB of data; low address = LSB of data.
2. The host may access only the X or Y data on any given read cycle, i.e., X and Y data cannot be accessed simultaneously.

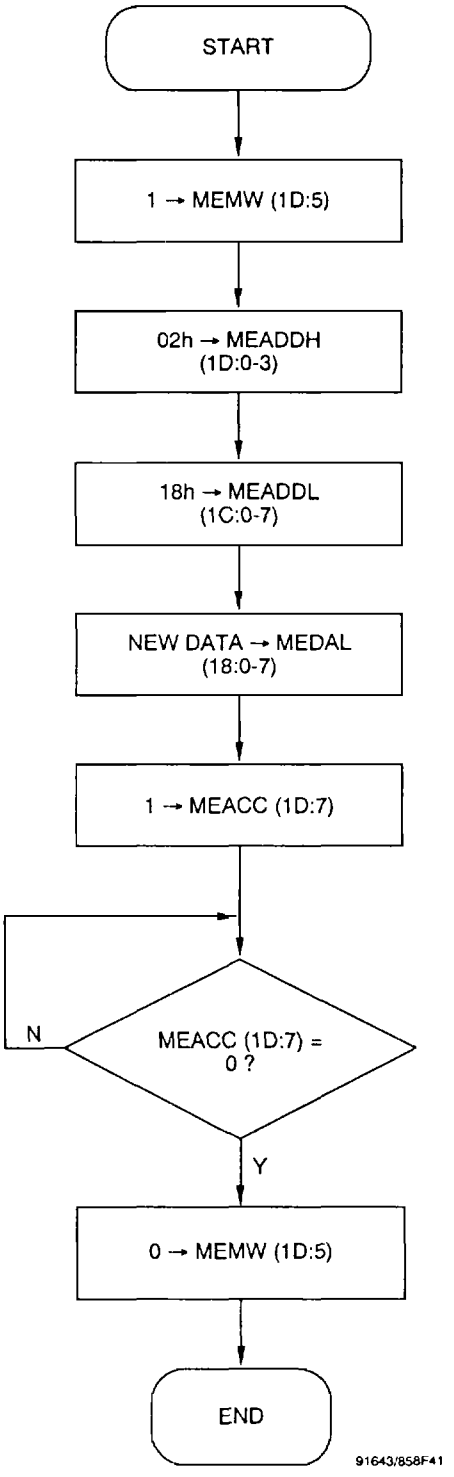


Figure 4-1. Method 1 Ex.-Changing DTMF Tone Duration (LSB)

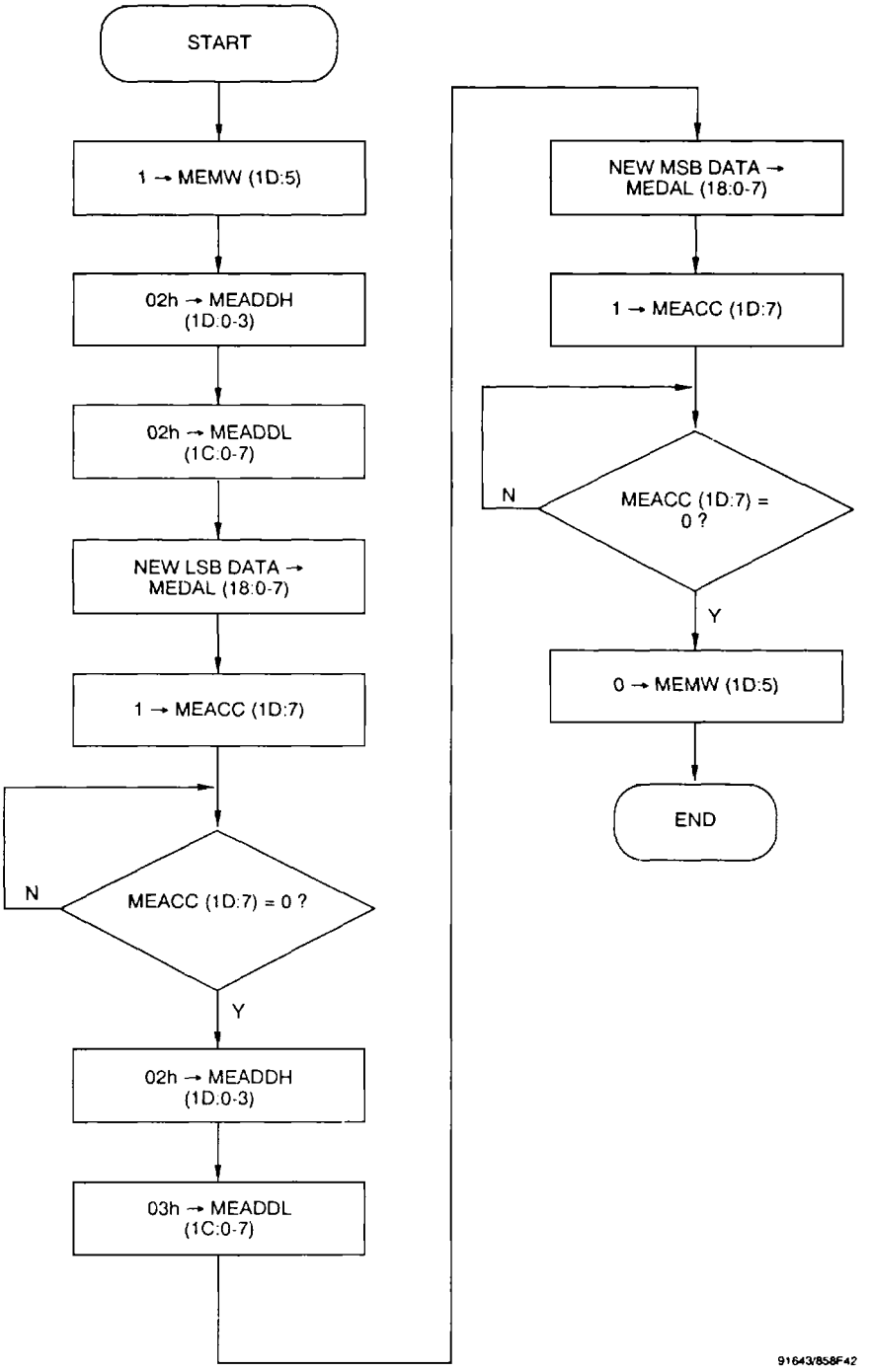


Figure 4-2. Method 2 Ex. - Changing RTS-CTS Delay

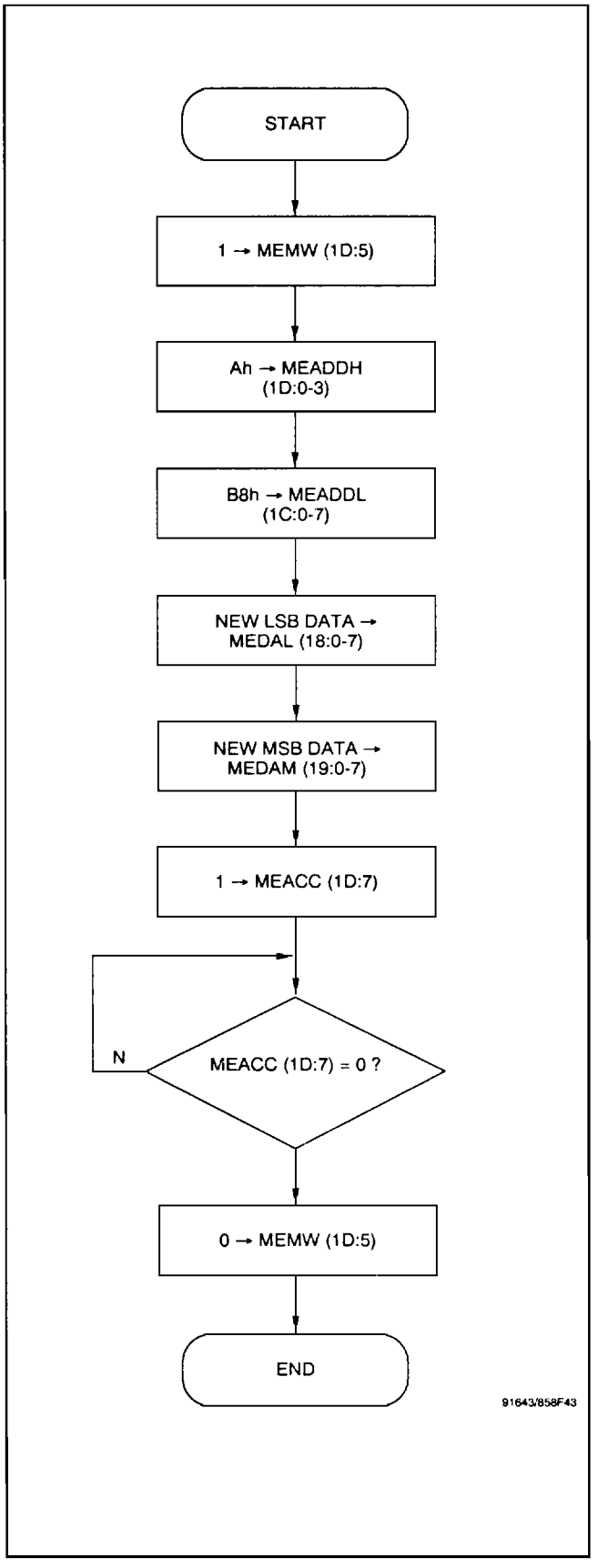


Figure 4-3. Method 3 Ex. - Changing TONEA THRHESHU

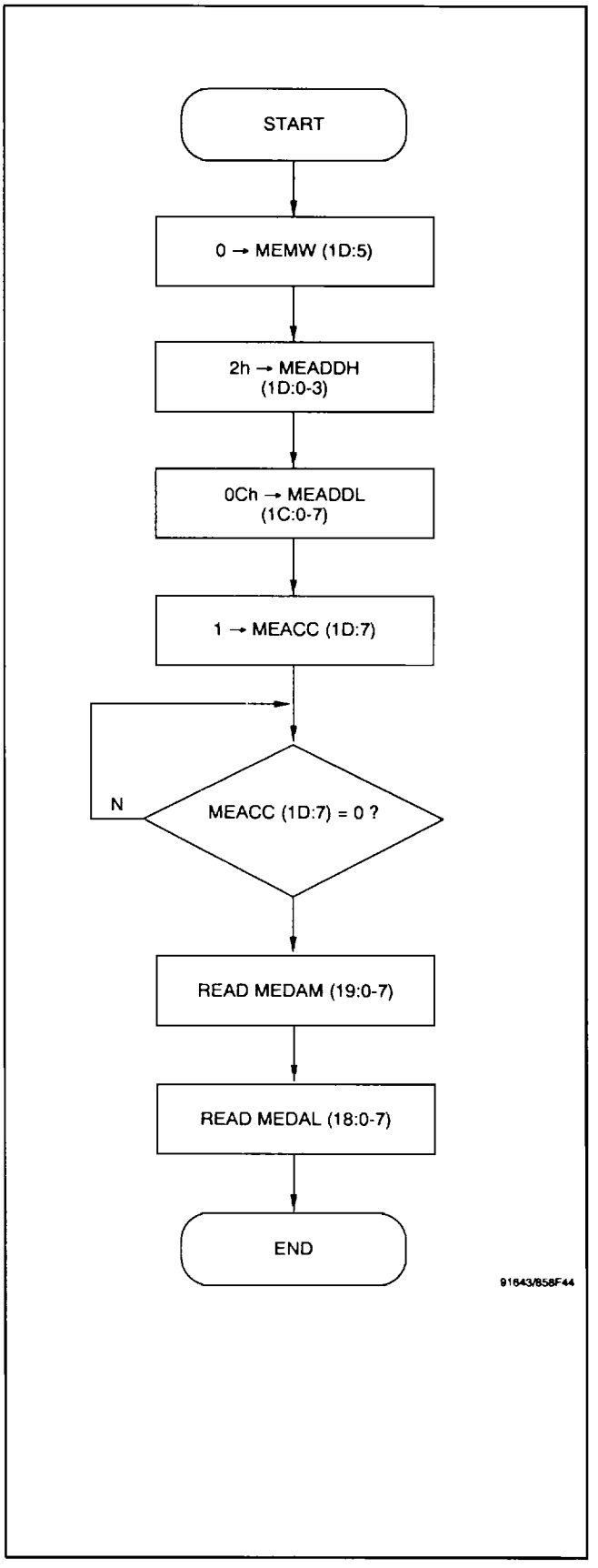


Figure 4-4. Method 4 Ex. - Reading EQM

4.4 DSP RAM DATA SCALING

Function 1: Transmitter Compromise Equalizer Coefficients

The transmitter compromise equalizer can be programmed by the user. The equalizer is a 25-tap finite impulse response (FIR) digital filter. The first tap is at address 5Bh (h denotes a hexadecimal number) and the last tap is at 34h. The sampling rate for the filter is 7200 Hz. New coefficients should be loaded while the modem is in idle mode before turning on DTR (2-wire full-duplex modes) or RTS (4-wire full-duplex modes). The coefficients have to be loaded only once. They are re-initialized to the default values only if a POR occurs. The user should ensure that the overall gain of any filter designed is 1. Set NEWC after new taps have been loaded.

Format: 16-bit, signed, 2s complement

Function 2: Rate Sequence

V.32 bis Rate Sequence Bits. CCITT defines the V.32 bis rate sequence bits as follows:

BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DATA	0	0	0	0	1	X	X	1	1	X	X	1	X	0	0	1

B0 = MSB; B15 = LSB

B0-B3, B7, B11, B15	for synchronizing on rate signal
B4	- 1 (Note 1)
B8	- 1 (Note 1)
B5	a 1 denotes the ability to receive at 4800 bps
B6	a 1 denotes the ability to receive at 9600 bps
B9	a 1 denotes the ability to receive at 7200 bps
B10	a 1 denotes the ability to receive at 12000 bps
B12	a 1 denotes the ability to receive at 14400 bps
B13, B14	- 0,0 (Note 2)

Note 1: When B4 or B8 is set to zero in a transmitted or received rate signal, then interworking can proceed only in accordance with Recommendation V.32.

Note 2: B13 and B14 shall be set to zero when transmitting and ignored during the reception of a rate signal; they are reserved for future definition by the CCITT and must not be used by the manufacturers.

Note 3: B4-B6, B9-B10, B12 set to zero calls for a GSTN clear down.

V.32 Rate Sequence Bits. CCITT defines the V.32 rate sequence bits as follows:

BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DATA	0	0	0	0	X	X	X	1	X	X	X	1	X	X	X	1

B0 = MSB; B15 = LSB

B0-B3, B7, B11, B15	for synchronizing on the rate sequence
B4	a 1 denotes the ability to receive at 2400 bps
B5	a 1 denotes the ability to receive at 4800 bps
B6	a 1 denotes the ability to receive at 9600 bps
B4-B6	0 0 0 calls for a GSTN clear down
B8	a 1 denotes the ability of trellis encoding and decoding at the highest data rate indicated in B3-B6.
B9-B14	0 0 1 0 0 0 denotes absence of special operational modes.

Note: When using the modem in a 7200 bps or 12000 bps proprietary configuration, B9 = 1 denotes the ability to receive at 7200 bps and B10 = 1 denotes the ability to receive at 12000 bps.

V.33 Rate Sequence Bits. CCITT defines the V.33 rate sequence bits as follows:

For B14 = 0:

BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DATA	0	0	0	0	X	X	X	1	X	X	X	1	X	X	0	1

B0 = MSB; B15 = LSB

B0-B3, B7, B11, B15	for synchronizing on the rate sequence
B4-B6, B10, B12, B13	not defined
B8	a 1 denotes the ability to receive at 12000 bps
B9	a 1 denotes the ability to receive at 14400 bps

For B14 = 1:

BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DATA	0	0	0	0	X	X	X	1	X	X	X	1	X	X	1	1

B0 = MSB; B15 = LSB

B0-B3, B7, B11, B15	for synchronizing on the rate sequence
B4, B5	a 00 denotes that B6, B10, B12, and B13 define multiplexer configuration selection
B8	a 1 denotes the ability to transmit and receive at 12000 bps
B9	a 1 denotes the ability to transmit and receive at 14400 bps
B6, B10, B12, B13	multiplexer configuration selection (see the V.33 specification for multiplexer configurations)

The V.32 and V.33 rate sequences contain undefined codes and/or bits. The user can use these bits to convey information to the remote modem during training (e.g., remote configuration, multiplexer configuration, test mode configuration, etc.).

The 16-bit rate sequence word in the modem's RAM corresponds exactly to the 16-bit rate sequences defined in V.32 and V.33. The MSB of the word in RAM is B0 of the rate sequence and the LSB is B15 of the rate sequence.

V.32/V.32 bis Rate Sequence

The V.32/V.32 bis rate sequence is available in RAM during the handshake when the RSEQ bit is a 1. The RSEQ bit will turn on when the E-sequence is available as well. The rate sequence(s) and E-sequence are read from two different RAM locations (see Table 4-1, Function 2). The RSEQ bit must be reset by the host after reading the rate sequence(s).

The host may modify the rate sequence in one of two ways.

Method 1 Description. The first and simplest method is to use the rate sequence mask (see Table 4-1, function 2). The rate sequence masks are available for R1, R2, R4, and R5. Rate sequences R1 and R2 are used during the initial handshake and retrains; R4 and R5 are used during rate renegotiations. The mask written to the appropriate RAM location will be logically ANDed to the out-going rate sequence. A power-on-reset will clear the masks to FFFFh.

Example of Method 1. To request or limit the modem speed to 9600 bps, the host would write 0B91h (see page 4-8 for rate sequence bit assignments) to address 2C1h and 2C0h if R1 is to be modified. The same value could be written to 2C5h and 2C4h if R4 is to be modified to limit the speed during a rate renegotiation. The available rates of the remote must be considered by the host before limiting speeds. If the modem determines no common rate is available between both modems during a rate change, the modem will send a clear down and turn off RLSD.

Method 2 Description. The second method for modifying the rate sequence is compatible with the RC144DP and is accomplished through addresses 205C and 204h. R1 and R3 are sent by the answering modem and R2 is sent by the originating modem.

To modify R1, the host must write a 0 at this address then wait for the value to equal non-zero. The host then has 1.5 seconds to change R1 (through RAM address 204 and 205) before it is sent.

To modify R2, the host must wait until the RSEQ bit is set to a 1 by the DSP. The host then has 1.5 seconds to modify R2 (through RAM address 204 and 205) .

To modify R3, the host must wait until the RSEQ bit is set to a 1 by the DSP, then change R3 (through RAM address 204 and 205).

In the case of rate renegotiations, R4 (sent by the requesting modem) is modified in the same manner as R3 after setting the RREN bit. R5 (sent by the responding modem) is also modified in the same manner after RREDT is set. The host has approximately 5 ms to modify R4 or R5 after the value in address 204h and 205h equals zero.

Typical rate sequences and E sequences shown in Table 4-2 and 4-3. The ARC bit is set on both modems. R1 and R3 are read on the originating modem, R2 is read on the answering modem. Refer to Section 5.3 of CCITT Recommendation V.32/V.32 bis for additional information on the V.32/V.32 bis rate sequence.

Table 4-2. R and E Sequences-V.32 to V.32 (V32BS=0)

Originate Set at	R1 (Hex)	R2 (Hex)	R3 (Hex)	E (Hex) (Ans and Org)	Answering Configuration	Resulting Configuration
V.32T/9600	0791	0791	0391	F391	V.32T/9600	V.32T/9600
	0711	0711	0311	F311	V.32/9600	V.32/9600
	0511	0511	0511	F511	V.32/4800	V.32/4800
V.32/9600	0791	0711	0311	F311	V.32T/9600	V.32/9600
	0711	0711	0311	F311	V.32/9600	V.32/9600
	0511	0511	0511	F511	V.32/4800	V.32/4800
V.32/4800	0791	0511	0511	F511	V.32T/9600	V.32/4800
	0711	0511	0511	F511	V.32/9600	V.32/4800
	0511	0511	0511	F511	V.32/4800	V.32/4800

Table 4-3. R and E Sequences-V.32bis to V.32bis (V32BS=1)

Originate Set at	R1 (Hex)	R2 (Hex)	R3 (Hex)	E (Hex) (Ans and Org)	Answering Configuration	Resulting Configuration
V.32T/14400	0FF9	0FF9	0999	F999	V.32T/14400	V.32T/14400
	0FF1	0FF1	09B1	F9B1	V.32T/12000	V.32T/12000
	0FD1	0FD1	0B91	FB91	V.32T/9600	V.32T/9600
	0DD1	0DD1	09D1	F9D1	V.32T/7200	V.32T/7200
	0D91	0D91	0D91	FD91	V.32/4800	V.32/4800
V.32T/12000	0FF9	0FF1	09B1	F9B1	V.32T/14400	V.32T/12000
	0FF1	0FF1	09B1	F9B1	V.32T/12000	V.32T/12000
	0FD1	0FD1	0B91	FB91	V.32T/9600	V.32T/9600
	0DD1	0DD1	09D1	F9D1	V.32T/7200	V.32T/7200
	0D91	0D91	0D91	FD91	V.32/4800	V.32/4800
V.32T/9600	0FF9	0FD1	0B91	FB91	V.32T/14400	V.32T/9600
	0FF1	0FD1	0B91	FB91	V.32T/12000	V.32T/9600
	0FD1	0FD1	0B91	FB91	V.32T/9600	V.32T/9600
	0DD1	0DD1	09D1	F9D1	V.32T/7200	V.32T/7200
	0D91	0D91	0D91	FD91	V.32/4800	V.32/4800
V.32T/7200	0FF9	0DD1	09D1	F9D1	V.32T/14400	V.32T/7200
	0FF1	0DD1	09D1	F9D1	V.32T/12000	V.32T/7200
	0FD1	0DD1	09D1	F9D1	V.32T/7200	V.32T/7200
	0DD1	0DD1	09D1	F9D1	V.32T/7200	V.32T/7200
	0D91	0D91	0D91	FD91	V.32/4800	V.32/4800
V.32/4800	0FF9	0D91	0D91	FD91	V.32T/14400	V.32T/4800
	0FF1	0D91	0D91	FD91	V.32T/12000	V.32T/4800
	0FD1	0D91	0D91	FD91	V.32T/9600	V.32T/4800
	0DD1	0D91	0D91	FD91	V.32T/7200	V.32T/4800
	0D91	0D91	0D91	FD91	V.32/4800	V.32/4800

Function 3-11: Dialing Parameters

The dialing parameters and their default values are listed in Table 4-4.

For Functions 3, 4, 7, 8, and 9, the time T (in ms) is calculated as follows:

Equation: $N = T \times 2.4$

Where: N is the decimal value of the hex number written to RAM (1-FFh).

A value of 0000 for the DTFM or calling tone on time will cause the modem to transmit the tone continuously until FFh is written into TBUFFER.

For functions 10 and 11, the time (in ms) is calculated as follows:

Equation: $N = T/10$

For Functions 5 and 6, the DTMF low or high band power level (P) in dBm is calculated as follows:

Equation: $N = \log^{-1}(P/20) \times 11264$

Where: N is the decimal value of the hex number written to RAM.

NOTE: The compromise equalizer is automatically disabled by the transmitter when sending DTMF tones, single tones, or dual tones. The DTMF levels are not affected by the transmit level bits (TLVL). The calling tones, however, are affected by the TLVL bits.

Table 4-4. Function 3-9 Dialing Parameters

Function	Parameter	Written Value (Hex)	Resultant Value (Dec)
3	DTMF Tone Duration	00DD	92 ms
4	DTMF Interdigit Delay	00AD	72 ms
5	DTMF Low Band Power Level	1DAA	– 4 dBm
6	DTMF High Band Power Level	2575	– 2 dBm
7	Pulse Relay Make Time	56	36 ms
8	Pulse Relay Break Time	99	64 ms
9	Pulse Interdigit Delay	0708	750 ms
10	Calling Tone On Time	0032	500 ms
11	Calling Tone Off Time	00C8	2 sec

DTMF Power Values

L (dBm)	N (Dec)	N (Hex)
+6	22475	57CB
+5	20031	4E3F
+4	17852	45BC
+3	15911	3E27
+2	14181	3765
+1	12638	315E
0	11264	2C00
–1	10039	2737
–2	8947	22F3
–3	7974	1F26
–4	7107	1BC3
–5	6334	18BE
–6	5645	1600

Function 12: Transmitter Output Level Gain

The transmitter output level gain constant (G) in dBm is calculated as follows:

Equation: $N = \log^{-1} [G/20] \times 16384$

Where: N is the decimal value of the hex number written to RAM.

Range: 0 - 7FFFh

Default: 4000h

The transmitter output level gain constant directly controls the output level of all configurations. It is used for fine tuning the output level which is controlled by the TLVL bits. Therefore,

Output Level = TLVL Setting + Transmitter Output Gain in dBm

Function 13-14 : Dual Tone 1 and 2 Frequency

G (dBm)	N (Dec)	N (Hex)
+0.5	17355	43CB
+0.4	17156	4304
+0.3	16956	423C
+0.2	16766	417E
+0.1	16574	40BE
0	16384	4000
–0.1	16196	3F44
–0.2	16011	3E8B
–0.3	15828	3DD4
–0.4	15647	3D1F
–0.5	15467	3C6B

Frequency F (in Hz) is calculated as follows:

Equation: $N = F/0.109863$

Where: N is the decimal value of the hex number written to RAM.

Default = 0

A single or dual tone is transmitted by writing 80h (single tone) or 83h (dual tone) to the CONF register, programming the tone transmit location in RAM, and then activating RTS. The tone will be transmitted as long as RTS is active.

Function 15-16 : Dual Tone 1 and 2 Power Level

F (Hz)	N (Dec)	N (Hex)
300	2731	0AAB
400	3641	0E39
445	4050	0FD2
600	5461	1555
1200	10923	2AAB
1800	16384	4000
2100	19115	4AAB
2250	20480	5000
2400	21845	5555
3000	27307	6AAB
3600	32768	8000

Power level in dBm (P_O) is calculated as follows:

Equation: $N = 19562 [10^{Po/20}]$ (Based on TLVL = 0 and 600 Ω termination.)

Where: N is the decimal value of the hex number written to RAM.

Range: 0 - 7FFFh

Default: 0 dBm (4C6Ah)

Notes:

1. The modem accepts change only when RTS is off.
2. The Transmit Level bits (TLVL) affect output level.
3. Power out = P_O + TLVL setting + transmitter output gain constant.

Function 17: NEWS Masking Register

Writing a 1 in the bit location corresponding to the desired bit will cause NEWS to go active when a status change occurs for the selected bit. All bits default to 0 at power-on-reset. Figure 4-5 shows the applicable masking register bits.

Modem Register	Bit								RAM Register (Hex)
	7	6	5	4	3	2	1	0	
1B	EDET	DTDET	OTS	DTMFD	DTMFW3	DTMFW2	DTMFW1	DTMFW0	27C
1A	—	—	—	—	—	SCOBF	SCIBE	—	27D
0F	RLSD	FED	CTS	DSR	RI	TM	RTSDT	V54DT	241
0E	RTDET	BRKD	RREDT	V32BDT	SPEED3	SPEED2	SPEED1	SPEED0	242
0D	P2DET	PNDET	S1DET	SCR1	U1DET	SADET	TXFNE	HKAB	243
0C	AADET	ACDET	CADET	CCDET	SDET	SNDET	RXFNE	RSEQ	244
0B	TONEA	TONEB	TONEC	ATV25	ATBEL	—	V32DIS	EQMAT	245
0A	PNSUC	—	PE	FE	OE	CRCS/SYNC	FLAGS	SYNCD	246
01	—	—	—	—	—	TXHF	RXFH	—	247

Figure 4-5. NEWS Masking Register

Function 18: Total Span of the Echo Canceller

Equation: N = Total Span of Echo Canceller x 2.4 ms

Where: N is the decimal value of the hex number read from RAM.

Function 19: Echo Canceller Dividing Point

Equation: N = Echo Canceller Dividing Point x 2.4 ms

Where: N is the decimal value of the hex number read from RAM.

Function 20: Far End Echo Canceller Center Tap Position

Equation: N = Center Tap Position x 2.4 ms

Where: N is the decimal value of the hex number read from RAM.

Function 21: Echo Canceller Error

Function 21 is the input to the receiver before the AGC in V.32 configurations. It is a 7200 Hz sampled signal. Note that it is sampled at the transmitter timing and not receiver timing. The parameter is a 16-bit 2s complement number.

Function 22: Far End Echo Frequency Offset

Function 22 provides the far-end echo frequency offset (FO), sometimes known as phase roll, in V.32 configurations.

Equation: FO = N/1749 Hz

Where: N is the decimal value of the hex number read from RAM.

Function 22 is a 16-bit 2s complement number. It is not valid until rate sequence R3 is detected in the originate modem, or rate sequence R2 is detected in the answer modem.

Function 23: Far End Echo Level

Function 23 provides the far-end echo power level at RXA in V.32 configurations. The following table lists average values read from RAM and the corresponding far end echo level in dBm:

Echo Level (dBm)	RAM Value (Hex)
-8	1200
-9	1000
-10	0E00
-11	0B00
-12	0A00
-13	0900
-15	0800
-20	0400
-25	0200
-30	0120
-35	0100
-40	0060
-45	0030

Note: Function 23 is not valid until RLSD is ON.

Function 24: CTS OFF-to-ON Response Time (RTS-CTS Delay)

Function 24 determines the CTS off-to-on response time in 2-wire full-duplex configurations. The response time equation depends on the selected configuration, i.e.:

Equation:

Configuration	Response Time Equation
V.32/V.32 bis	N = (Response time x 2.4 ms) –1
V.22 bis, V.22, Bell 212A	N = (Response time x 0.6 ms) –1
Bell 103, V.21	N = (Response time x 0.298 ms) –1
V.23/1200Tx	N = Response time x 1.2 ms
V.23/75Tx	N = Response time x 0.072 ms

Where: N is the decimal value of the hex number written to RAM.

Example: For an RTS-CTS delay of 20 ms in V.22 bis, N = [(20)(0.6)]-1 = 11 = 000Bh.

Default: Default values are listed in Table 4-5.

Note: Response time may vary by ± 2 baud times.

Table 4-5. RTS -CTS Delay Parameters

Function	Configuration	Default Value (Hex)	Default Value (Dec)	Units
24	V.32	0000	0.4	ms
	V.22 bis, V.22, Bell 212A	0000	1.6	ms
	Bell 103	003F	215	ms
	V.21	0098	500	ms
	V.23/1200Tx	00FC	210	ms
	V.23/75Tx	0010	235	ms

Functions 25 and 26: Answer Tone Length and Silence Period

The CCITT 2100 Hz answer tone length and silence after answer tone is calculated as follows:

Equation:

Configuration	Equation
V.32, V.21, Bell 103	N = T x 300 (V.32 silence: N = T x 2400)
V.22 bis, V.22, Bell 212	N = T x 600
V.23/75Tx,1200Rx	N = T x 75
V.23/1200Tx,75Rx	N = T x 1200

Where: N is the decimal equivalent of the hex number written to RAM and T is the time in seconds.

The DSP will rewrite the default values when DTR is turned off or the NEWC bit is set.

The end of answer tone transmission may be determined by monitoring the RAM location at address 151h. Bit 3 of the byte read from 151h will set to a 1 when the answer has finished and the silence period has commenced. Unless a power-on reset is performed, this bit must be reset by the host if it is to be monitored again on the following connection.

NOTE: Address 228h, 229h lengthens individual phase reversal times in V.32 bis/V.32. The V.32 bis/V.32 answer tone length may be adjusted by increasing or decreasing the number of phase reversals at address 04Bh. The default value at address 04Bh is 08h (8 phase reversals). This value may be changed only after DTR is set.

Function 27 through 29: Tone Detector Filter Tuning

A block diagram of the three tone detectors is shown in Figure 4-6. Tone detector C is preceded by a prefilter and a squarer. The purpose of the prefilter and squarer is to allow dual tones to be detected while rejecting the main channel energy. For example, TONEC can be programmed to detect a difference frequency generated by the squarer for detection of 350 Hz and 440 Hz. The prefilter would be designed to reject the energy in the 600 to 3000 Hz band. If the dual tone pair of 350 and 440 Hz appeared (or any other frequency pair in the range of 300 to 600 Hz with a difference of 90 Hz) TONEC would turn on.

The SQDIS bit (2:6) allows the squarer in front of tone detector C to be disabled. If the squarer is disabled then tone detector C will have four cascaded biquads (since there is a prefilter consisting of two biquads), forming an 8-order IIR filter with user programmable coefficients.

The implementation of the filters in the ultra high speed modems allows user definition of the characteristics of the prefilter and the three tone detectors. Table 4-6 provides the DSP RAM address codes for the filter coefficients. Table 4-7 shows the default values. Figure 4-6 shows that the prefilter and the main filter sections of the tone detectors are fourth order (two second-order biquads in cascade), thereby allowing a wide variety of filter characteristics to be synthesized. The only limitation on these user-definable shapes is that their gain should be around unity at the pass frequencies to avoid problems of saturation at one extreme (gain too high) and digital noise at the other (gain too low). Computation of the filter coefficients can be performed by any infinite impulse response (IIR) filter design program which outputs the coefficients in cascaded second-order sections.

The level detector in each of the tone detectors flags the detection of a tone if it is in the tone detector passband and if it is above an upper threshold defined by THRESHU. The tone detected flag will remain set until, or unless, the tone falls below a lower threshold defined by THRESHL.

The first-order low pass filter in each level detector, defined by the coefficients LPGAIN and LPFBK, controls the response time of each tone detector. Normally, these coefficients will not require alteration, but if, for example, a rapid cadence must be detected on a tone, then the 3 dB cutoff is approximately the reciprocal of the on-time or off-time of the tone, whichever is shorter. Decreasing LPFBK will speed up the response time. If LPFBK is decremented, then LPGAIN should be increase by the same amount. The gain of the filter should be set to unity (LPGAIN + LPFBK ~ 7FFFh). The default response time is in the order of 0.01 seconds.

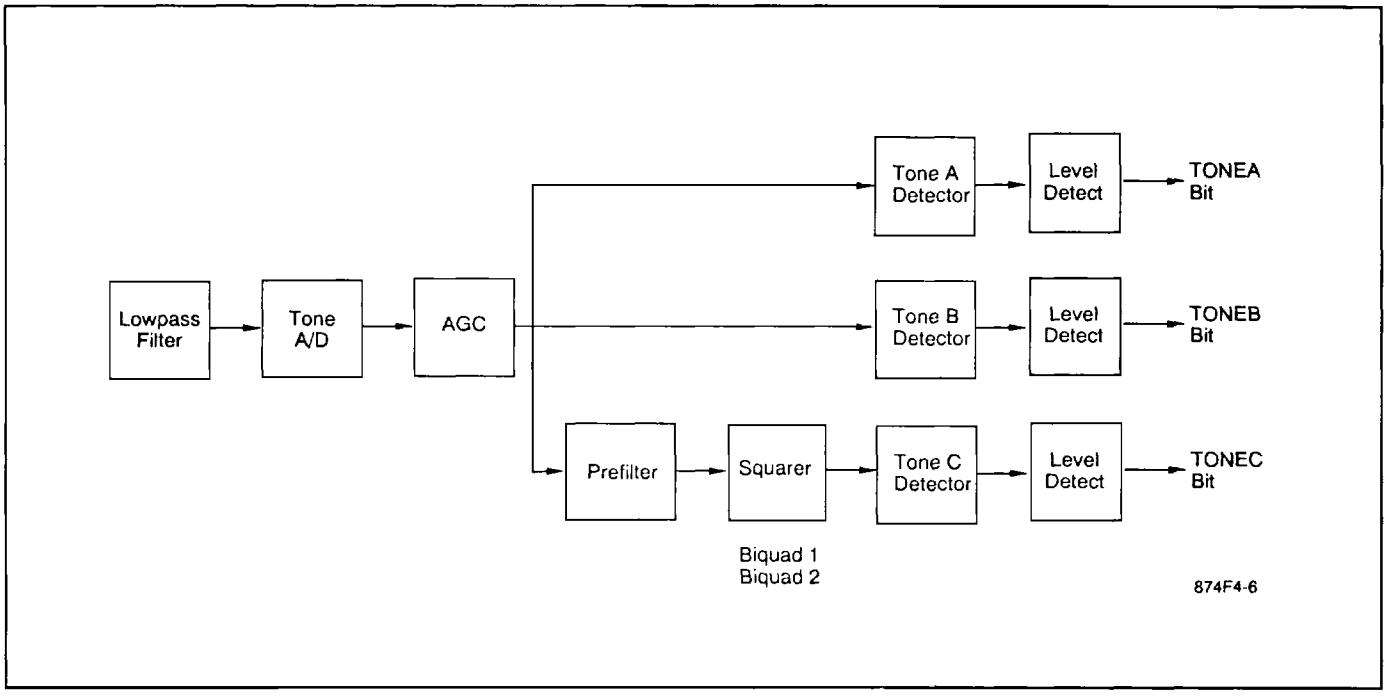


Figure 4-6. Tone Detectors

Table 4-6. TONEA, TONEB, and TONEC DSP RAM Addresses

Parameter	TONEA		TONEB		TONEC		Prefilter	
	Biquad1	Biquad2	Biquad1	Biquad2	Biquad1	Biquad2	Biquad1	Biquad2
A3	AA1	BA1	AA7	BA7	AAD	BAD	AB2	BB2
A2	AA2	BA2	AA8	BA8	AAE	BAE	AB3	BB3
A1	AA3	BA3	AA9	BA9	AAF	BAF	AB4	BB4
B2	AA4	BA4	AAA	BAA	AB0	BB0	AB5	BB5
B1	AA5	BA5	AAB	BAB	AB1	BB1	AB6	BB6

Table 4-7. TONEA, TONEB, and TONEC Default Values

Parameter	TONEA		TONEB		TONEC	
	Address	Value (Hex)	Address	Value (Hex)	Address	Value (Hex)
LPFBK	BA0	7F30	BA6	7E67	BAC	7F30
LPGAIN	AA0	00CF	AA6	02DF	AAC	00CF
THRESHU	AB8	0880	AB9	2A00	ABA	1600
THRESHL	BB8	0580	BB9	1C00	BBA	0A00

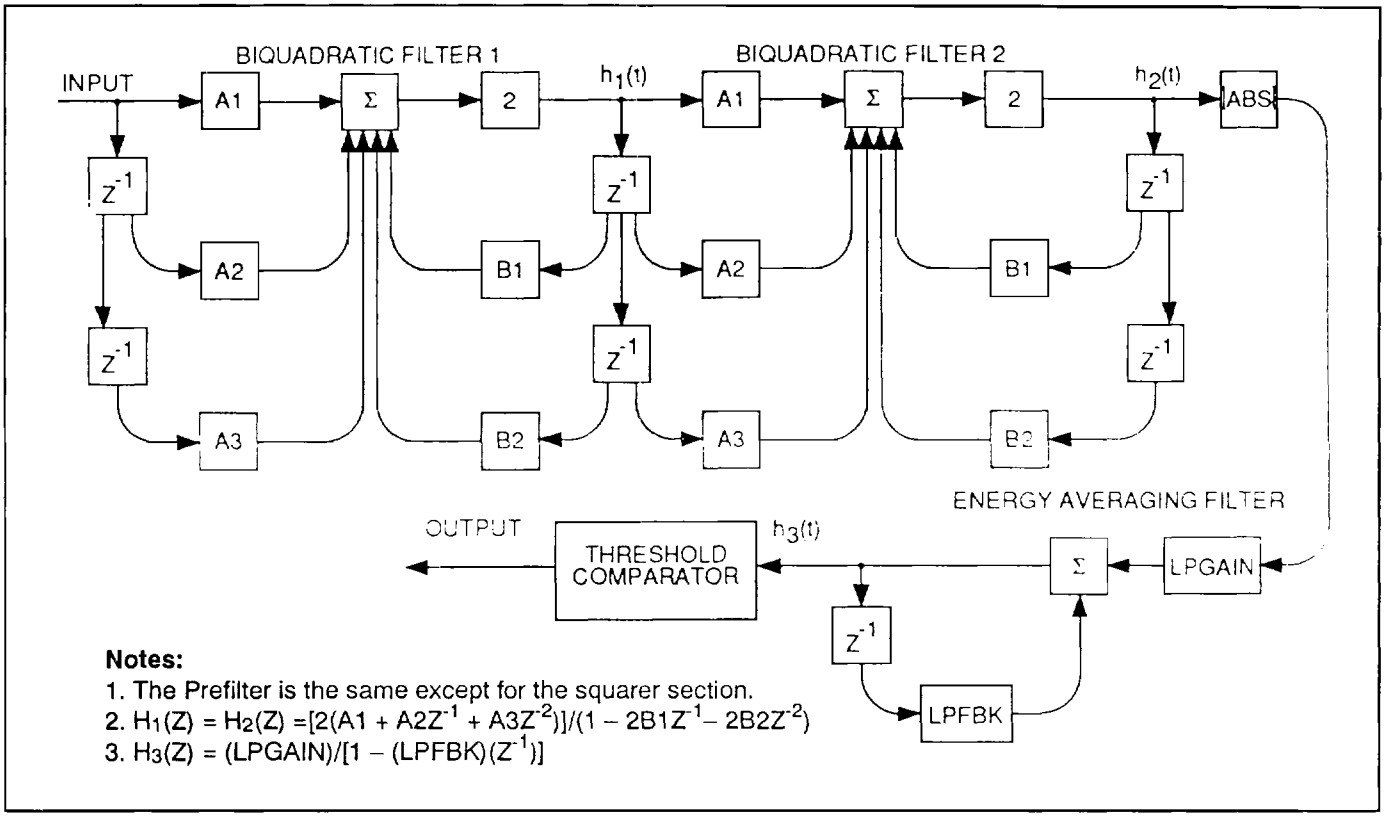


Figure 4-7. Biquad Filter and Level Detector

Example:

A call-progress tone detector is required for the US telephone network to detect appropriate tones that exceed –35 dBm.

Solution:

The requirement can be met by detecting tones in the 245 Hz-650 Hz range. A bandpass filter with a passband of 245Hz-650 Hz must be designed. Any filter up to fourth order can be implemented and, normally, it is best to choose the highest order available, especially for bandpass designs. A biquad filter design package could carry out this function by defining the passband frequencies, the filter order, the filter gain (chose unity), and the filter sampling rate (7200 Hz). An example of suitable coefficients is:

	A1	A2	A3	B1	B2
Biquad 1	0.1368	–0.2736	0.1368	1.8281	–0.8835
Biquad 2	0.1368	0.2736	0.1368	1.5716	–0.7920

These values should first be divided by two because coefficients greater than one are unrealized in the actual filter implementation. This division should be done even if none of the coefficients in the design are greater than one. This is because the biquad sections have been implemented as shown in Figure 4-7. The modified values are, therefore:

	A1'	A2'	A3'	B1'	B2'
Biquad 1	0.0684	–0.1368	0.0684	0.9140	–0.4418
Biquad 2	0.0684	0.1368	0.0684	0.7858	–0.3960

Next, convert the above numbers to fractional 2s complement numbers. In this case, the default coefficient values for TONEA:

	A1"	A2"	A3"	B1"	B2"
Biquad 1	08C2	EE7C	08C2	74FE	C774
Biquad 2	08C2	1184	08C2	6495	CD4F

The second part of the requirement is to detect tones that exceed –35 dBm. The approximate values of THRESHU and the corresponding tone level detected for TONEA at 500 Hz are:

THRESHU (Hex)	Tone Level Detected (dBm)
1100	–29
0C00	–32
0880	–35
0600	–38

THRESHU should be 0880h. If no hysteresis is required in the tone detector, then set THRESHL to 0880h (see Table 4-7). If hysteresis is required, then make THRESHL < THRESHU. Threshold levels stated in the data sheets are measured at the band edges. Other filter designs may require different values to those shown above. Note that changing threshold coefficients may change the bandwidth response of tone detectors.

Table 4-8 shows the filter coefficient values for specific filters. Adjust THRESHL and THRESHU as necessary (see Table 4-7).

Table 4-8. Example Tone Detect Filter Coefficients

	Biquad1 Coefficients (Hex)					Biquad2 Coefficients (Hex)				
Filter	**A3**	**A2**	**A1**	**B2**	**B1**	**A3**	**A2**	**A1**	**B2**	**B1**
1100 Hz	01B3	FC9C	01B4	C147	48C6	01B3	0097	01B4	C147	4897
1800 Hz	0184	FCFB	0185	C147	001C	0184	01BD	0185	C147	FFE4
2250 Hz	0205	FBF9	0206	C147	CF9C	0205	0380	0206	C147	CF68
2100 Hz	01E8	FC32	01E9	C147	DF4F	01E8	034E	01E9	C147	DF19
2225 Hz	0205	FBF9	0206	C147	D22D	0205	0380	0206	C147	D1F8
1270 Hz	02B2	FAA1	02B3	C147	38A4	02B2	00F0	02B3	C147	3871
1650 Hz	0306	F9F9	0307	C147	10A6	0306	010D	0307	C147	106E
980 Hz	0205	FBF9	0206	C147	5337	0205	00B4	0206	C147	530D
1300 Hz	0244	FB7B	0245	C147	35A7	0244	00CA	0245	C147	3574
245-650 Hz[1]	08C2	EE7C	08C2	C774	74FE	08C2	1184	08C2	CD4F	6495
360-440 Hz[2]	0000	FD36	02CA	C63E	7243	02CA	0593	02CA	C63E	7243

Notes: 1. TONEA default.
2. TONEB default.

Function 31 and 32: RLSD Thresholds

The receive RLSD thresholds may be modified using either of two different methods.

Method 1

The first and easiest method consists of altering the internal receiver gain (RAM address A03h) to shift the turn-on and or turn-off threshold up or down.

The RTH bit field selects a default threshold setting for the modem's receiver (see RTH bit description). The receiver gain is adjusted automatically for each of the four RTH values and switches between a turn-on and a turn-off value depending if the modem is in an idle mode (RLSD off) or connect mode (RLSD on). A threshold offset is associated with each RTH setting (see Function 32) which in turn offsets the receiver gain by a given amount. The higher the gain value, the higher the threshold. The following are the RTH offset RAM addresses and the corresponding default offset.

RTH	RAM Address	Default Offset
0	2D1,2D0	0000
1	2D3,2D2	1AC0
2	2D5,2D4	2CC0
3	2D7,2D6	4640

Note: A power-on-reset will return the offset values to their default states.

The following are the default idle receiver gain values for the corresponding modes and RTH value. The gain values are increased by the modem when in data mode.

	Idle Receiver Gain Value			
Mode	RTH = 0	RTH = 1	RTH = 2	RTH = 3
V.32bis/V.32	0900	23C0	35C0	4F40
V.22bis/V.22/Bell 212A	0100	1BC0	2DC0	4740
Bell 103	1A00	34C0	46C0	6040
V.33/V.17	0E4C	290C	3B0C	548C
V.29/9600/7200	0C80	2740	3940	52C0
V.29/4800	0D80	2840	3A40	53C0
V.27	0C00	26C0	38C0	5240
V.21	2000	3AC0	4CC0	6640
V.23/1200	1800	32C0	44C0	5E40
V.23/75/V.21CH2	1C00	36C0	48C0	6240

Example: To increase both the turn-on and turn-off thresholds by a few tenths of a dB using RTH=0, write a value of approximately 0100h in RAM address 2D1,2D0 while in idle mode and set NEWC. By setting NEWC, the offset is added to the receiver gain value. If setting NEWC is not desired, the offset loaded in RAM may be manually added to the gain value at RAM address A03.

Example: To decrease both the turn-on and turn-off thresholds by a few tenths of a dB using RTH=0, write a value of FF00h in RAM address 2D1,2D0 while in idle mode and set NEWC. This will subtract 0100h from the gain value.

In both examples, note that if RTH is set to a 1, the corresponding offset is 1AC0 and a value of 1BC0h should be written to RAM address 2D3,2D2 to increase the threshold or 19C0h to decrease the threshold. The offset is always relative to the RTH value used.

The offset may be changed when connected in data mode (RLSD on) if the default hysteresis is not satisfactory. For example, choose an offset value to obtain the desired turn-on threshold and set NEWC. When RLSD is on in data mode, change the offset value to increase or decrease the turn-off threshold in order to obtain a narrower or wider hysteresis. After writing the desired offset, add or subtract the change in offset to the current receiver gain value at RAM address A03. **Do not set NEWC.** Setting NEWC in data mode will either terminate or disrupt the connection. When RLSD turns off, repeat the process.

Selecting the appropriate offset is accomplished by empirical measurements. Note that the gain value for RTH=1 is equal to the default offset value plus the gain value for RTH=0, a total offset of 1AC0h. The difference in thresholds between RTH=0 and RTH=1 is 10 dB. From this, the user can extrapolate the approximate offset value needed for the desired threshold.

Method 2

The second method is a little more difficult and not as reliable as the first method but is compatible with the RC144DP modem. The RLSD thresholds may be modified as follows.

Method 2

The second method is a little more difficult and not as reliable as the first method but is compatible with the RC144DP modem. The RLSD thresholds may be modified as follows.

The host must monitor the RLSD bit and rewrite a RAM location to alter the RLSD turn-on and turn-off thresholds. The turn-off value may be written any time after RLSD has turned on but the turn-on value must be written after RLSD has turned off and after the modem has reinitialized the default value in RAM.

The higher the value, the higher the threshold level. Line hits or dropouts may cause the turn-off value to be reset by the DSP. The host should, therefore, periodically monitor the turn-off RAM location and rewrite the desired value if it has changed while RLSD is still on. A minimum hysteresis of 2 dB between the turn-on and turn-off thresholds should be maintained.

The default RLSD threshold values are as follows:

Configuration	RLSD Turn-on (Address A05h)		RLSD Turn-off (Address A04h)	
V.32 bis/V.32	581		135	
V.29, V.27, V.17, V.33, V.22 bis, V.22, Bell 212	6C8		17D	
V.21 Channel 2	1F2		18C	
	Ans.	**Org.**	**Ans.**	**Org.**
V.21	200	130	0E4	0C0
V.23 75Tx/1200Rx	2FB	3C9	156	21A
V.23 1200Tx/75Rx	3C9	2FB	21A	156
Bell 103	273	13D	189	0CB

Function 34: V.32 PN Length

The V.32/V.32 bis handshaking and retrain sequence may be shortened or lengthened to meet special applications by adjusting the length of the PN (TRN) sequence. The answering modem sends two TRN sequences during the handshake while the originating modem sends only one.

The TRN time T (in ms) is calculated as follows:

Equation: $N = (2.56 \times T) - 512$

Where: N is the decimal equivalent of the hex number written to RAM and T is the time in ms.

Note: Values of N should be kept within 400h to 1C00h. A power-on reset will clear this location.

Changing the TRN lengths should be reserved for special applications only and is not recommended. Short TRN sequences may jeopardize the success of the handshake or retrain. Consult the CCITT V.32/V.32 bis specifications for TRN length limitations.

Function 36: AGC Gain Word

Function 36 is useful for determining the receive level at the Receive Analog (RXA) input. The number in RAM is related to the receive level as follows:

Equation: Receive level = $1.5 \times Y - 50.5$ dBm

Where: $Y = \text{int}(N/1024)$

N is the decimal value of the hex number read from RAM.

This formula is only valid if the receive level is above the RLSD off-to-on threshold.

Function 37: Round Trip Far Echo Delay

Function 37 provides the value of the round trip delay measured during the V.32 handshake.

Equation: $RTD = (N/2.398) - 29$

Where: RTD = Round Trip Delay in ms

N = Decimal equivalent of value read from RAM

Function 46: Eye Quality Monitor

In V.32 4800 bps, V.29, V.27, V.22 bis, V.22 and Bell 212A modes, EQM is the filtered squared magnitude of the error vector. However, for all TCM modes (V.33 modes and V.32 12000, 9600, and 7200 bps modes), EQM is the filtered minimum trellis path length (or metric). This gives a better indication of signal quality for trellis modes.

The error vector formed by the decision logic can be used to indicate relative signal quality. As signal quality deteriorates, the average error vector increases in magnitude. By calculating the magnitude of the error vector and filter the results, a number inversely proportional to signal quality is derived. This number is called the eye quality monitor (EQM). Because of the filter time constant, EQM should be allowed to stabilize for approximately 700 baud times following RLSD going active.

The EQM value for the non-trellis configurations is the filtered squared magnitude of the error vector and represents the average signal power contained in the error component. The power is directly proportional to the probability of errors occurring in the received data and can be used to implement a discrete Data Signal Quality Detector circuit (circuit 110 of CCITT Recommendation V.24 or circuit CG of the RS-232-C standard) by comparing the EQM value against experimentally determined criteria (Bit Error Rate curves). Figure 4-6 illustrates the relationship of the EQM number to an eye pattern created by a 4-point signal structure (e.g., V.29/4800 bps) in the presence of high level white noise. The EQM value is proportional to the square of the radius of the disk around any ideal point. The radius increases when signal to noise ratio (SNR) decreases. As the radius approaches the ideal point's boundary values, the bit error rate (BER) increases. Curves of BER as a function of the SNR are used to establish a criteria for determining the acceptability of EQM values. Therefore, from an EQM value, the host processor can determine an approximate BER value. If the BER is found to be unacceptable, the host may cause the modem to fallback to a lower speed to improve BER.

It should be noted that the meaning of EQM varies with the type of line disturbance present on the line and with the various configurations. A given magnitude of EQM in V.29/9600 does not represent the same BER as in V.27/4800. The former configuration has 16 points that are more closely spaced than the four signal points in the latter, resulting in a greater probability of error for a given level of noise or jitter. Also, the type of line disturbance has a significant bearing on the EQM value. For example, white noise produces an evenly distributed smearing of the eye pattern with about equal magnitude and phase error while phase jitter produces phase error with little error in magnitude.

Since EQM is dependent upon the signal structure of the modulation being used and the type of line disturbance, EQM must therefore be determined empirically in each application.

A typical eye pattern generation circuit is shown in Figure 4-9.

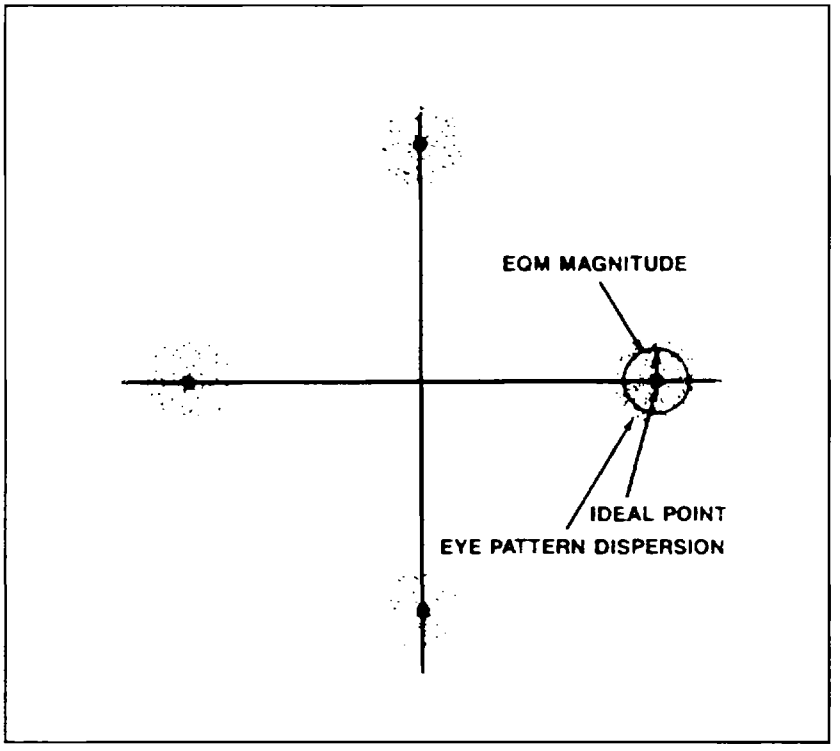


Figure 4-8. Relationship of EQM to Eye Pattern

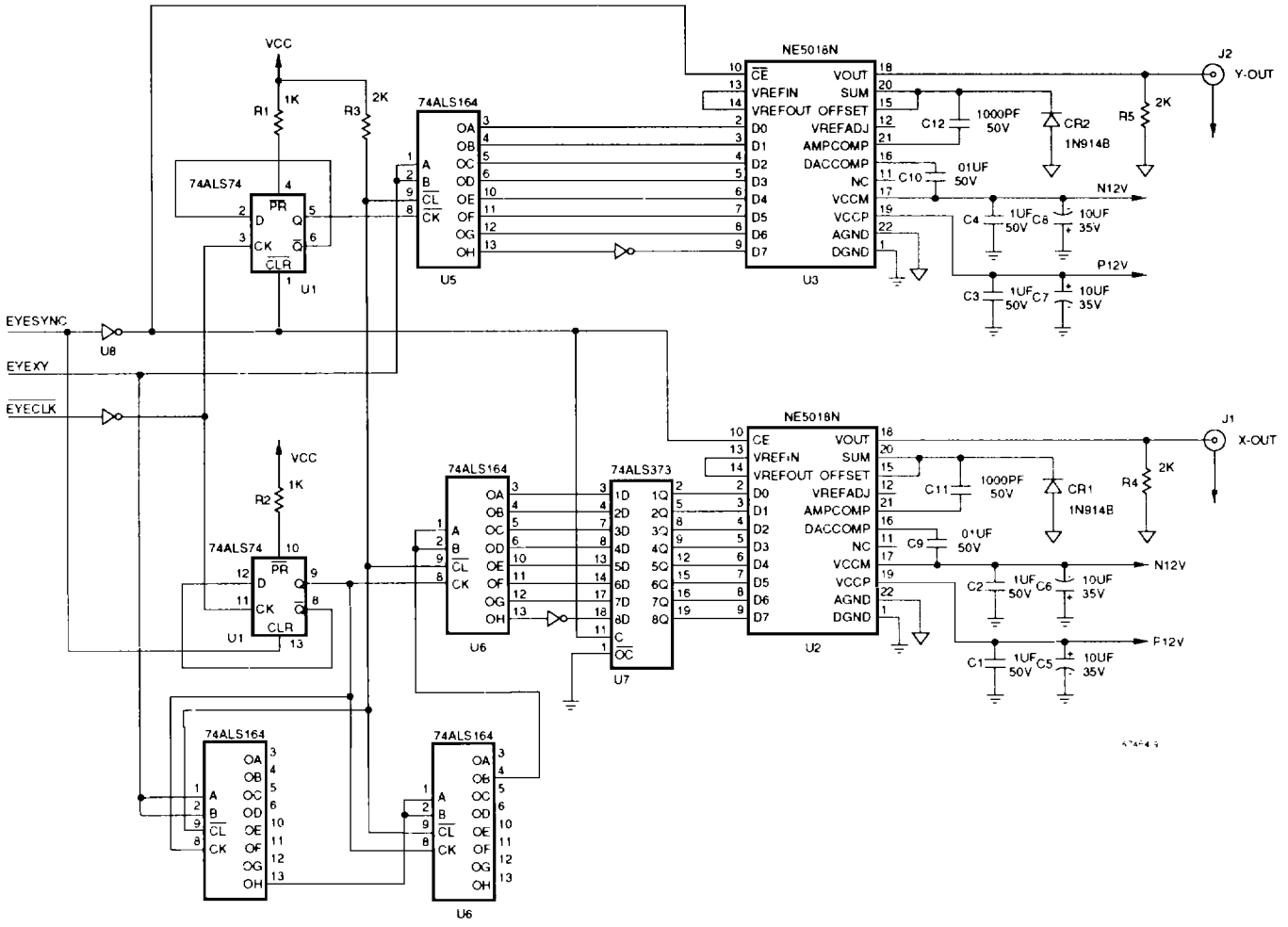


Figure 4-9. Eye Pattern Generator Circuit

Function 47 and 48: Ring Detection Parameters

The ring detector measures the period of pulses on the ring detect input and determines whether the pulses are within the frequency range specified by the Maximum Period of Valid Ring Signal and Minimum Period of Valid Ring Signal functions. Since maximum period corresponds to minimum frequency, the formula for calculating these functions is given in terms of frequency.

Frequency F (in Hz) is calculated as follows:

Equation: $N = 2400/F$

Where: N is the decimal value of the hex number written to RAM (05h-FFh).

Table 4-9 lists the Function 48 and 49 parameters.

Note: Writing 00 to Function 48 will cause the RI bit state and $\overline{RI}$ pin level to follow the $\overline{RD}$ pin level.

Table 4-9. Function 48 and 49 Parameters

Function	Parameter	Default Value		
		(Hex)	(Dec)	Units
47	Maximum Period of Valid Ring Signal	A0	15	Hz
48	Minimum Period of Valid Ring Signal	23	68	Hz

Functions 49 and 50: Phase Jitter Frequency and Amplitude Estimate

The phase jitter frequency and amplitude estimates are available in V.32/V.32 bis only. The phase jitter amplitude must be greater than approximately 6 degrees with a minimum frequency of 10 Hz in order for the modem to lock on and track the jitter.

The approximate phase jitter frequency and amplitude are calculated as follows:

Equation: $F = N/27.3$ (Function 49)

$AP = N/81$ (Function 50)

Where: N is the decimal equivalent of the hex number read from RAM
F is the frequency in Hz
AP is the amplitude in degrees.

Function 51: Guard Tone Level

Guard tone power in dBm (P_O) is calculated as follows (based on TLVL bits = 9 and 600 Ω termination):

Equation: $N = 5456\ [10^{Po/20}]$ (for 1800 Hz guard tone, GTS bit = 0; CEQ bit = 1)

$N = 5712\ [10^{Po/20}]$ (for 550 Hz guard tone, GTS bit = 1; CEQ bit = 1)

$N = 4650\ [10^{Po/20}]$ (for 550 Hz or 1800 Hz guard tone, GTS bit = 1; CEQ bit = 0)

Where: N is the decimal value of the hex number written to RAM.

Default: 0360h (for 1800 Hz guard tone, GTS bit = 0; CEQ bit = 1)

0476h (for 550 Hz guard tone, GTS bit = 1; CEQ bit = 1)

0322h (for 1800 Hz guard tone, GTS bit = 0; CEQ bit = 0)

03B4h (for 550 Hz guard tone, GTS bit = 1; CEQ bit = 0)

Notes:

1. Setting the NEWC bit will reset the power level to its default level.
2. The power level may be adjusted only after the GTE bit is set.
3. The transmit level bits (TLVL) affect the guard tone power output level.
4. Guard tone power is available in V.22 bis/2400 or V.22/1200 answer mode only.

Function 52: CCITT CRC32

When bit 0 (LSB) of address 0B3h is set, CCITT CRC 32 generation and detection is used in HDLC mode as opposed to the default CCITT CRC 16.

Function 53: Secondary Channel Speed

The default data rate for the secondary channel is 150 bps. The rate can be changed by modifying a divide factor in two RAM locations. The RAM locations are: 28Eh for the transmitter and 28Bh for the receiver. The following table lists the possible secondary channel speeds for the various main channel speeds and the corresponding RAM value. A power-on-reset will clear locations 28Eh and 28Bh.

Transmitter and Receiver RAM Divide Constant Values(hex)

	Secondary Channel Speed (bps)					
Main Channel Speed (bps)	75	150	300	600	1200	2400
14400	8	10				
12000	8	10				
9600 TCM	4	8	10			
9600 QAM	2	4	8	10		
7200	2	4	8	10		

Function 54: ADC Speech Sample Scaling Parameter, ADCS (ADPCM Rx-coding))

The received signal sample is scaled by parameter ADCS prior to ADPCM compression by the Rx-coder. Decreasing the value of this parameter attenuates the received speech samples.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Default: 7FF0h

Function 55: White Noise Output Scaling Parameter, RANOISE (ADPCM Tx-decoding and Silence Interpolation)

This parameter controls the output level of the white noise inserted during silence intervals when the decoder is enabled.

Format: 16 bit, twos complement, positive value

Range: 0000h to 7FFFh

Default: 0080h

Function 56: Minimum Silence Magnitude Threshold, MTHRESH (ADPCM Rx-coding and Silence Deletion)

If the background noise level is high, MTHRESH may be increased to allow more silence to be detected and deleted. Any signal with energy less than MTHRESH is detected as silence. However, a signal with energy greater than MTHRESH may or may not be detected as silence depending upon ADPCM algorithm processing.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Default: 0100h

Function 57: Detecting Silence in Speech Parameter, SILSPE (ADPCM Rx-coding and Silence Deletion)

SILSPE is used in determining when silence is detected during speech. To delay detection of speech-to-silence transition, increase SILSPE. A late transition will prevent the ends of spoken words from being deleted.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Default: 5555h

Function 58: Detecting Speech in Silence Parameter, SPESIL (ADPCM Rx-coding and Silence Deletion)

SPESIL is used in determining when speech is detected during silence. To advance detection of silence-to-speech transition, increase SPESIL. An early transition will prevent the beginning of spoken words from being deleted.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Default: 5000h

Function 59: Minimum Silence Magnitude Adaptation Parameter, MADAPT (ADPCM Rx-coding and Silence Deletion)

MADAPT controls the rate at which the silence-to-speech energy threshold adapts to the changing received signal energy. If MADAPT is too small, segments of a speech signal will be deleted resulting in unintelligible, choppy, speech.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Default: 5555h

Function 60 Minimum On Time (DTMF)

The on-time is defined as the minimum period of time of the DTMF signal beginning when the signal is detected and ending when the energy is below the turn-off threshold. The on-time parameter cannot be set below 20 ms (0000h). The default on-time parameter is set for 40.0 ± 1 ms. The on-time will vary with signal level. To increase or decrease the on-time parameter value, convert the increase/decrease into hexadecimal and add/subtract to/from the current value.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Equation: Minimum On Time ± [(Increase/Decrease)Sample Rate]h

Function 61 Minimum Off Time (DTMF)

The minimum off time is defined as the minimum period of time of the DTMF signal beginning when the energy falls below the turn-off threshold and ending when a gain hit is detected. The off-time parameter is equal to the desired minimum off-time minus the drop out time. The default off time is set for 40.0 ± 1 ms with a default dropout time parameter of 5.0 ms. To increase or decrease the off-time parameter value, convert the increase/decrease into hex and add/subtract to/from the current value.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Equation: Minimum Off Time ± [(Increase/Decrease)Sample Rate]h (dropout time equal to 5.0 ms).

Function 62 Minimum Cycle Time (DTMF)

The minimum cycle time is defined as the minimum period of the DTMF signal beginning when the signal is detected and ending when the next signal begins. The cycle time parameter is equal to the desired minimum cycle-time minus the dropout time. The default cycle time parameter is set for 93.0 ± 1 ms with a default drop out time parameter of 5.0 ms. To increase or decrease the cycle time parameter value, convert the increase/decrease into hex and add/subtract to/from the current value.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Equation: Minimum Cycle Time ± [(Increase/Decrease)Sample Rate]h (dropout time equal to 5.0 ms).

Function 63 Minimum Dropout Time (DTMF)

The minimum dropout time is defined as the maximum period of the DTMF signal beginning when the signal energy drops below the turn-off threshold and ending when the signal energy returns that is considered to be part of the on time. The default dropout time parameter is set to 5.0 ms.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Equation: [(Desired time)Sample Rate]h

Function 64 Maximum Speech Energy (DTMF)

This parameter specifies the maximum relative speech energy that may be detected and still receive DTMF signals. The speech energy is measured in the frequency region of second or third harmonics of the DTMF tones. To disable the speech energy detector, set this parameter to its full scale positive value (7FFFh). Decreasing the value of this parameter may degrade signal-to-noise ratio (SNR) performance, but may reduce false settings of status bit EDET due to speech signals. To increase or decrease the maximum speech energy parameter value, convert the increase/decrease into hex and add/subtract to/from the current value.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Equation: Maximum Speech Energy ± (Increase/Decrease)h

Function 65 Frequency Deviation, Low Group (DTMF)

This parameter controls the acceptable frequency range for the low group DTMF tones (697, 770, 852, and 941 Hz). Increasing the value of this parameter increases the frequency range. The frequency range will vary from one DTMF symbol to another. To increase or decrease the parameter value, convert the increase/decrease into hex and add/subtract to/from the current value.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Equation: Frequency Deviation ± (Increase/Decrease)h

Function 66 Frequency Deviation, High Group (DTMF)

This parameter controls the acceptable frequency range for the high group DTMF tones (1209, 1336, 1477, and 1633 Hz). Increasing the value of this parameter increases the frequency range. The frequency range will vary from one DTMF symbol to another. To increase or decrease the parameter value, convert the increase/decrease into hex and add/subtract to/from the current value.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Equation: Frequency Deviation ± (Increase/Decrease)h

Function 67 Negative Twist Control, TWIST4 (DTMF)

This parameter controls the acceptable negative twist for the DTMF signals. Decreasing this parameter increases the acceptable negative twist level. The twist will vary from one DTMF symbol to another. To increase or decrease the parameter value, convert the increase/decrease into hex and add/subtract to/from the default value.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Equation: Negative Twist ± (Increase/Decrease)h

Default: 1420h

Function 68 Positive Twist Control, TWIST8 (DTMF)

This parameter controls the acceptable positive twist for the DTMF signals. Decreasing this parameter increases the acceptable positive twist level. The twist will vary from one DTMF symbol to another. To increase or decrease the parameter value, convert the increase/decrease into hex and add/subtract to/from the default value.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Equation: Positive Twist ± (Increase/Decrease)h

Default: 2800h

Function 69 Maximum Energy Hit Time (DTMF)

This parameter represents the duration of an allowed energy impulse during the off time measurement. The default value of 0000h means no gain hits will be tolerated during the off time.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Equation: [(Desired Time)(Sample Rate)]h

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5 HDLC OPERATION

The HDLC (High Level Data Link Control) protocol is a standard procedure used for data communications. SDLC (Synchronous Data Link Control) is a bit-oriented protocol which is a subset of HDLC. The same format is used in both protocols although all SDLC fields must be eight-bit octets. The modem uses the SDLC protocol but it is referred to as HDLC to avoid confusion.

5.1 HDLC FRAMES

Data and control information on a HDLC link are transmitted via frames. These frames organize the information into a format specified by an ISO standard that enables the transmitting and receiving station to synchronize with each other. This format is shown in Figure 5-1. Flags and the frame check sequence are distinguished from the other fields by status bits in the modem interface memory.

Flags

All frames start and end with a flag sequence. The beginning flag and the ending flag are defined by the bit pattern 01111110 (7E). The ending flag for one frame can also serve as the beginning flag for the following frame. If separate ending and beginning flags are used, the final zero in the ending flag of one frame may also serve as the first zero of the beginning flag in the following frame. This process is known as "zero-sharing". The zero-sharing bit pattern is 011111101111110.

Address Field

The address field informs the receiver where the information is to go (if the primary station is transmitting) or where the message originated (if a secondary station is transmitting). This field is eight bits in length for the "basic" format.

For the "extended" format, the length is N number of octets, each octet having the first bit a binary zero with the exception of the last octet that begins with a binary one.

Control Field

The control field defines the function of the frame. It may contain a command or response. The control field might also contain send or/and receive sequence numbers. This field can be in one of the following formats:

1. Information Transfer Format
2. Supervisory Format
3. Unnumbered Format

This field is normally eight bits in length. Certain protocols allow for an extended control field of 16 bits in length.

Information Field

The modem does not distinguish between the address field, the control field, or the information field. The information field does not have a set length; however, this field is in the SDLC protocol format of 8-bit bytes.

Zero Insertion

Since flags mark the beginning and ending of a frame, some method must be implemented to inhibit or alter the transmission of data that appear as flags. The method used is called "zero insertion". HDLC procedures require that a zero be transmitted following any succession of five continuous ones. This includes all data in the address, control, information and Frame Check Sequence (FCS) fields. Use of zero insertion denies any pattern of 01111110 to ever be transmitted between beginning and ending flags.

The modem transmitter always performs zero insertion when in HDLC mode.

Zero Deletion

When transmitting flags, zero insertion is disabled. During reception of data, after testing for flag recognition, the receiver removes a zero that immediately follows five continuous ones. This is termed "zero deletion". A one that follows five continuous ones signifies either a frame abort (i.e., at least seven ones with no zero insertion) or a flag (i.e., 01111110). The sixth one is, therefore, not removed.

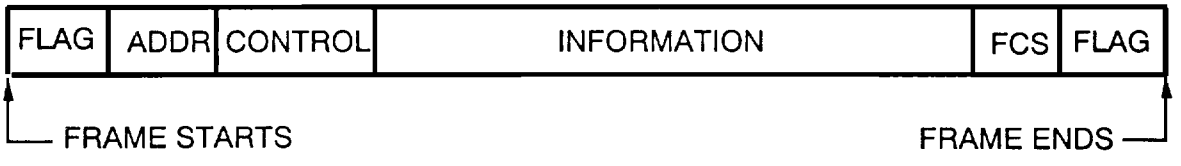


Figure 5-1. HDLC Frame

The modem receiver always performs zero deletion when in HDLC mode.

Frame Check Sequence

The purpose of the Frame Check Sequence (FCS) is to give a shorthand representation of the entire transmitted information field and to compare it to the identically generated shorthand representation of the received sequence. If any difference occurs, the received frame was in error and should be re-transmitted.

The FCS computation is done on all fields within the frame but does not include the flags. A standard Cyclic Redundancy Check (CRC) is used to compute the FCS. Either 16-bit (CRC16) (default) or 32-bit (CRC32) CRC may be selected using the CCITT CRC32 RAM parameter (see parameter 52 in Section 4.4). The CRC polynomials are:

$$CRC16 = x^{16} + x^{12} + x^5 + 1 \quad \text{(SDLC and X.25)}$$

$$CRC32 = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + 1$$

The FCS is sent as two bytes of data immediately preceding the ending flag of the frame. The FCS register is first preset to all binary ones. The register is then modified by shifting in the data (no flags) contained in the address, control, and information fields. Following the last bit of data, the ones complement of the FCS register is transmitted as the FCS. The FCS is transmitted with the highest order bit first.

Frame Abortion, Frame Idle, and Time Fill

Frame abortion prematurely finishes transmission of a frame. This occurs by sending at least seven consecutive ones with no zero insertion. This abort pattern terminates a frame immediately and does not require a FCS or an ending flag.

An abort pattern followed by a minimum of eight additional consecutive ones idles the data link. Thus, seven to fourteen ones establish the abort pattern; fifteen or more ones constitute an idle pattern.

Interframe time fill is accomplished by transmitting continuous flags.

5.2 OPERATION

5.2.1 Transmitter and Receiver Setup

To select HDLC mode, the host must:

1. Set the CONF bits to the desired modem configuration. HDLC can be used in all data modes except the full-duplex FSK modes (i.e., V.21, V.23, and Bell 103).
2. Reset the ASYN bit to select synchronous mode, if not already in synchronous mode.
3. Set the TPDM bit to select Transmitter Parallel Data Mode (transmitting only). Setting TPDM is not required when receiving since received data is always available in RBUFFER. Note that HDLC transmission cannot be performed using the serial interface (TPDM = 0).
4. Set the RTS bit to turn on RTS (transmitting only).
5. Set the HDLC bit to select HDLC mode.
6. Set the NEWC bit.

5.2.2 Transmitter HDLC Operation

The format of the data input to the modem is in groups of 8-bit bytes. As in the normal synchronous parallel data mode, the least significant bit of the byte is transmitted first.

Flag Transmission and Reception

In HDLC mode, the modem will send continuous flags with no zero sharing (i.e., 0111111001111..) until the host loads data into the Transmit Data Buffer, TBUFFER (register 10). Thus, the modem defaults to transmitting time-fill and keeps the receiving link station active. The status bit FLAGS (0A:1) is set to indicate that the modem is transmitting the flag sequence.

Information Field Transmission and Reception

The host must load the data into TBUFFER and then wait for the Transmit Data Buffer Empty bit, TDBE (1E:3), to be set by the modem before loading in the next byte of data. If the FIFO is not enabled (FIFOEN bit = 0), if the next byte is not loaded into TBUFFER within the next eight bit times, the modem interprets this as the end of a frame. If the FIFO is enabled (FIFOEN bit = 1), the TEOF bit must be set by the host to indicate that the next byte to be written into TBUFFER is the last byte in the frame.

FCS and Ending Flag Transmission and Reception

Following the detection end of frame, the modem automatically sends the FCS and ending flag. Status bit CRCS (0A:2)is set just before the highest order bit is sent to indicate that the FCS is being transmitted. Once the host sees this bit set, the first byte of the next frame can be loaded. In this case, the ending flag serves as the beginning flag for the next frame. The modem resets the CRCS bit when the ending flag is transmitted. At the same time, the modem sets the FLAGS bit .

After the FCS transmission (immediately following bit x^0), the modem sends one flag to signify the end of the current frame and the beginning of the next frame. After the final zero in a flag is transmitted, the modem looks to see if the host has loaded new data into TBUFFER. If no new data is loaded before this time, another flag is sent. Therefore, if more than one flag between frames is desired, the host must wait N-1 multiples of eight bit times after FLAGS is set by the modem to load new data into TBUFFER, where N is the number of flags. The host then has seven bit times in which to load new data and thus prevent another flag from being sent. For example, if three flags are desired between frames, the host must wait at least 16 bit times

and not more than 23 bit times after FLAGS is set by the modem.

Abort/Idle Sequence Transmission and Reception

An abort/idle sequence can be sent by the host setting the MHLD bit (07:0). The modem stops sending any normal frame transmission, as well as continuous flag transmission, and sends continuous ones. To stop sending continuous ones, the host must reset MHLD. Then, if no new data is loaded into TBUFFER, the modem sends continuous flags. If new data is loaded into TBUFFER, the modem sends a beginning flag and then the data in TBUFFER.

5.2.3 Receiver HDLC Operation

The format of the data output to the host is in groups of 8-bit bytes. As in the normal synchronous parallel data mode, the least significant bit of the byte is transmitted first.

Flag Transmission and Reception

The modem receiver continually searches for the flag data pattern. When one or more flags are detected, status bit SYNCD (0A:0) is set. The flags themselves are not presented to the host through the receiver data buffer RBUFFER (register 00). The host must service the RDBF interrupt while waiting for the SYNC bit to be set to a 1 in order to clear the Receive FIFO of any unwanted or leftover characters and to ensure the alignment of the SYNCD bit with the received flag.

The modem can also detect consecutive flags with zero-sharing.

Information Field Transmission and Reception

Received data between flags is passed to the host through the RBUFFER by the use of the handshaking bit RDBF (1E:0). The host must wait for RDBF to be set by the modem reading the data. Note that the RBUFFER and Receive FIFO can accumulate nine bytes before overflowing. If the host does not read the data within nine byte times, the data in RBUFFER will be overwritten by the next received byte and the Overrun Error bit (0A:3) will be set. The flag sequence and abort/idle sequence are not presented to the user. The receiver determines where the FCS field is by detecting the ending flag. There is at least a 16-bit time delay in the reception of data.

FCS and Ending Flag Transmission and Reception

Upon the receipt of an ending flag in the current frame (which may also be the beginning flag of the next frame), the receiver checks the data in the FCS register. If the FCS register remainder is correct, the PE bit (0A:5) is left a zero. If the remainder is incorrect, the PE bit is set. The FCS field is also passed to the host, in case the host wishes to do his own CRC checking. The receiver will set the SYNCD bit and the PE bit (if the modem detected a frame with a bad CRC) after sending the FCS to the host. The modem does not change the PE bit until the end of the next frame when a correct or incorrect frame is determined. However, the host can reset this bit anytime. The modem presets the FCS register to all ones after one or more flags are received.

After the FCS transmission (immediately following bit x^0), one flag is sent to signify the end of the current frame and the beginning of the next frame. After the final zero in a flag is transmitted, the modem looks to see if the host has loaded new data into TBUFFER. If no new data is loaded before this time, another flag is sent. Therefore, if more than one flag between frames is desired, the host must wait N-1 multiples of eight bit times after FLAGS is set by the modem to load new data into TBUFFER, where N is the number of flags. The host then has seven bit times in which to load new data and thus prevent another flag from being sent. For example, if three flags are desired between frames, the host must wait at least 16 bit times and not more than 23 bit times after FLAGS is set by the modem.

Abort/Idle Sequence Transmission and Reception

The modem receiver not only continually searches for flags, but also continually searches for an abort/idle sequence. When the modem detects this data pattern, it sets the FE bit (0A:4). After the modem sets the FE bit, it does not change the bit until the end of the next frame when the abort/idle sequence is again determined. However, the host can reset the FE bit anytime. Then, if an abort/idle sequence is detected during the next frame, the modem will again set the FE bit. The reception of data following the abort/idle sequence is treated as invalid data and is not presented to the host. Therefore, to re-establish transmitter and receiver synchronization, the receiver must see at least one flag. Remember, the abort/idle sequence is not output through the RBUFFER register.

5.3 EXAMPLE APPLICATION

Refer to Table 3-1 for a description of the bits associated with the HDLC functions. Figure 5-2 illustrates bit timing.

5.3.1 Transmitter Example (Tx FIFO Disabled)

The steps to perform a typical HDLC transmission with the Transmitter FIFO disabled are (Figure 5-2a):

1. Set the modem configuration in CONF; reset the ASYN and FIFOEN bits; set the HDLC, TPDM, and RTS bits.
2. The modem starts transmitting flags immediately and continues with flags until the first byte of data is loaded into TBUFFER.
3. Place the first byte of data into TBUFFER. The modem finishes transmitting the current flag followed by this byte of data.
4. As soon as TDBE is set, load in the next byte of data. This must occur within eight bit times of TDBE being set.

5. After all information but the last byte is given to the modem, load in the last byte of data in the frame as in step 4.
6. Wait until FLAGS is set to load in the first byte of the next frame. The modem follows the last byte of the current frame with the FCS and a flag.
7. Repeat steps 4 through 6 for all frames to be transmitted.

5.3.2 Transmitter Example (Tx FIFO Enabled)

The steps to perform a typical HDLC transmission with the Transmitter FIFO enabled are:

1. Set the modem configuration in CONF; reset the ASYN bit; set the FIFOEN, HDLC, TPDM, and RTS bits.
2. The modem starts transmitting flags immediately and continues with flags until the first byte of data is loaded into TBUFFER.
3. Place the first byte of data into TBUFFER. The modem finishes transmitting the current flag followed by this byte of data.
4. As soon as TDBE is set, load in the next byte of data.
5. After all information but the last byte is given to the modem, set TEOF then load in the last byte of data in the frame as in step 4.
6. Repeat steps 4 through 5 for all frames to be transmitted.

5.3.3 Receiver Example

The steps to perform a typical HDLC reception are (Figure 5-2b):

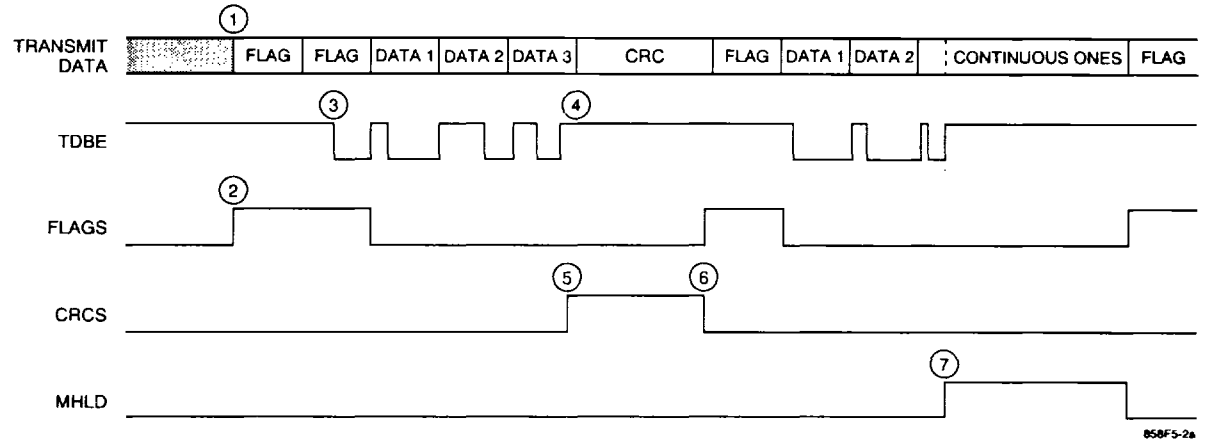
1. Set the modem configuration in CONF; reset the ASYN bit; set the HDLC bit. Then monitor, through interrupts, the RDBF, OE, SYNCD, PE, and FE status bits.
2. Wait for an interrupt. If it is caused by the modem setting RDBF (RDBIA is also set by the modem), read the data in RBUFFER. The modem will set the NEWS and NSIA bits if any of the other bits caused the interrupt.

   OE indicates that RBUFFER was loaded with new data before the host read the old data.

   SYNCD indicates that the modem is receiving flags.

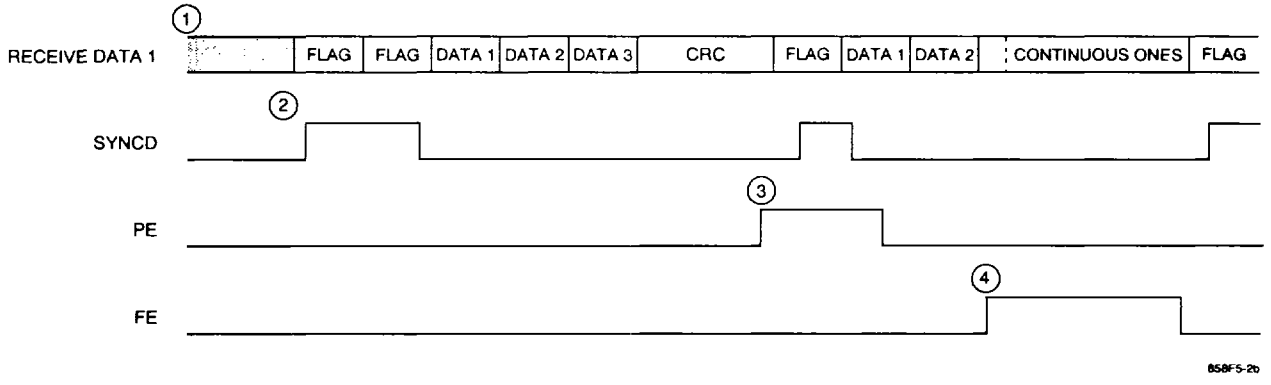
   PE indicates that the FCS had an incorrect CRC.

   FE indicates that an abort/idle sequence is detected and the frame that was aborted is invalid. The modem does not set the PE bit in this case since no FCS checking is done.
3. Continue waiting for interrupts and take appropriate action when the interrupts are received.



1. The host enters HDLC mode by setting HDLC bit.
2. The modem sets FLAGS prior to sending the first bit of the first 7E flag.
3. If the host loads the first data byte into TBUFFER while FLAGS is being sent, the data will not be sent until the flag is completely sent.
4. After TDBE is set, the host has 8 bit times to load new data into TBUFFER.
5. CRCS is set as soon as the last bit of the last data byte is sent and prior to sending the first bit of the CRC sequence. As soon as FLAGS is set, a new data byte of the next frame can be loaded.
6. CRCS is reset and FLAGS is set when the last bit of the CRC sequence is sent.
7. If MHLD is set anytime during the data, CRC, or flag transmission, the byte transmitted is interrupted and the abort sequence is started.

a. Transmitter (FIFOEN = 0)



1. Timing refers to when received data is presented to the host. Flags and the abort sequence are not presented to the host.
2. SYNCD will turn on 8-15 bit times after entering HDLC mode, when 7E flags are detected.
3. PE is set only if a bad CRC is detected by the modem.
4. FE will turn on when seven consecutive 1s are detected.

b. Receiver (FIFOEN = 0)

Figure 5-2. HDLC Signal Timing

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6 HOST FUNCTIONS

6.1 RETRAIN AND AUTOMATIC RATE CHANGE

V.32 defines retrain and automatic rate change. This section explains how to perform the retrain and rate change.

6.1.1 Retrain Without a Rate Change

V.17 Configurations

When the RTRN bit is set to a 1 and the ARC bit is reset to a 0, the modem will send the training sequence. The modem for which the retrain is intended will detect the training sequence and will retrain. This can be monitored at the transmitter by examining the state of CTS (CTS off means going through training sequence) and at the receiver by examining the RLSD, P2DET, and PNDET bits. Once the retrain is completed, the process is complete. The modem which was retrained does not respond with a retrain. It is up to the user to set the retrain bit for this to occur.

V.32/V.32 bis and V.22 bis Configurations

When the RTRN bit is set to a 1, the modem will initiate the retrain sequence. The modem which detects the retrain sequence will respond with training, and both modems will proceed with the proper training sequence. The retrain process can be monitored by observing the appropriate status bits in the transmitter and receiver.

6.1.2 Retrain With a Rate Change

V.32/V.32 bis and V.22 bis Configurations

The following procedure describes how to obtain a rate change (V.32) along with a retrain.

1. Set ARC to a 1 to enable the automatic rate change.
2. Store the desired configuration in the CONF register. Use configuration code 82h (V.22 bis/1200) for fall forward or fallback between 2400 bps and 1200 bps.

   NOTE: Do not set the NEWC bit.
3. Set the RTRN bit to a 1.

The modem will then send the retrain sequence at the correct operating speed as selected in the configuration registers. The rate sequence is automatically changed in the training sequence to tell the other modem at what speed to operate. The status bits will change as mentioned above and the CTS bit will be set to a 1 when the retrain sequence is completed. (See the RREN bit description in Section 3 for rate change procedures in V.32 bis by means of a rate renegotiation rather than a retrain.)

6.2 MODEM SELF TEST INFORMATION

After a power-on reset, the modem performs a self test of the internal controller (C26) and DSP (C59) devices. After each self test, the test results and configuration information is loaded into interface memory. Bit 1E:3 (TDBE) is then set to indicate that the test is complete and the test results can be read.

Figure 6-1 shows the flowchart for reading the self test data.

The controller self test is performed first. Upon test completion, the following test results and configuration information is loaded into interface memory and bit 1E:3 is set to a 1:

Register	Function	Value (Hex)	Value Type
1D, 1C	RAM1 Checksum	A6BB	Constant
1B, 1A	RAM2 Checksum	5164	Constant
19, 18	ROM1 Checksum	412B	Constant
17, 16	ROM2 Checksum	422C	Constant
15	Timer/ROM/RAM	0F	Constant
13, 12	Part Number	3030	ASCII 00
11, 10	Revision Level	4343	ASCII CC

The host should read the test results within 5 ms of bit 1E:3 being set. Register 10 should be read last since reading register 10 resets bit 1E:3.

When bit 1E:3 is reset or 5 ms has expired since bit 1E:3 was set, the information is cleared and the DSP self test is performed. If the register 10 is not read by the host, bit 1E:3 will not be reset.

Upon completion of DSP self test, the following test results and configuration information is loaded into interface memory and bit 1E:3 is set to a 1:

Register	Function	Value (Hex)	Value Type
1B, 1A	EC Checksum	267F	Constant
19, 18	Multiplier Checksum	46EE	Constant
17, 16	RAM Checksum	CB42	Constant
15, 14	ROM Checksum	3539	Constant
13, 12	Part Number	3030	ASCII 00
11, 10	Revision Level	2046	ASCII F

The host should read the test results within 5 ms of bit 1E:3 being set. Register 10 should be read last since reading register 10 resets bit 1E:3.

When bit 1E:3 is reset or 5 ms has expired since DSP test completion, the information is cleared and modem initialization continues.

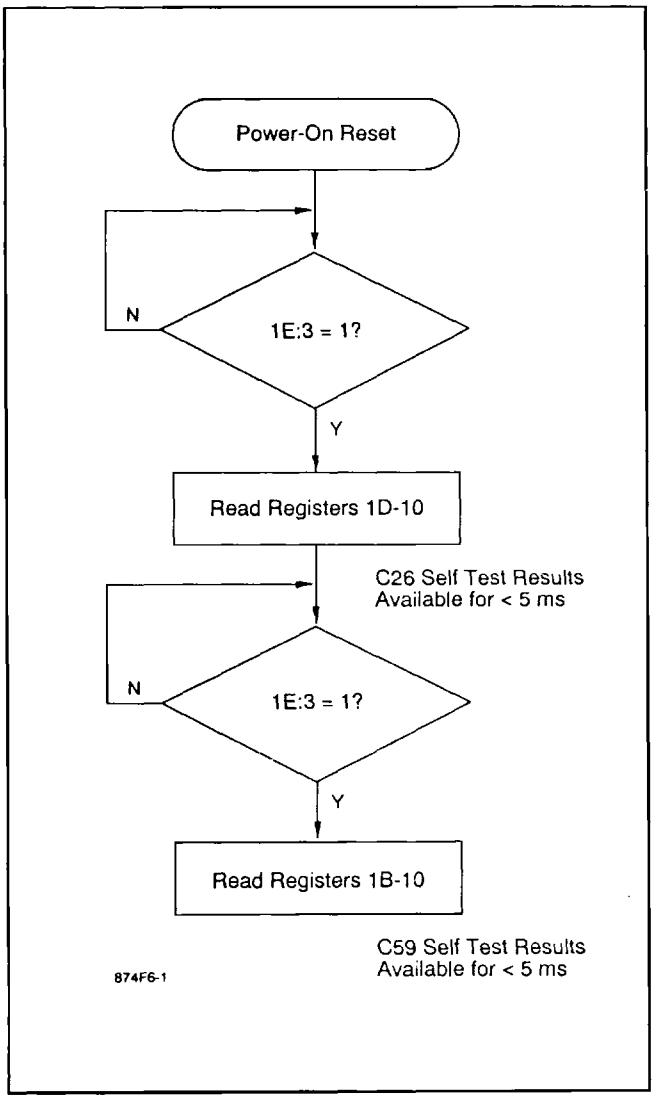


Figure 6-1. Modem Self Test Results Read Procedure

6.3 HANDSHAKE TIMEOUT TIMERS

If any part of the handshake is not detected, the modem will time out and abort the handshake. In this case, the transmitter will immediately stop sending the training sequence. Also, the modem, upon timing out, will load an error code into register 14 (ABCODE) of interface memory that indicates that point in the handshake the timeout occurred. The error code is not cleared even if the modem immediately goes into a new handshake after aborting. The user can observe this register during the handshake to determine if an abort occurred.

The user can progressively observe the handshake detector bits (AADET, ACDET, CCDET, etc.) to determine how the handshake is proceeding. The user can thus be interrupted at each step of the handshake progression.

The V.32 handshake error codes and their meanings are:

Error Code	Reason For Aborting (Time-out)
00	No error
01	FED went off while waiting to get into round trip delay estimate.
10	Unexpected E-sequence, do retrain.
81	FED lost during round trip delay estimate.
82	Lost track of AC/AA/CA/CC during round trip delay estimate.
84	Timed out waiting for first S-sequence from ANS modem.
85	Timed out waiting for second S-sequence from ANS modem.
86	Timed out waiting for S-sequence from ORG modem.
8C	Lost FED during first TRN-sequence from ANS modem.
8D	Lost FED during second TRN-sequence from ANS modem.
8E	Lost FED during TRN-sequence from ORG modem.
90	R1 not detected.
91	R2 not detected.
92	R3 not detected.
93	R4/R5 not detected.
97	E-sequence not detected.

7 ADPCM VOICE COMPRESSION AND DECOMPRESSION

ADPCM compression (Rx-coding) of received, ADC digitized voice may be selected to minimize the memory required for message storage. Silence detection and deletion may also be selected to further reduce the memory storage requirements.

ADPCM decompression (Tx-decoding) of stored/recorded compressed voice may be selected in order to either playback or transmit messages. Silence interpolation may be enabled to interpolate any silence deleted during reception.

Data flow through the Rx-coder and Tx-decoder are shown in Figures 7-1 and 7-2, respectively.

7.1 ADPCM RECEIVER (RX-CODER)

7.1.1 Mode Selection

ADPCM Rx-coding is selected when Coder Enable (CDEN) is set in Receive Voice Mode [i.e., Transmit Single Tone, Transmit Dual Tone, Dialing, or DTFM Receiver configuration (CONF = 80, 83, 81, or 86) and Receive Voice (RXV) is set]. (See Table 7-1.)

Squelching the transmitter output by setting the TXSQ bit will prevent the TXA1 and TXA2 noise floor from being coupled back into the RXA input when receiving voice samples in(either pass-through or ADPCM voice mode.

7.1.2 Operation

When Rx-coding is selected, received analog voice from the RXA input is sampled, converted to digital, digitally scaled, compressed (coded), compressed for silence (if silence detection/deletion is enabled), then passed to the 16-bit Voice Receive Buffer (VBUFRM and VBUFRL) where the speech samples can be read by the host (Figure 7-1). Typical receive ADPCM voice mode operation is illustrated in Figure 7-3.

The host must select 2, 3, or 4 bits per sample compression with the Coder No. of Bits (CODBITS). With 2, 3, or 4 bits per sample at the 7.2k Hz default programmable sample rate, the 16-bit coder output words are provided at 14.4k, 21.6k, or 28.8k bps (900, 1350, or 1800 16-bit words per second), respectively. The specific application will dictate a higher bits/sample rate for best speech quality or a lower bits/sample rate for minimum storage requirements.

If enabled by the Silence Coder Enable (SCDE) bit, silence detection and deletion provides additional compression (see Section 7.3.1).

The Rx-coder writes 16-bit coded words to output register VBUFRM (most significant byte) and VBUFRL (least significant byte) then sets status bit RDBF. The IRQ output may be enabled using the RDBIE bit to interrupt the host whenever the RDBF bit sets to indicate that VBUFR is full.

7.2 ADPCM TRANSMITTER (TX-DECODER)

7.2.1 Mode Selection

ADPCM Tx-decoding is selected when Decoder Enable (DCDEN) is set in Transmit Voice Mode [i.e., Transmit Single Tone, Transmit Dual Tone, Dialing, or DTFM Receiver configuration (CONF = 80, 83, 81, or 86) and Transmit Voice (TXV) is set]. (See Table 7-1.)

7.2.2 Operation

When TX-decoding is selected, compressed digital voice samples (coded words) received from the host through the 16-bit Voice Transmit Buffer (VBUFTM and VBUFTL) are decompressed (decoded), decompressed for silence (if silence interpolation is enabled), digitally scaled, converted to analog, then routed to the TXA1 and TXA2 outputs (Figure 7-2). Typical transmit ADPCM voice mode operation is illustrated in Figure 7-4.

Table 7-1. ADPCM Voice Mode Selection

CONF	RXV	TXV	CDEN	DCDEN	SCDE	SDCDE	Mode	Silence Detection & Insertion	Silence Interpolation
*	0	1	0	0	DC	DC	Tx Pass-through Voice Mode	NA	NA
*	0	1	1	0	0	DC	Tx ADPCM Voice Mode	No	NA
*	0	1	1	0	1	DC	Tx ADPCM Voice Mode	Yes	NA
*	1	0	0	0	DC	DC	Rx Pass-through Voice Mode	NA	NA
*	1	0	0	1	DC	0	Rx ADPCM Voice Mode	NA	No
*	1	0	0	1	DC	1	Rx ADPCM Voice Mode	NA	Yes

NOTES:
* = 80h, 81h, 83h, or 86h.
DC = Don't care
NA = Not applicable

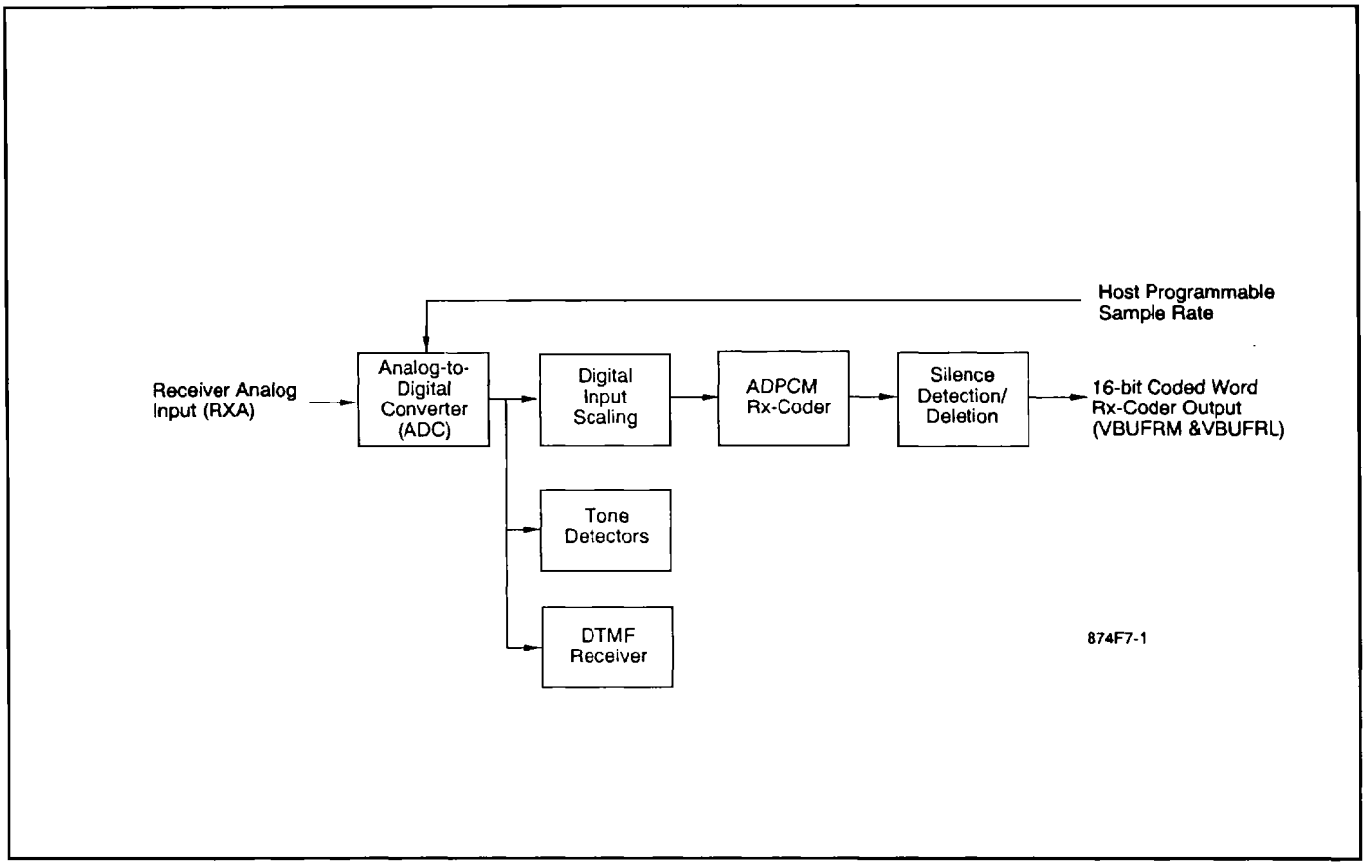


Figure 7-1. ADPCM Rx-Coder

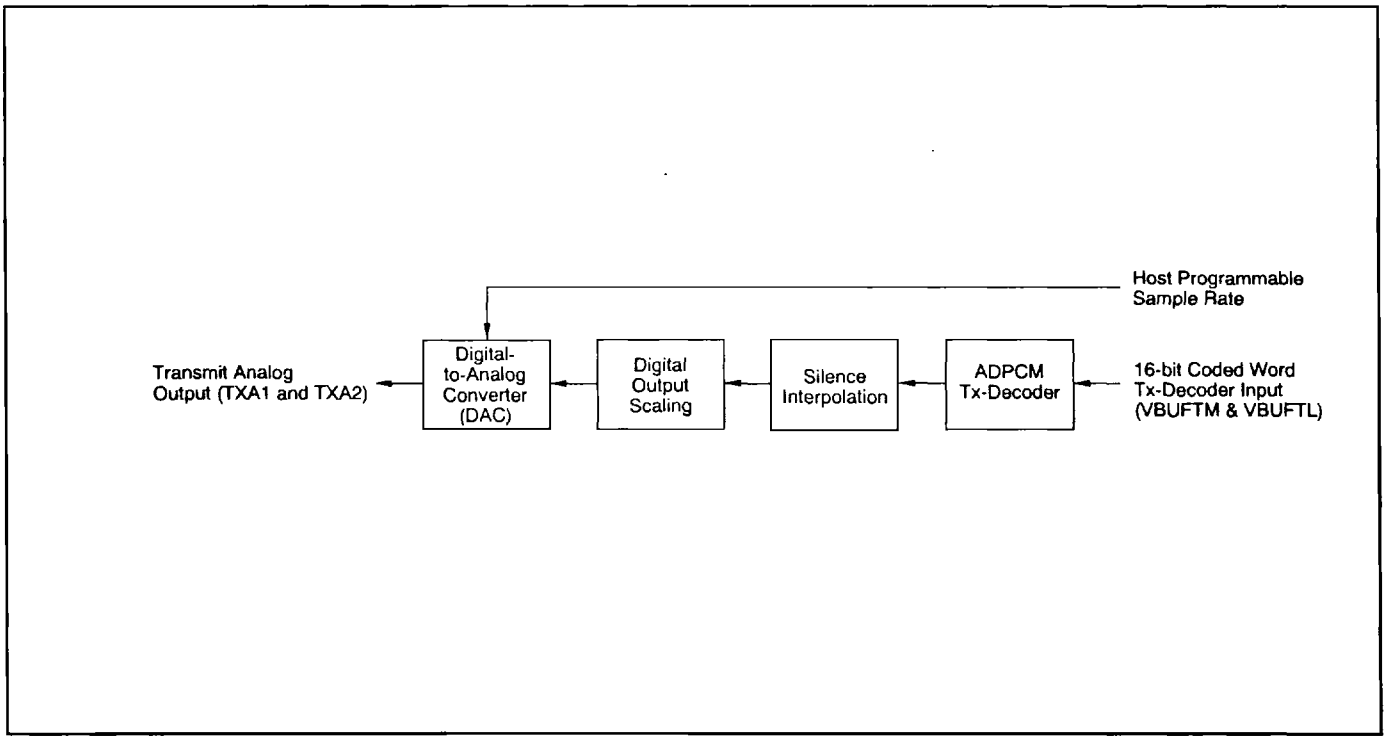
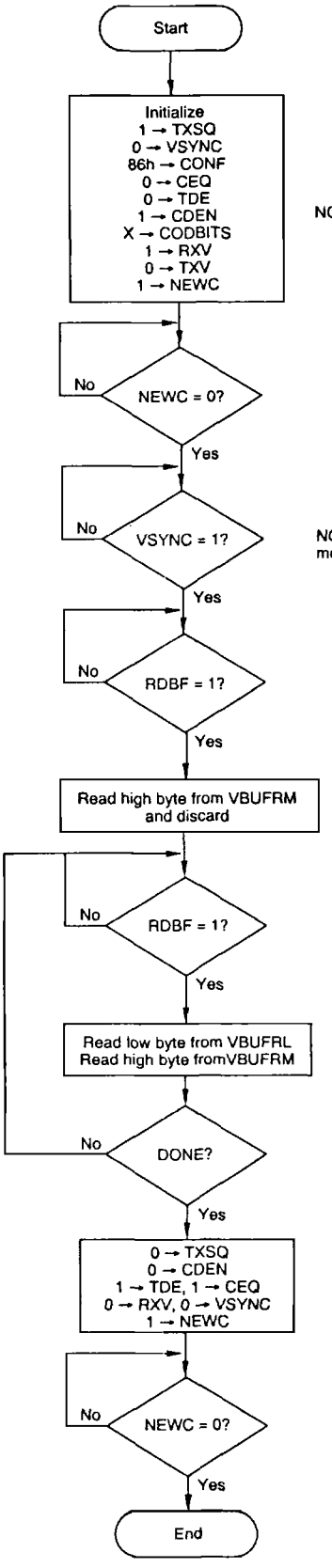


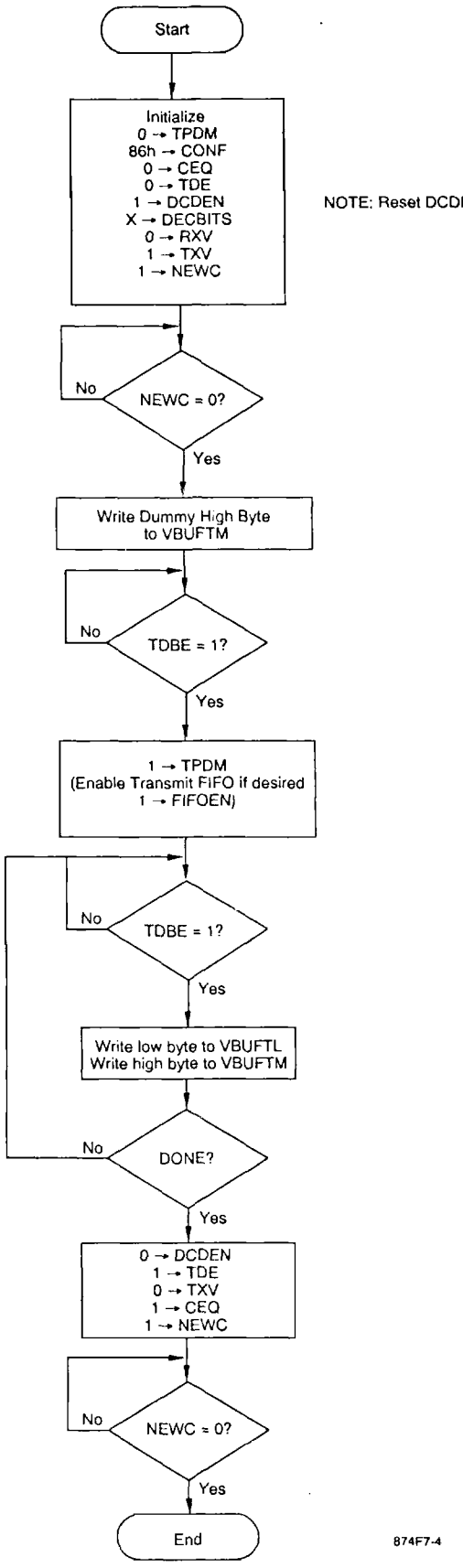
Figure 7-2. ADPCM Tx-Decoder



NOTE: Reset CDEN = 0 for 16-bit pass-through voice mode.

NOTE: VSYNC check is required for ADPCM voice mode only, not pass-through voice mode.

Figure 7-3. Rx-Coder Operation



NOTE: Reset DCDEN = 0 for 16-bit pass-through voice mode.

Figure 7-4. Tx-Decoder Operation

The host must select 2, 3, or 4 bits per sample decompression with the Decoder No. of Bits (DECBITS).

If enabled by the Silence Decoder Enable (SDCDE) bit, silence interpolation is performed to reconstruct deleted silence from stored voice samples and white noise is inserted (see Section 7.3.2). The programmable white noise level may be set to zero for absolute silence insertion.

The host supplies the decoder with the 16-bit coder output words by writing to VBUFTM (most significant byte) and VBUFTL (least significant byte) when TDBE is set.

7.3 SILENCE DETECTION/DELETION AND SILENCE INTERPOLATION PROGRAMMING GUIDE

Silence detection and deletion reduces the bit rate necessary to digitally record speech via ADPCM compression. "Background noise deletion" is a more accurate description, and the term "silence" is used with the understanding that it represents "background noise."

Because speech quality is highly subjective, the silence deletion feature is host programmable. The modem system designer may program ADPCM parameter values to achieve desired speech quality required for specific applications. These parameters basically determine how much silence is deleted.

7.3.1 Rx-Coder Silence Deletion (Recording)

When Rx-coding is selected, prior to silence detection, the Rx-coder passes the coded output, 16 bits at a time, to the host. Once silence is detected, a maximum of 32,768 sample periods may pass before any more data is given to the host. Once this maximum time interval is reached or speech is detected, a 16-bit code word is passed to the host. The next 16-bit coder output represents the full or partial duration of the detected silence interval.

Silence interval measurements continue until speech is detected.

Silence length coding is shown in Figure 7-5a, first for the silence interval less than 32,768 sample periods, and then for the silence interval greater than 32,768 sample periods.

7.3.2 Tx-Decoder Silence Interpolation (Playback)

When TX-decoding is selected, ADPCM decompression is halted upon recognizing the silence codeword in the Tx-decoder input from the host, White noise is inserted and transmitted for the duration of the silence interval previously deleted by the ADPCM Rx-coder.

Note that inserting low level white noise (not absolute silence) during playback of silence intervals improves perceived speech quality.

The amount of white noise inserted can be reduced or eliminated using the RANOISE parameter (see parameter #55 in Section 4.4).

7.3.3 Parameter Selection Guidelines

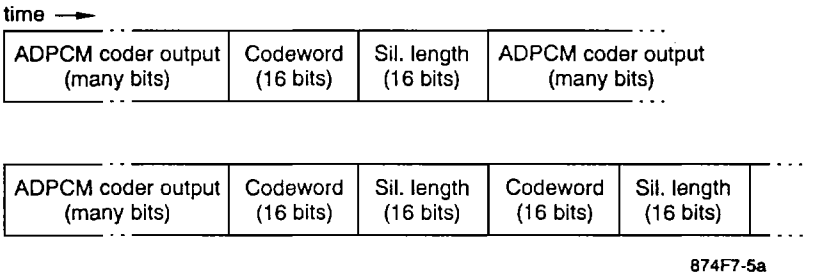
Four parameters are used to detect speech and silence: MTHRESH, SILSPE, SPESIL, and MADAPT (see parameters #56, #57, #58, and #59, respectively, in Section 4.4).

If silence deletion is to be used on prerecorded speech files, these parameters may be changed for each file to achieve maximum speech quality and compression.

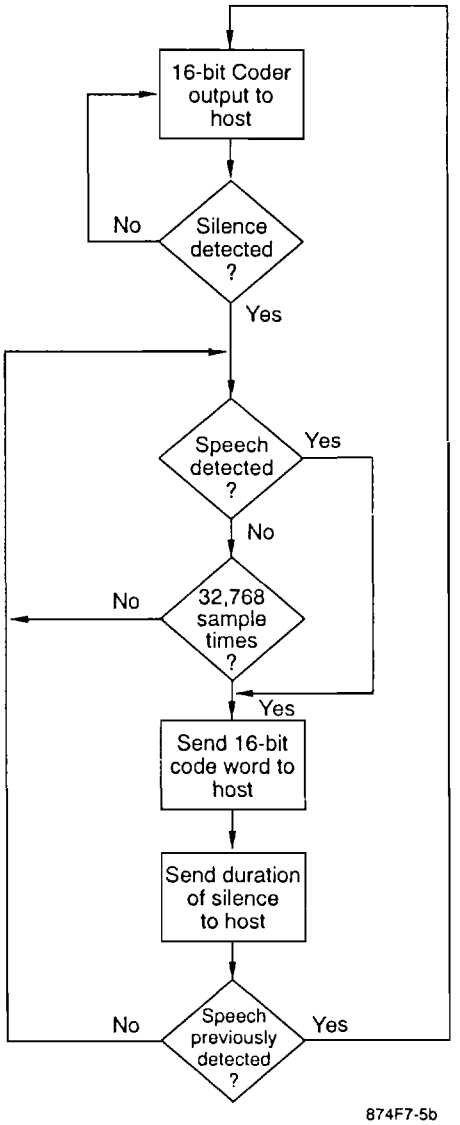
The following is a suggested interactive method for selecting parameter values to achieve more or less silence deletion (see Figure 7-6):

NOTE: The parameter values must be changed after first voice sample is received or sent since default values are loaded by the voice mode initialization.

1. To evaluate the amount of silence being deleted, increase the inserted noise level by increasing RANOISE. Once all other parameter values are selected, reduce RANOISE to an acceptable level.
2. Record and playback the desired file using the parameter default values (except RANOISE).
3. If speech is deleted, do the following:
   a. If the beginning of words are deleted, raise SPESIL so that the silence-to-speech transition is detected earlier.
   b. If the ends of words are deleted, raise SILSPE so that the speech-to-silence transition is detected later.
   c. If raising SILSPE and SPESIL in (a) and (b) above have minimal effects, raise MADAPT.
   d. Keep MADAPT as low as possible. MADAPT is too low if speech is being deleted at any point during playback.
4. If not enough silence is deleted, raise MTHRESH until some speech is deleted, and repeat the procedure starting at step 3.



a. Silence Length Format



b. Rx-Coder Silence Deletion Procedure

Figure 7-5. Rx-Coder Silence Deletion

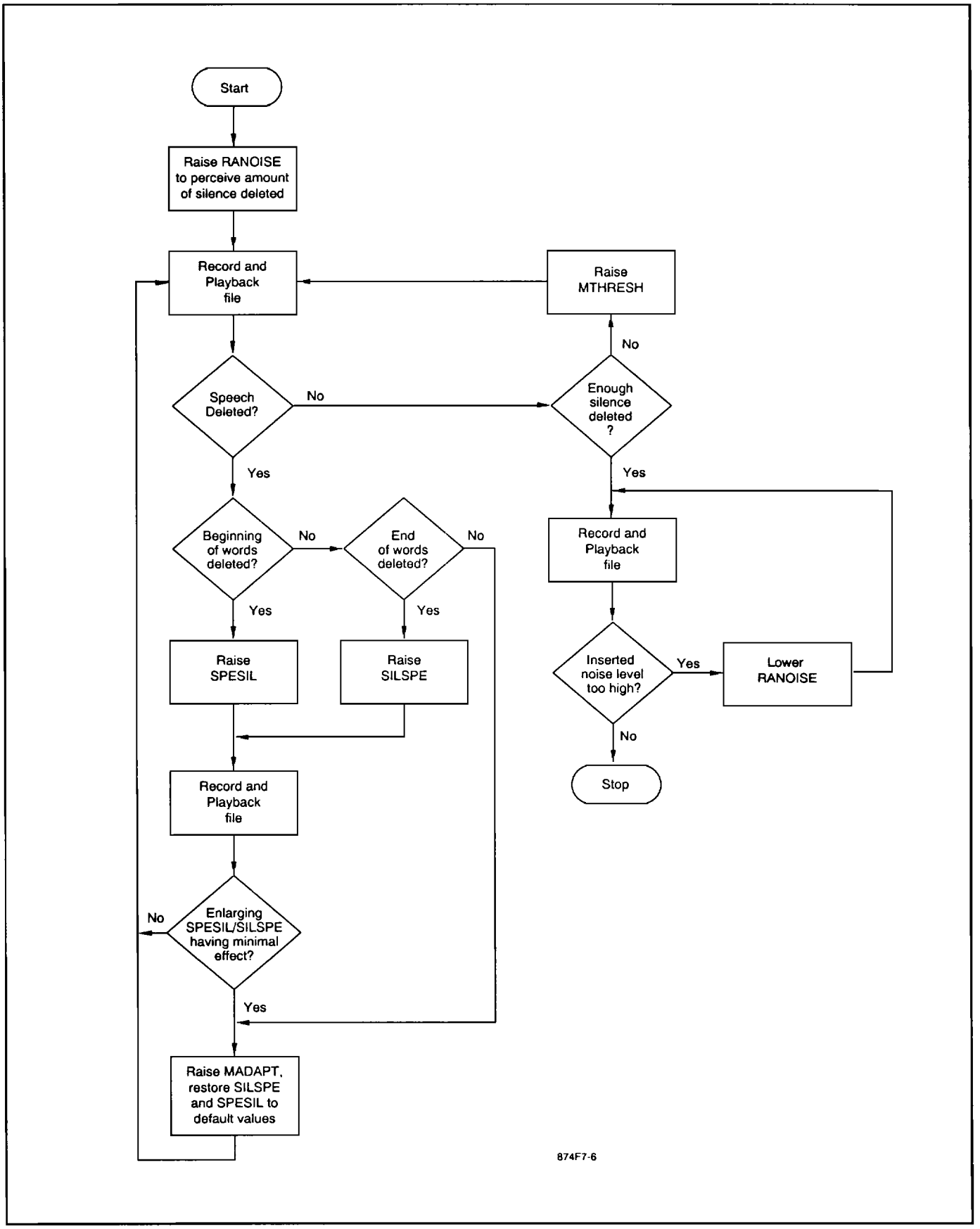


Figure 7-6. Silence Parameter Selection Procedure

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8 DESIGN CONSIDERATIONS

Good engineering practices must be adhered to when designing a printed circuit board (PCB) containing the modem device set. Suppression of noise is essential to the proper operation and performance of the modem itself and for surrounding equipment.

Two aspects of noise in an OEM board design containing the modem device set must be considered: on-board/off-board generated noise that can affect analog signal levels and analog-to-digital conversion (ADC)/digital-to-analog conversion (DAC), and on-board generated noise that can radiate off-board. Both on-board and off-board generated noise that is coupled on-board can affect interfacing signal levels and quality, especially in low level analog signals. Of particular concern is noise in frequency ranges affecting modem performance.

On-board generated electromagnetic interference (EMI) noise that can be radiated or conducted off-board is a separate, but equally important, concern. This noise can affect the operation of surrounding equipment. Most local governing agencies have stringent certification requirements that must be met to allow use in specific environments.

Proper PC board layout (component placement, signal routing, trace thickness and geometry, etc.), component selection (composition, value, and tolerance), interface connections, and shielding are required for the board design to achieve desired modem performance and to attain EMI certification.

All the aspects of proper engineering practices are beyond the scope of this designer's guide. The designer should consult noise suppression techniques described in technical publications and journals, electronics and electrical engineering text books, and component supplier application notes. Seminars addressing noise suppression techniques are often offered by technical and professional associations as well as component suppliers.

8.1 PC BOARD LAYOUT GUIDELINES

1. Provide an adequate ground.
   a. In a 2-layer design, provide a ground grid in all unused space around and under components (judiciously near analog components) on both sides of the board and connect in such a manner as to avoid small islands. A grid is preferred over a plane to improve solderability. Typically, the grid is composed of .012 in. traces and .012 in. spaces on a .025 in. grid. Connect each grid to other grids on the same side at several points and to grids on the opposite side through the board at several points. Connect all modem DGND and AGND pins to the ground grid.
   b. In a 4-layer design, provide a ground plane covering the entire board. Connect all modem DGND and AGND pins to the ground plane at a single point.
2. As a general rule, route digital signals on the component side of the PCB and the analog signals on the solder side. The sides may be reversed to match particular OEM requirements. Route the digital traces perpendicular to the analog traces to minimize signal cross coupling.
3. Route the modem signals to provide maximum isolation between noise sources and noise sensitive inputs. When layout requirements necessitate routing these signals together, they should be separated by neutral signals. The modem noise source, neutral, and noise sensitive pins are listed in Table 8-1.
4. All power and ground traces should be at least 0.05 inch wide.
5. Keep all traces and component leads connected to crystal input and output pins (e.g., XTLI and XTLO) short in order to reduce induced noise levels and minimize any stray capacitance that could affect the crystal oscillator. Keep the XTLO trace extremely short with no bends greater than 45 degrees and containing no vias since the XTLO pin is connected to a fast rise time, high current driver.
6. Connect crystal can(s) to ground.
7. Locate the the modem device(s) and all supporting analog circuitry, including the data access arrangement, on the same area of the PCB.
8. Locate the analog components close to and on the side of board containing the TXA1, TXA2, and RIN signals.
9. Avoid placing noisy components and traces near TXA1, TXA2, RIN and VREF lines.
10. Locate receivers and drivers for DTE EIA-232 serial interface signals close to the connectors and away from traces carrying high frequency clocks in order to avoid/minimize the addition of noise suppression components (i.e., chokes and capacitors) for each line.
11. Route modem interconnect signals (e.g., TMODE to RMODE or TXDAT to SR4OUT) directly to the interfacing by the shortest possible route avoiding all analog components.
12. Provide an RC network on the +5VA supply in the immediate proximity of the +5VA pin to filter out high frequency noise above 115 KHz. A tantalum capacitor is recommended (especially in a 2-layer board design) for improved noise immunity with a current limiting series resistor or inductor to the +5V supply which meets the RC filter frequency requirements.

Table 8-1. Modem Pin Noise Characteristics

Device	Function	Noise Source	Neutral	Noise Sensitive
MDP	+5VD, +5VA		11, 21, 36, 41, 56	
68-Pin PLCC	DGND, AGND		10, 19, 22, 30, 40, 43, 55	
	Crystal	12-13		
	Control			
	Eye Pattern	46-47	48	
	Line Interface		6, 28, 31	23, 26-27
	Speaker Interface	29		
	Serial/LED Interface	35, 50, 52, 54	51	
	MCU Interface	9, 14-18, 20, 35, 60-68	8, 59	
	MDP Interconnect		2-4, 32-33, 38-39, 44-45, 53	
	No connection (NC)		5, 37, 42, 49, 58	
MDP	+5VD, +5VA		25, 35, 45, 56, 86	
100-PQFP	DGND, AGND		16, 21, 30, 37, 43, 66, 80-81, 97	
	Crystal	87-88		
	Control			
	Line Interface		26, 46, 78	28-29, 38
	Speaker Interface	44		
	MCU Interface	1-6, 13, 82, 89-96		
	MDP Interconnect	12, 17-19, 23-24, 36, 47-48, 50, 53-54, 57-65, 67-69, 83-84, 99-100	70, 72, 76,	
	Serial/LED Interface	9-10, 13-14	11	
	No connection (NC)		7, 15, 22, 31-34, 41-42, 49, 51-52, 55, 71, 77, 79, 85, 98	
MDP	+5VD, +5VA		29-30, 39, 41, 52, 74-75	
80-PQFP	DGND, AGND		11-13, 31-32, 50, 72-73, 76	
	Control			
	Eye Pattern	1, 6	10	
	MDP Interconnect	5, 7-8, 14, 23-28, 33-38, 42-46 70-71, 77	63, 67	62
	Serial/LED Interface	15, 18, 22,	17	
	No connection (NC)		2-4, 9, 16, 19, 21, 40, 47-49, 51, 53-61, 64-66, 69,78-80	

13. Provide a 0.1 μF ceramic decoupling capacitor to ground between the high frequency filter and the +5VA pin.
14. Provide a 0.1 μF ceramic decoupling capacitor to ground between the +5V supply and the +5VD pin.

8.2 Electromagnetic Interference (EMI) Considerations

The following guidelines are offered to specifically help minimize EMI generation. Some of these guidelines are redundant with or similar to the general guidelines but are *mentioned to reinforce their importance.*

In order to minimize the contribution of the modem device set-based design to EMI, the designer must understand the major sources of EMI and how to reduce them to acceptable levels.

1. Keep the crystal/oscillator and other related external components as close to the device XTLI and XTLO pins as physically possible.
2. Keep any traces carrying high frequency signals as short as possible.
3. Provide a good ground plane or grid. In some cases a multilayer board may be required with full layers for ground and power distribution.
4. Decouple power to ground with decoupling capacitors as close to the modem device power pins as possible.
5. Eliminate ground loops, which are unexpected current return paths, to the power source.
6. Decouple the telephone line cables at the telco jacks. Typically, use a combination of series inductors, common mode chokes, and shunt capacitors. Methods to decouple telco lines are similar to decoupling power lines, however, telco line decoupling may be more difficult and deserves additional attention. A commonly used design aid is to place footprints for these components and populate as necessary during performance/EMI testing and certification.
7. Decouple the power cord at the power cord interface with decoupling capacitors. Methods to decouple power lines are similar to decoupling telephone lines.
8. Locate high frequency circuits in a separate area to minimize capacitive coupling to other circuits.
9. Locate cables and connectors to avoid coupling from high frequency circuits.
10. Lay out the highest frequency signal traces next to the ground grid.
11. If a multilayer board design is used, make no cuts in the ground or power planes and be sure the ground plane covers all traces.
12. Minimize the number of through-hole connections on traces carrying high frequency signals.
13. Avoid right angle turns on high frequency traces. Forty-five degree corners are good, radius turns are better.
14. On 2-layer boards with no ground grid, provide a shadow ground trace on the opposite side of the board to traces carrying high frequency signals. This will be effective as a high frequency ground return if it is three times the width of the signal traces.
15. Distribute high frequency signals continuously on a single trace rather than several traces radiating from one point.

8.3 CRYSTAL SPECIFICATIONS

Recommended crystal specifications are listed in Table 8-2.

8.4 PACKAGE DIMENSIONS

The dimensions of the 68-pin PLCC, 100-pin PQFP, and 80-pin PQFP packages are shown in Figure 8-1.

8.5 RECOMMENDED INTERFACE CIRCUITS

Recommended modem inrterface connections to the modem packaged in PLCC and PQFP are shown in Figures 8-2 and 8-3, respectively.

Typical external circuits for connection to the line are shown in Figure 8- 4 (no external hybrid; transmit level to -7 dBm) and Figure 7-5 (external hybrid; transmit level to 0 dBm). A typical external speaker circuit is shown in Figure 8-6).

Table 8-2a. Crystal Specifications - 333R34-001

Characteristic	Value
Rockwell Part No.	333R34-001
Electrical Specifications	
Frequency, F	35.251200 MHz nom. @ 25°C
Frequency Tolerance	±15 ppm @ 25°C
Frequency Stability	
vs. Temperature	±30 ppm (0°C to 70°C)
vs. Aging	±5 ppm/year
Oscillation Mode	Fundamental
Calibration Mode	Parallel resonant
Load Capacitance, C_L	18 pF nom.
Frequency Variation	±35 ppm (C_L = 16.5 or 19.5 pF)
Shunt Capacitance, C_O	7 pF max.
Series Capacitance, C_1	0.0183 pF typ. @F
Series Inductance, L_1	1.1 mH typ. @F
Series Resistance, R_1	70 W max. @F
Drive Level	1.0 mW max.
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to 85°C
Mechanical Specifications	
Holder Type	UM-1
Third Lead	N/A
Sleeving	N/A

Notes:

Suggested Suppliers:

1. Hy-Q International (USA), Inc.
   Erlanger, KY
   (606) 283-5000
2. KDS America, Inc.
   Fountain Valley, CA
   (714) 557-7833

Table 8-2b. Crystal Specifications - 333R34-002

Characteristic	Value
Rockwell Part No.	333R34-002
Electrical Specifications	
Frequency, F	35.251200 MHz nom. @ 25°C
Frequency Tolerance	±15 ppm @ 25°C
Frequency Stability	
vs. Temperature	±30 ppm (0°C to 70°C)
vs. Aging	±5 ppm/year
Oscillation Mode	3rd overtone
Calibration Mode	Parallel resonant
Load Capacitance, C_L	18 pF nom.
Frequency Variation	±35 ppm (C_L = 16.5 or 19.5 pF)
Shunt Capacitance, C_O	7 pF max.
Series Capacitance, C_1	0.0291 pF typ. @ F/3 0.0023 pF typ. @ F
Series Inductance, L_1	6.3 mH typ. @ F/3 9.1 mH typ. @ F
Series Resistance, R_1	150 Ω max. @ F/3 70 Ω max. @ F
Drive Level	1.0 mW max.,
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to 85°C
Mechanical Specifications	
Holder Type	HC-49/U
Third Lead	Required
Sleeving	N/A

Notes:

Suggested Suppliers:

1. Hy-Q International (USA), Inc.
   Erlanger, KY
   (606) 283-5000
2. KDS America, Inc.
   Fountain Valley, CA
   (714) 557-7833
3. Toyocom U.S.A., Inc.
   Costa Mesa, CA
   (714) 668-9081

Table 8-2c. Crystal Specifications - 333R34-003

Characteristic	Value
Rockwell Part No.	333R34-003
Electrical Specifications	
Frequency, F	35.251200 MHz nom. @ 25°C
Frequency Tolerance	±25 ppm @ 25°C
Frequency Stability	
vs. Temperature	±40 ppm (0°C to 70°C)
vs. Aging	±20 ppm/4 years
Oscillation Mode	3rd overtone
Calibration Mode	Parallel resonant
Load Capacitance, C_L	18 pF nom.
Frequency Variation	±15 ppm (C_L = 16.5 or 19.5 pF)
Shunt Capacitance, C_O	7 pF max.
Series Capacitance, C_1	0.0291 pF typ. @ F/3
	0.0023 pF typ. @ F
Series Inductance, L_1	6.3 mH typ. @ F/3
	9.1 mH typ. @ F
Series Resistance, R_1	150 Ω max. @ F/3
	70 Ω max. @ F
Drive Level	1.0 mW max.,
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to 85°C
Mechanical Specifications	
Holder Type	HC-49/U
Third Lead	N/A
Sleeving	N/A

Notes:

Suggested Suppliers:

1. Hy-Q International (USA), Inc.
   Erlanger, KY
   (606) 283-5000

Table 8-2d. Crystal Specifications - R333R02-004

Characteristic	Value
Rockwell Part No.	R3333R02-004
Electrical Specifications	
Frequency, F	35.251200 MHz nom.
Frequency Tolerance	±50 ppm (C_L = 16.5 or 19.5 pF)
Frequency Stability	
vs. Temperature	±35 ppm (0°C to 70°C)
vs. Aging	±15 ppm/4 years
Oscillation Mode	Fundamental
Calibration Mode	Parallel resonant
Load Capacitance, C_L	18 pF nom.
Shunt Capacitance, C_O	7 pF max.
Series Resistance, R_1	80 Ω max. @20 nW Drive Level
Drive Level	100 μW correlation; 300 μW max.
Operating Temperature	0°C to 70°C
Storage Temperature	–30°C to 80°C
For Modeling Only	
Series Inductance, L_1	23.3 mH
Series Capacitance, C_1	0.0009 pF
Shunt Capacitance, C_O	2.8 pF
Mechanical Specifications	
Holder Type (L x W x H)	SMT 7.5 x 5.1 x 1.3 mm

Notes:

Electrical specifications at 25°C unless otherwise noted.

Suggested Suppliers:

1. KDS America, Inc.
   Fountain Valley, CA
   (714) 557-7833

Table 8-2e. Crystal Specifications - R3333R03-006

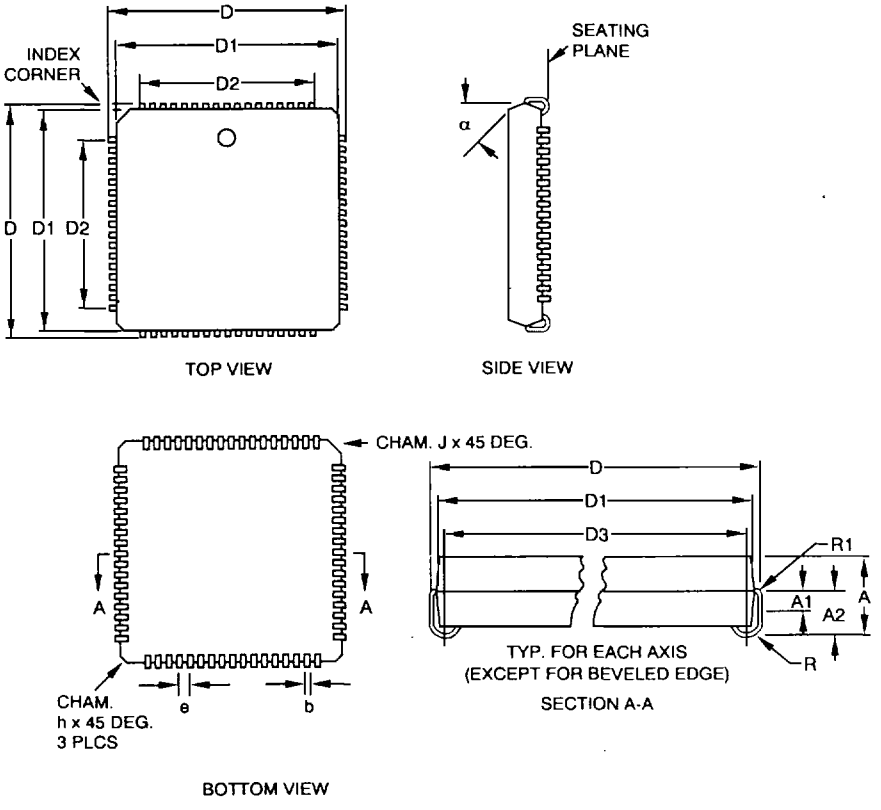
Characteristic	Value
Rockwell Part No.	R3333R03-006
Electrical Specifications	
Frequency, F	35.251200 MHz nom.
Frequency Tolerance	±50 ppm (C_L = 16.5 or 19.5 pF)
Frequency Stability	
vs. Temperature	±35 ppm (0°C to 70°C)
vs. Aging	±15 ppm/4 years
Oscillation Mode	3rd Overtone
Calibration Mode	Parallel resonant
Load Capacitance, C_L	18 pF nom.
Shunt Capacitance, C_O	7 pF max.
Series Resistance, R_1	60 Ω max. @20 nW Drive Level
Drive Level	100 μW correlation; 300 μW max.
Operating Temperature	0°C to 70°C
Storage Temperature	–30°C to 80°C
For Modeling Only	
Series Inductance, L_1	19.0 mH
Series Capacitance, C_1	0.0011 pF
Shunt Capacitance, C_O	3.4 pF
Mechanical Specifications	
Holder Type (L x W x H)	SMT 12 x 5.7 x 2.5 mm

Notes:

Electrical specifications at 25°C unless otherwise noted.

Suggested Suppliers:

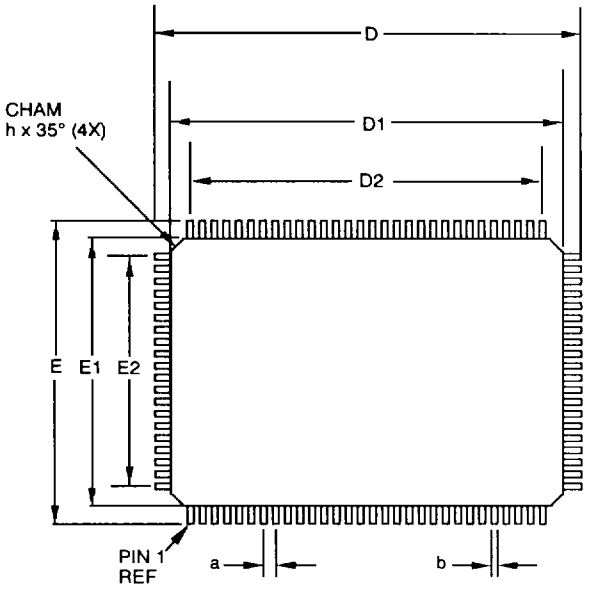
1. KDS America, Inc.
   Fountain Valley, CA
   (714) 557-7833



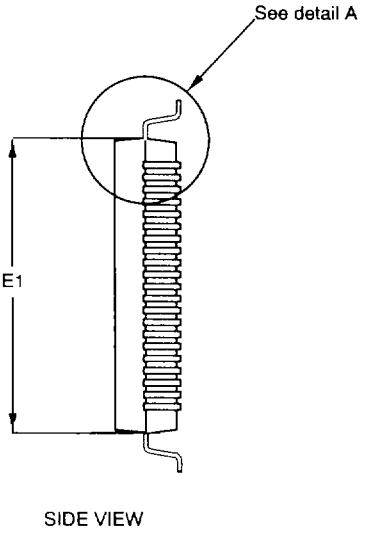
Dim.	Millimeters Min.	Millimeters Max.	Inches Min.	Inches Max.
A	4.14	4.39	0.163	0.173
A1	1.37	1.47	0.054	0.058
A2	2.31	2.46	0.091	0.097
b	0.457 TYP		0.018 TYP	
D	25.02	25.27	0.985	0.995
D1	24.00	24.26	0.945	0.955
D2	20.19	20.45	0.795	0.805
D3	23.24	23.50	0.915	0.925
e	1.27 BSC		0.050 BSC	
h	0.254 TYP		0.010 TYP	
J	1.15 TYP		0.045 TYP	
α	45° TYP		45° TYP	
R	0.89 TYP		0.035 TYP	
R1	0.254 TYP		0.010 TYP	
Ref: PD68J/GP00-D164				

91710:2

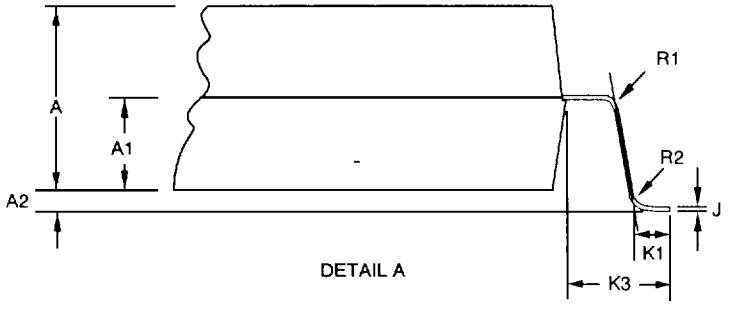
Figure 8-1a. 68-Pin PLCC Dimensions



TOP VIEW



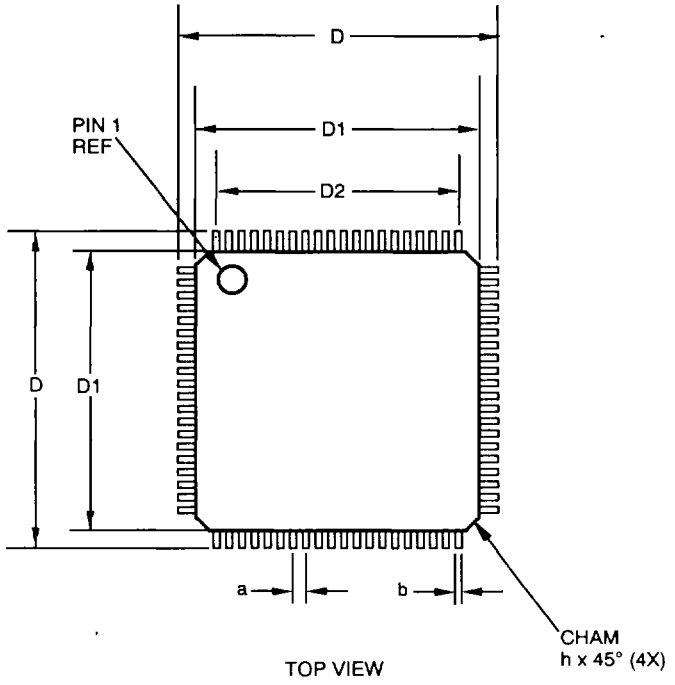
SIDE VIEW



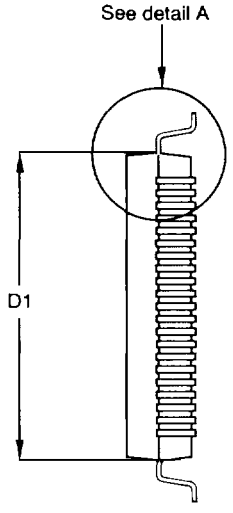
DETAIL A

Dim.	Millimeters Min.	Max.	Inches Min.	Max.
A	1.95	2.05	0.077	0.081
A1	0.95	1.05	0.037	0.041
A2	0.25 REF		0.010 REF	
D	23.05	23.35	0.907	0.919
D1	19.95	20.05	0.785	0.789
D2	18.85 REF		0.742 REF	
E	17.05	17.35	0.671	0.683
E1	13.95	14.05	0.549	0.553
E2	12.35 REF		0.486 REF	
K1	0.70	0.90	0.028	0.035
K3	1.60 REF		0.063 REF	
R1	0.13	---	0.005	---
R2	0.15	0.25	0.006	0.010
a	0.65 REF		0.026 REF	
b	0.30 REF		0.012 REF	
h	--	0.50	--	0.020
J	0.1524 REF		0.006 REF	
Ref: GP00-D234-5/92				

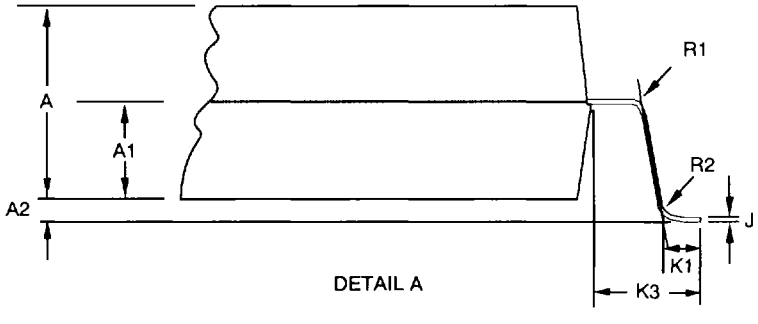
Figure 8-1b. 100-Pin PQFP Dimensions



TOP VIEW



SIDE VIEW



DETAIL A

Dim.	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.95	2.05	0.077	0.081
A1	0.95	1.05	0.037	0.041
A2	0.15	0.25	0.006	0.010
D	17.05	17.35	0.671	0.683
D1	13.95	14.05	0.549	0.553
D2	12.35 REF		0.486 REF	
K1	0.70	0.90	0.028	0.035
K3	1.60 REF		0.063 REF	
R1	0.13	---	0.005	---
R2	0.15	0.25	0.006	0.010
a	0.65 REF		0.026 REF	
b	0.26	0.36	0.010	0.014
h	---	0.25	---	0.010
J	0.13	0.17	0.005	0.007
Ref: GP00-D227				

Figure 8-1c. 80-Pin PQFP Dimensions

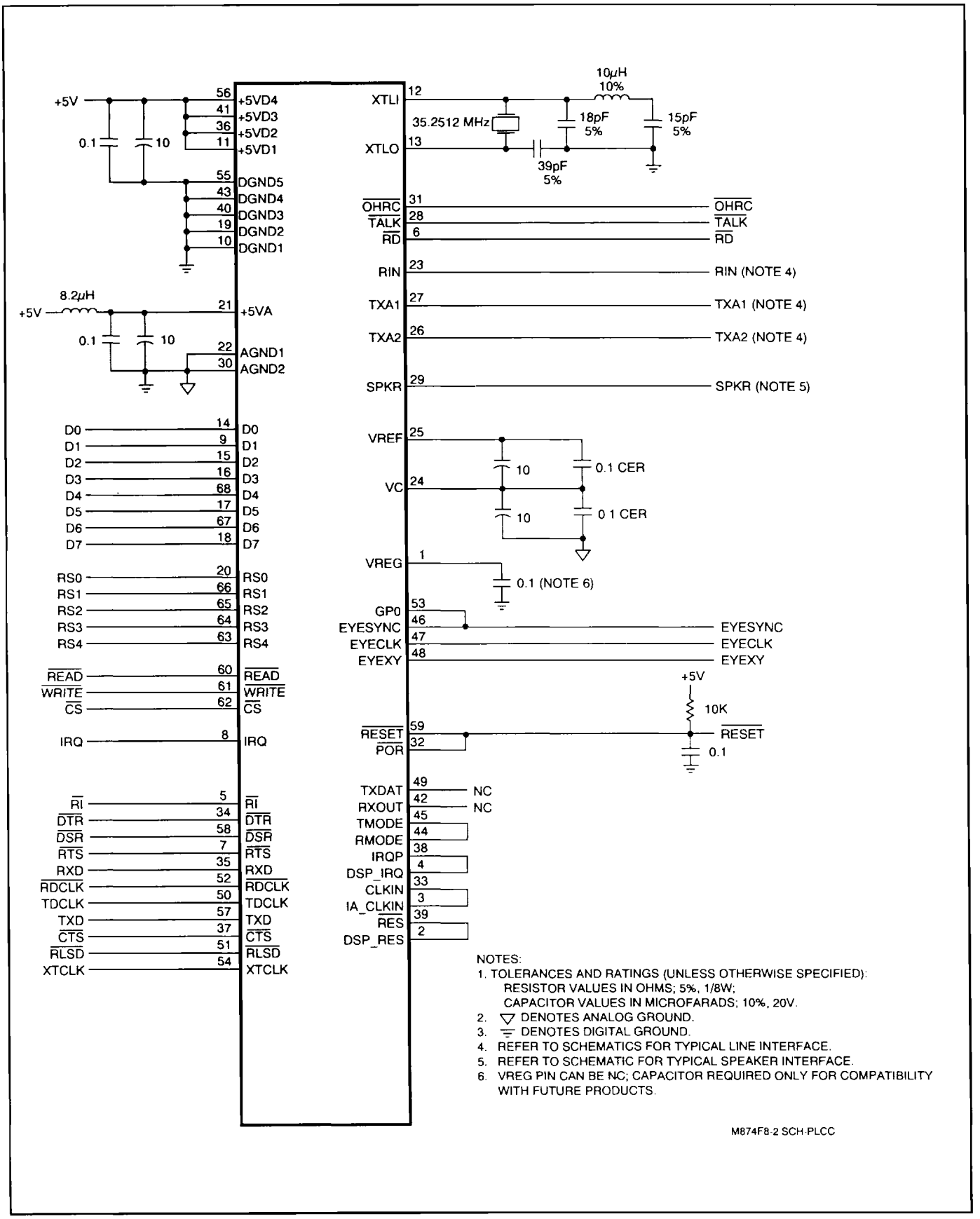


Figure 8-2. Typical Interface to Modem in PLCC

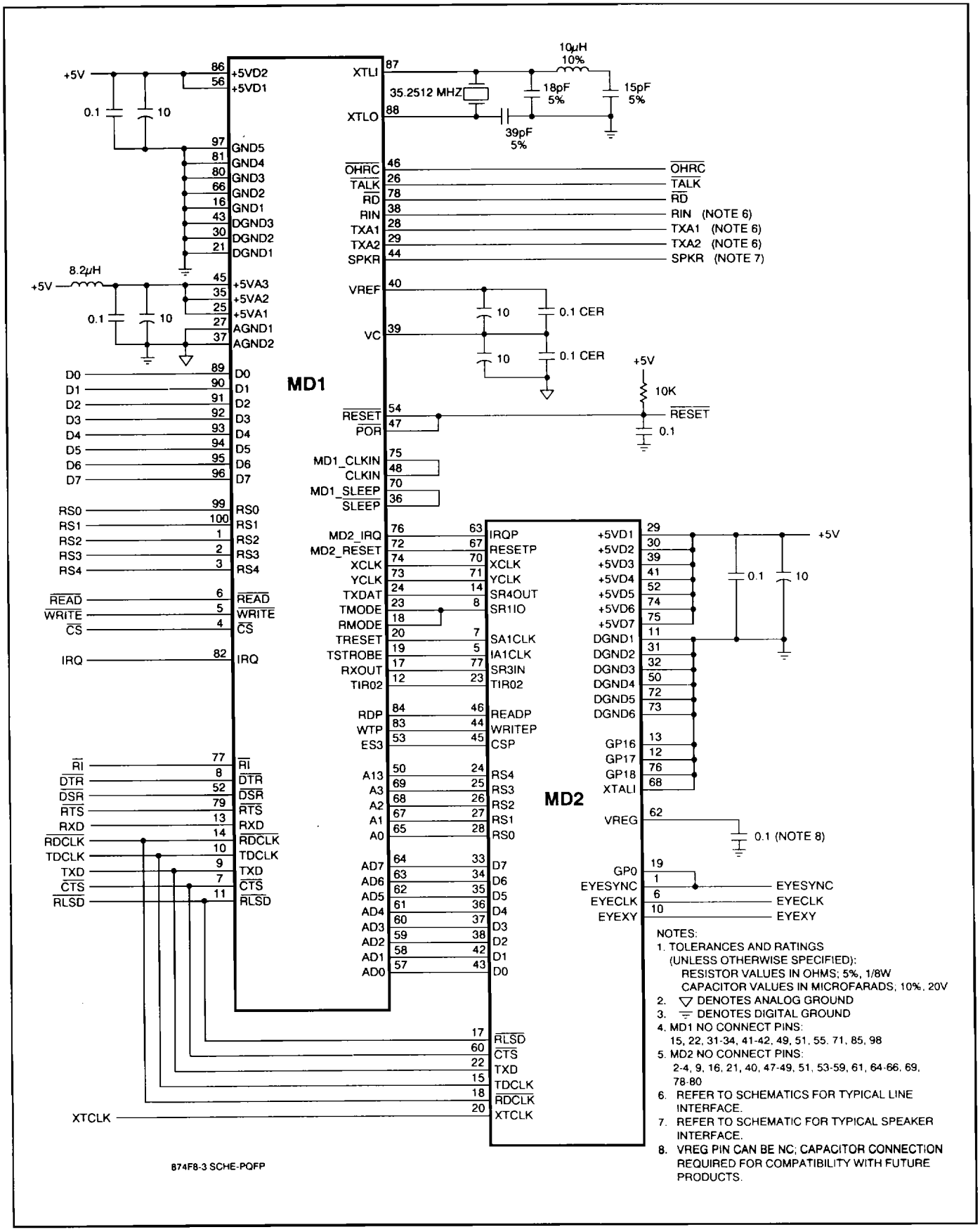


Figure 8-3. Typical Interface to Modem in PQFP

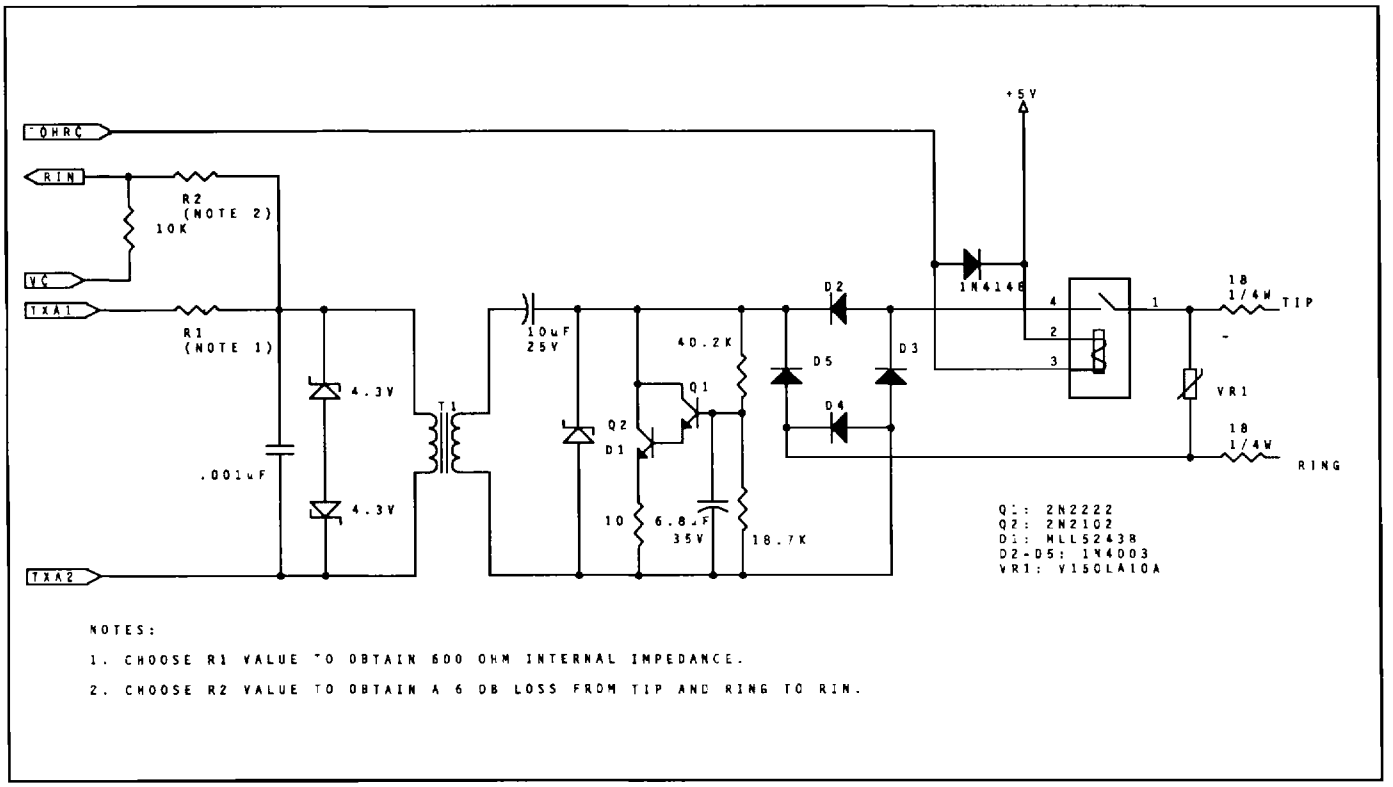


Figure 8-4. Typical Line Interface

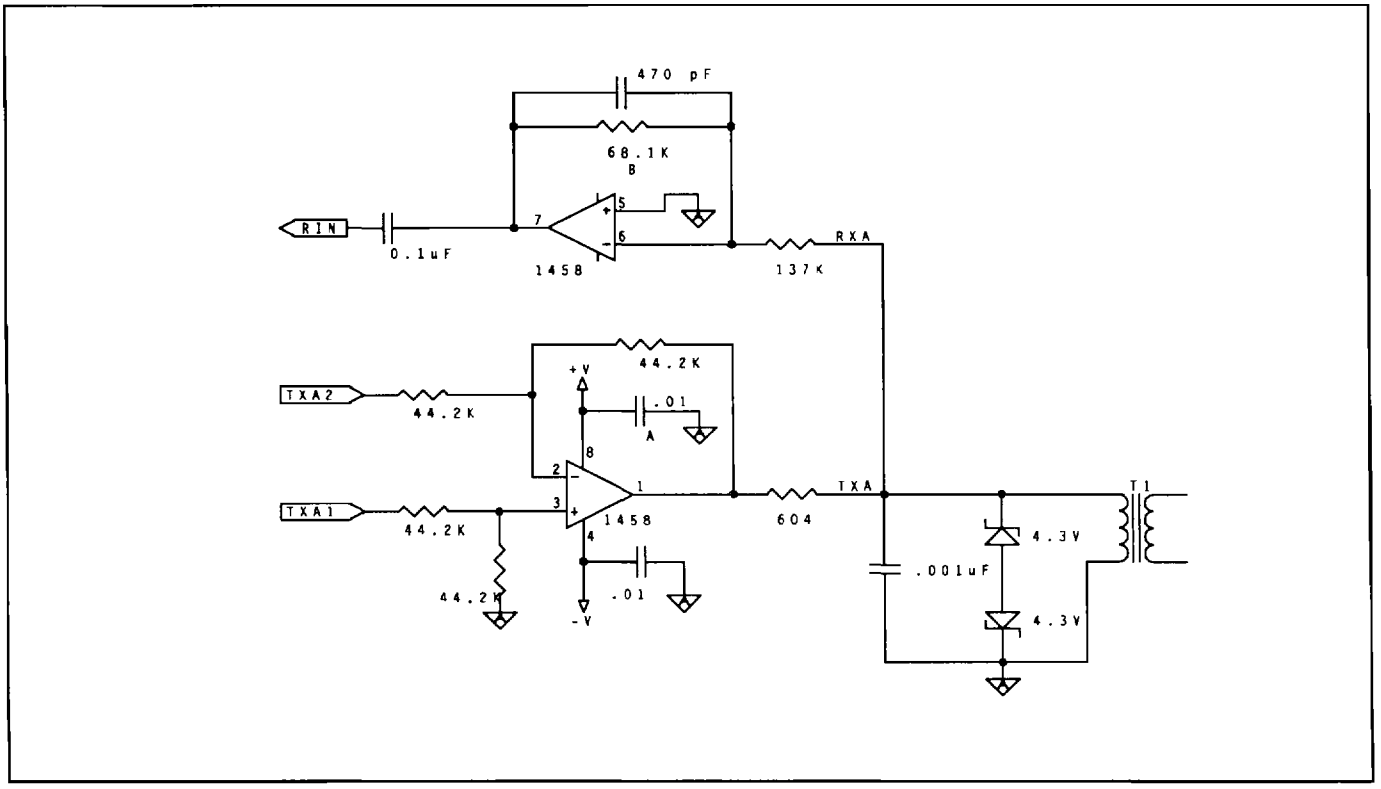


Figure 8-5. Typical Interface to External Hybrid

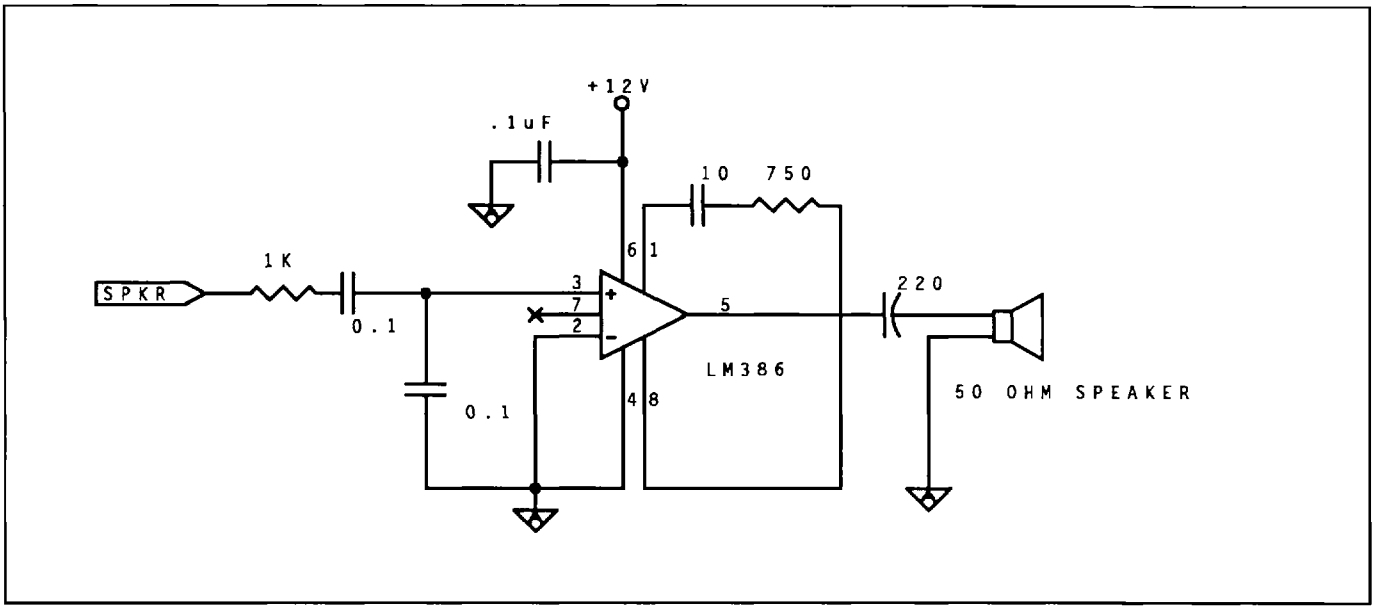


Figure 8-6. Typical External Speaker Circuit

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9 T.30 IMPLEMENTATION

9.1 GENERAL

CCITT Recommendation T.30 details procedures for facsimile transmission over the PSTN. This standard describes how to initiate, complete, and end a fax transmission. This section describes methods to set up host software to implement T.30 with the modem.

A basic block diagram of a Group 3 facsimile machine is shown in Figure 9-1. The modem performs the modulation/demodulation process. The fax machine manufacturer must implement the interface between the modem (T.30), the data compression/decompression (T.4), and the interface to the scanner and printer.

There are five phases (A-E) to the T.30 facsimile protocol. Phase A is the call setup, in which both facsimile machines connect to the line. Phase B is a pre-message procedure which consists of identification and command sections. The actual high speed message transmission occurs during Phase C. This is followed by the post-message procedure or Phase D. Both facsimile machines release the line in Phase E.

Figure 9-2 illustrates a typical Group 3 facsimile procedure. This example on T.30 describes a facsimile call where the calling unit (originate) transmits a documents to a called unit (answer). Phase E is not included in this example since it is the call release and both ends hang up.

Figures 9-3 through 9-7 illustrate how to originate a fax call. Figures 9-8 through 9-13 illustrate how to answer a fax call. Figures 9-14 through 9-19 illustrate subroutines for originating or answering a fax call.

9.1.1 Phase A

T.30 specifies that call establishment can be realized one of four ways. The four methods of call establishment are: manual-to-manual, manual-to-automatic, automatic-to-manual, and automatic-to-automatic. Manual corresponds to operator or human intervention while automatic means machine only. The explanation that follows describes an automatic-to-automatic example.

After dialing, the calling unit, or originating fax, first transmits a calling tone (CNG) to indicate it is a non-speech terminal. The called unit, or answering fax, then responds with a called station ID (CED). The end of Phase A is signified after the called unit sends a 2100 Hz (CED) tone and the calling unit has detected this tone. Some facsimile manufacturers do not configure the modem to detect these tones. In this case, the modem looks for the preamble of flags (see phase B).

9.1.2 Phase B

The pre-message procedure consists of the following handshake. The answering fax machine sends an identification signal and the originating machine responds with a command signal. A training check is sent at a high speed and the receiving machine informs the transmitting machine if the training check was successful. This usually occurs at V.21 300 bps Frequency Shift Keying (FSK) modulation in HDLC format.

HDLC stands for High level Data Link Control. It is a standard procedure used for data communications. HDLC is a bit-oriented protocol (normally used in synchronous communications) that defines how the data being sent over the data link is organized and arranged.

When using the HDLC protocol, the data is transmitted via frames. These frames organize the data into a format specified by an ISO (International Standards Organization) standard that enables the transmitting and receiving station to synchronize with each other. Figure 9-20 illustrates the HDLC frame structure used for the facsimile protocol.

The preamble is a series of HDLC Flags for one second ±15%. The purpose of the 7E flags is to condition the line. The flag sequence defines the beginning and ending of a frame. The address field is required to provide identification for multi-point addressing. For PSTN the format is 11111111. The control field's purpose is to provide the capability of encoding the commands and responses. The format is 1100X000 (X=0 non-final frame; X=1 final frame).

The HDLC information field provides the specific information for the control and message interchange between the two stations. In the fax protocol the format for the information field consists of two parts, the Facsimile Control Field (FCF) and the Facsimile Information Field (FIF).

The FCF contains information regarding the type of information being exchanged and the position in the overall sequence. The acronyms, functions, and format for FCF commands are defined in the T.30 Recommendation. The FIF contains additional information which further clarifies the facsimile procedure. Some examples of information communicated with the FIF are: group capability, data rate, vertical resolution, coding scheme, recording width, recording length, and minimum scan line time.

The Frame Check Sequence (FCS) follows the FIF. The modem automatically generate the FCS or Cyclic Redundancy Check (CRC). The frame ends with an ending 7E flag. It is recommended that more than one ending flag be transmitted.

After the modem has been configured for FSK, the Digital Identification Signal (DIS) is transmitted by the called unit. The DIS informs the calling unit about the called unit's capabilities such as group capability (G1, G2, G3), data rate, vertical resolution, coding scheme (Modified Huffman, Modified Read), recording width, recording length, and minimum scan line time. The calling unit then responds with a Digital Command Signal (DCS) which in-

forms the called unit which options are chosen to complete this facsimile call.

After the DCS is transmitted, both the calling unit and the called unit set up for the high speed configuration that was chosen and transmitted via the DCS. A Training Check (TCF) is transmitted by the calling unit to verify training and give an indication of channel acceptability for the selected data rate. The TCF consists of a series of zeros for 1.5 seconds ±10%. Since the called unit knows it will be receiving 1.5 seconds of zeros, the host can make a decision whether the line is good enough at the chosen data rate or fallback to a slower speed.

After completing the TCF, the calling unit and the called unit re-configure for FSK, HDLC format. The called unit then transmits either a Confirmation to Receive (CFR) or a Failure To Train (FTT). The CFR is a response informing the calling unit of a successful pre-message procedure completion. A FTT informs the calling unit that the training signal was rejected and requests re-training. If a FTT is received by the calling unit, the fax protocol jumps back to the transition of DCS and continues until finally a CFR is received or the calling unit host decides to terminate the call.

9.1.3 Phase C

Phase C occurs after both facsimile machines have set up for the high speed configuration that was decided upon in phase B. The T.30 Error Correction Mode is addressed in a following section. The high speed message information is usually compressed data using a Modified Huffman (MH) or Modified Read (MR) algorithm. The host processor must perform the MH or MR compression before loading the data into the modem. On the receive end, the host processor must perform the MH or MR decompression.

The start of phase C is denoted by an End Of Line (EOL) 8-bit code. The data follows this first EOL character until the end of the line. Another EOL character is transmitted to indicate a new line. A minimum transmission time of a total coded scan line is measured from the beginning of the EOL to the beginning of the following EOL. If the transmitted data requires less time than the minimum transmission time, fill bits must be transmitted. Six consecutive EOL character constitute a Return To Control (RTC) command meaning end of document transmission. Figure 9-21 illustrates the phase C format.

9.1.4 Phase D

The post-message phase D procedure uses FSK and HDLC format. The calling station will typically send an End Of Message (EOM) signal. This FCF command (EOM) informs the called station that this is the end of the page and return to Phase B. A Multi-Page Signaling (MPS) or End Of Procedure (EOP) signal may be sent instead of EOM. The MPS signal informs the called unit that there are more pages in this facsimile transmission. EOP signals the end of the facsimile transmission. Procedure Interrupt-EOM (PRI-EOM), Procedure Interrupt-MPS (PRI-MPS), and Procedure Interrupt-EOP (PRI-EOP) indicate the same as EOM, MPS, and EOP, respectively, with the additional optional capability of requesting operator intervention. If operator intervention is required, further facsimile procedures commence at the beginning of phase B.

The called station might respond to an EOM, MPS, or EOP signal with a Message Confirmation (MCF) command. This FCF command indicates to the calling unit that the complete message was received. One of the following FCF commands may be sent instead of the MCF: Re-Train Positive (RTP), Re-Train Negative (RTN), Procedure Interrupt Positive (PIP), or Procedure Interrupt Negative (PIN). RTP indicates that a complete message has been received and that additional messages may follow after retransmission of TCF and CFR. RTN indicates that the previous message has not been satisfactorily received, however, further receptions may be possible provided there is a retransmission of TCF and CFR. PIP and PIN indicate that the previous message was received satisfactorily or not satisfactorily, respectively, and operator intervention is required for further transmissions.

9.1.5 Phase E

Call Release, or phase E, occurs after the last post-message signal of the procedure or under certain conditions such as a time-out, procedural interrupt, or a Disconnect (DCN) command.

The DCN command indicates the initiation of phase E. This command requires no response.

9.2 T.30 ERROR CORRECTION MODE

9.2.1 General

The revised T.30 contains an Error Correction Mode (ECM) option. The ECM allows the phase C portion of the facsimile transmission to be encoded in a HDLC framing format using a specified number of bits in the information field. The transmitted high speed message is broken up into a number of frames identified by frame numbers. If an error is detected during reception of the message, the called station records the frame number. After all the frames in the message has been received, the called station transmits the frame numbers that were received in error. The calling station then re-transmits only those frames in error. This continues until the entire message is received error free or the calling station decides not to transmit any more frames.

The error detection is performed by comparing the CRC or FCS. Using ECM, the data rate can be as fast as 14400 bps, therefore, the host microprocessor may not be able to keep up if implementing HDLC without the use of a serial I/O device. The modem provides HDLC features at speeds up to 9600 bps.

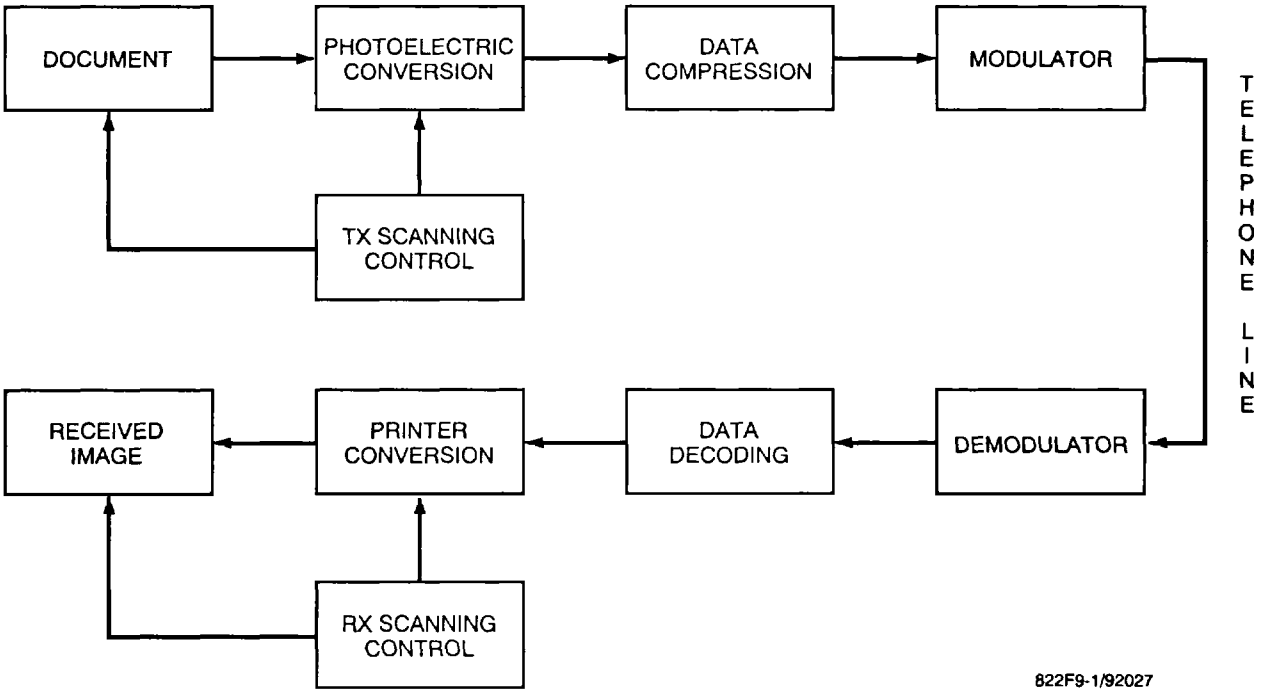


Figure 9-1. Basic Block Diagram of G3 Facsimile

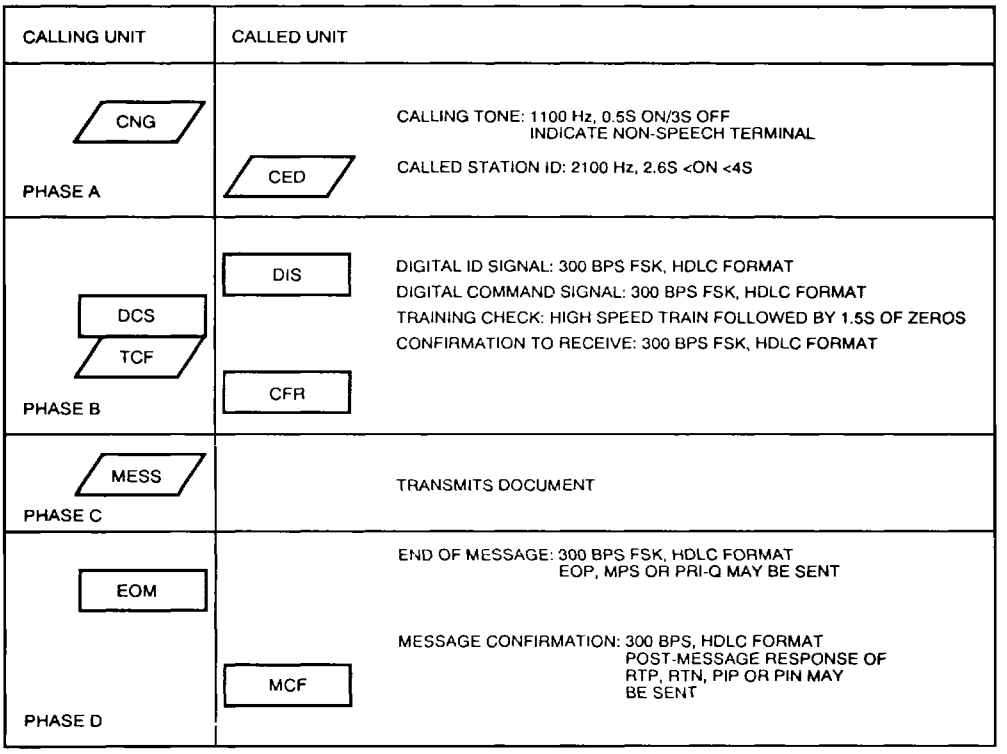


Figure 9-2. G3 Facsimile Procedure

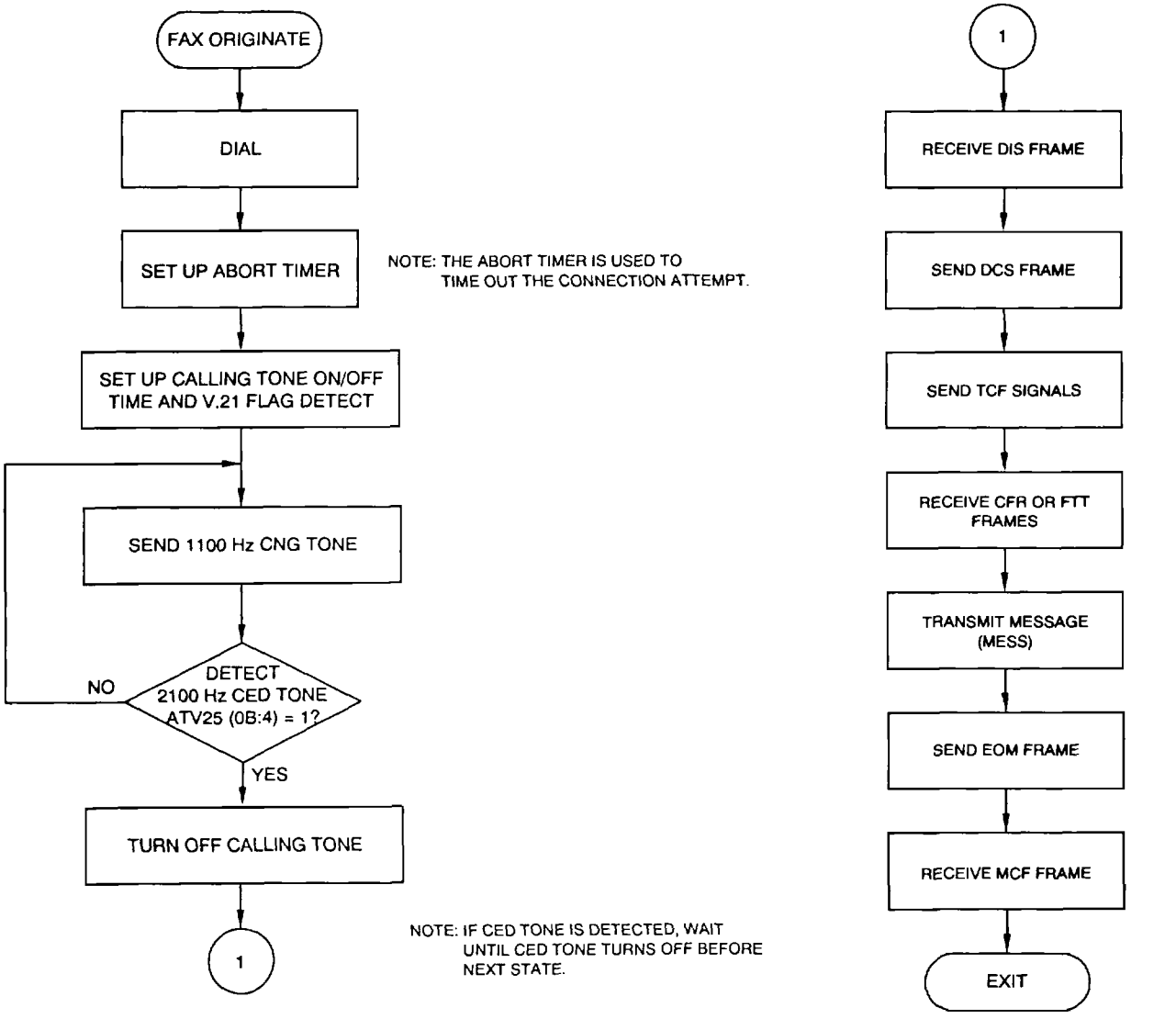


Figure 9-3. Originating a Fax Call - General

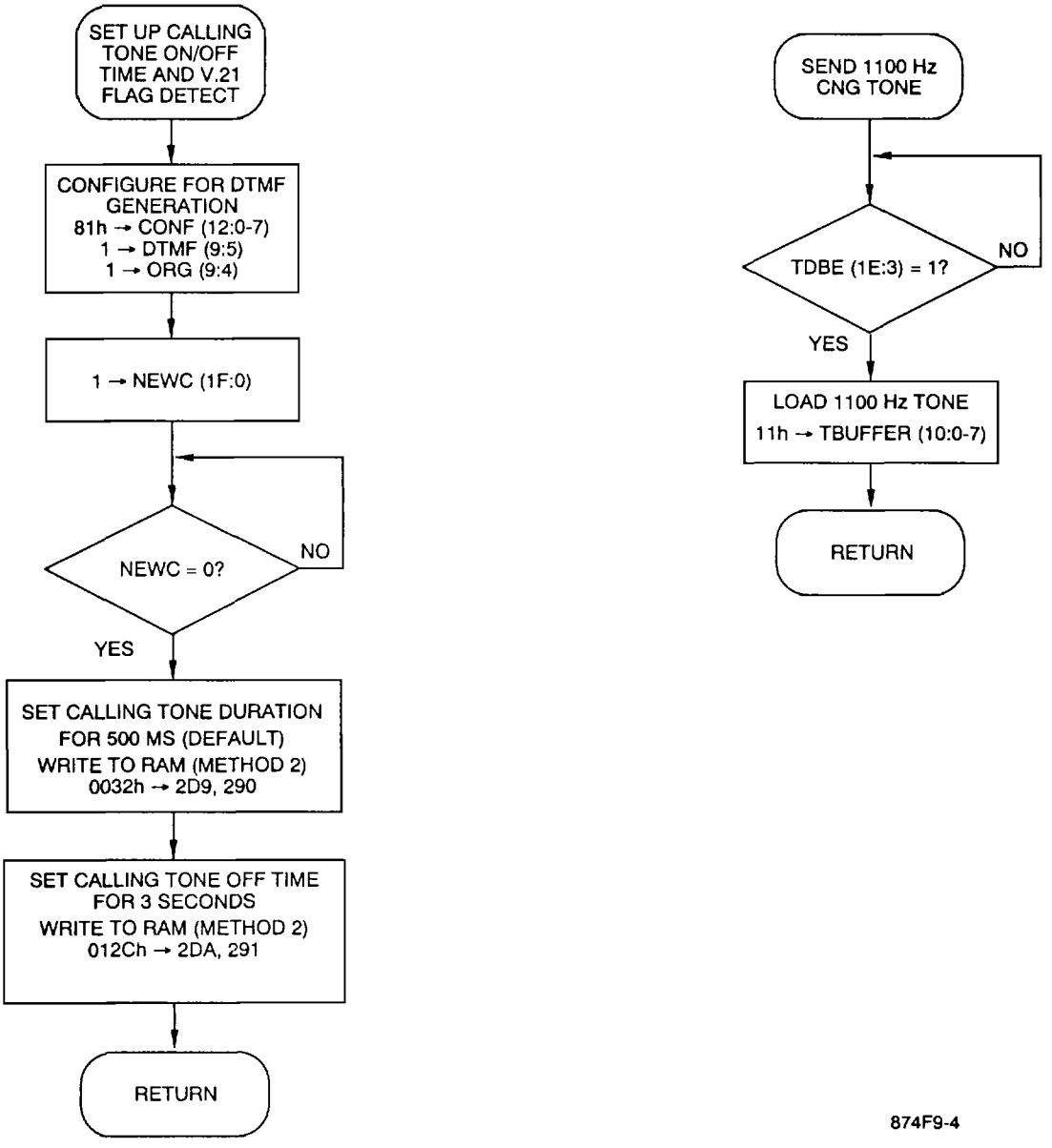


Figure 9-4. Originating a Fax Call - Phase A

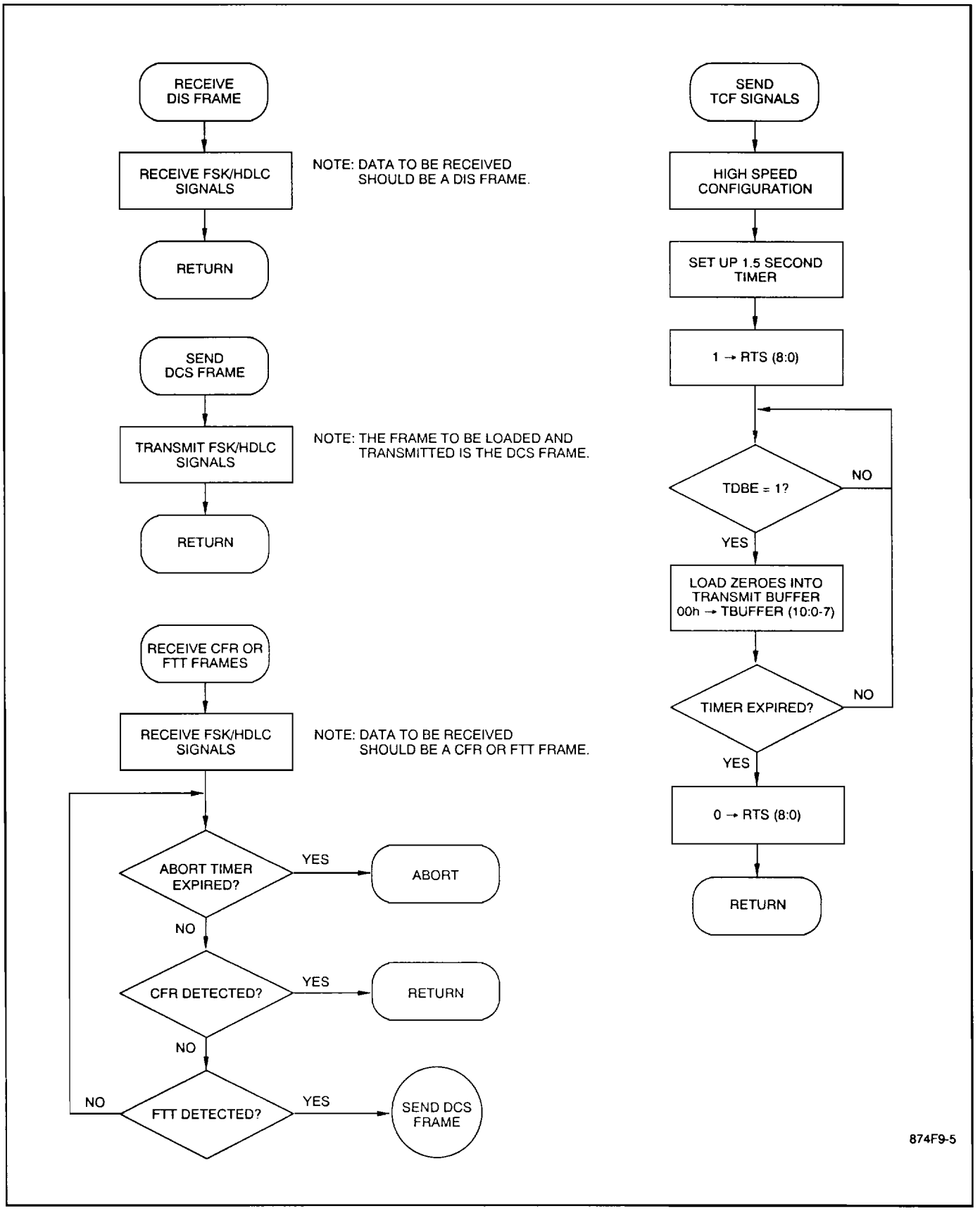


Figure 9-5. Originating a Fax Call - Phase B

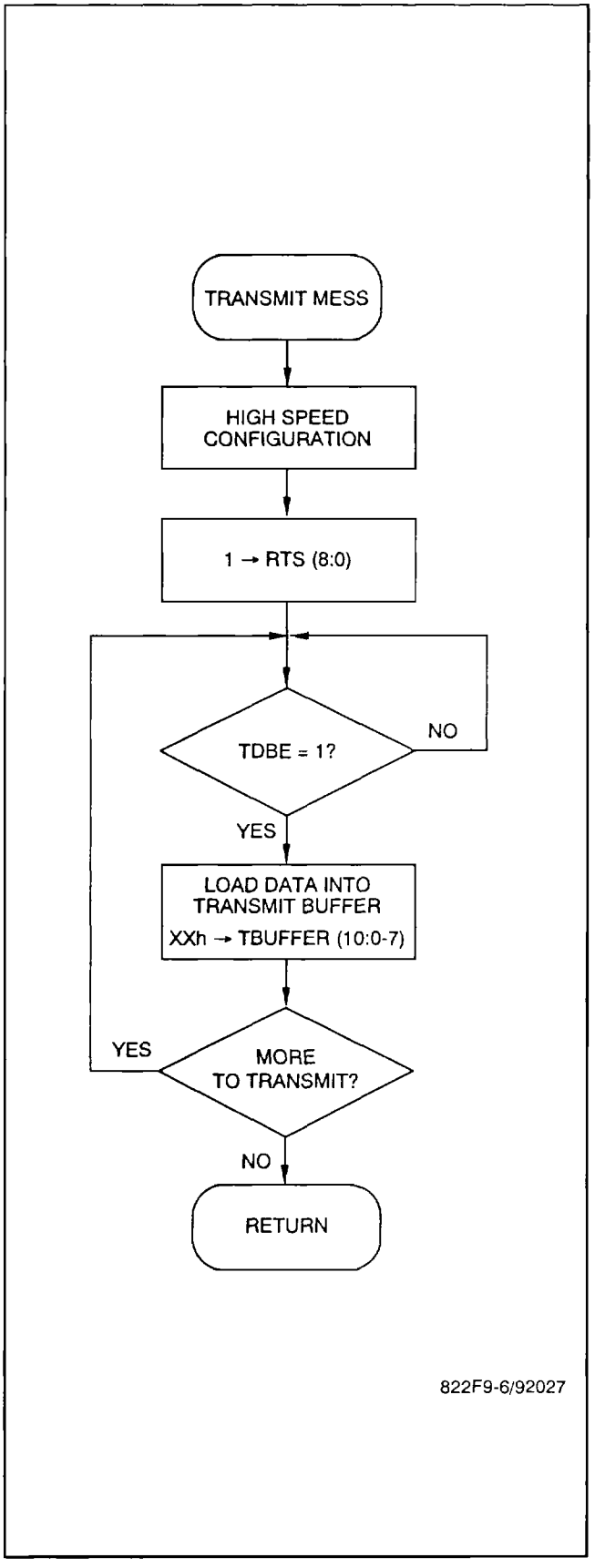


Figure 9-6. Originating a Fax Call - Phase C

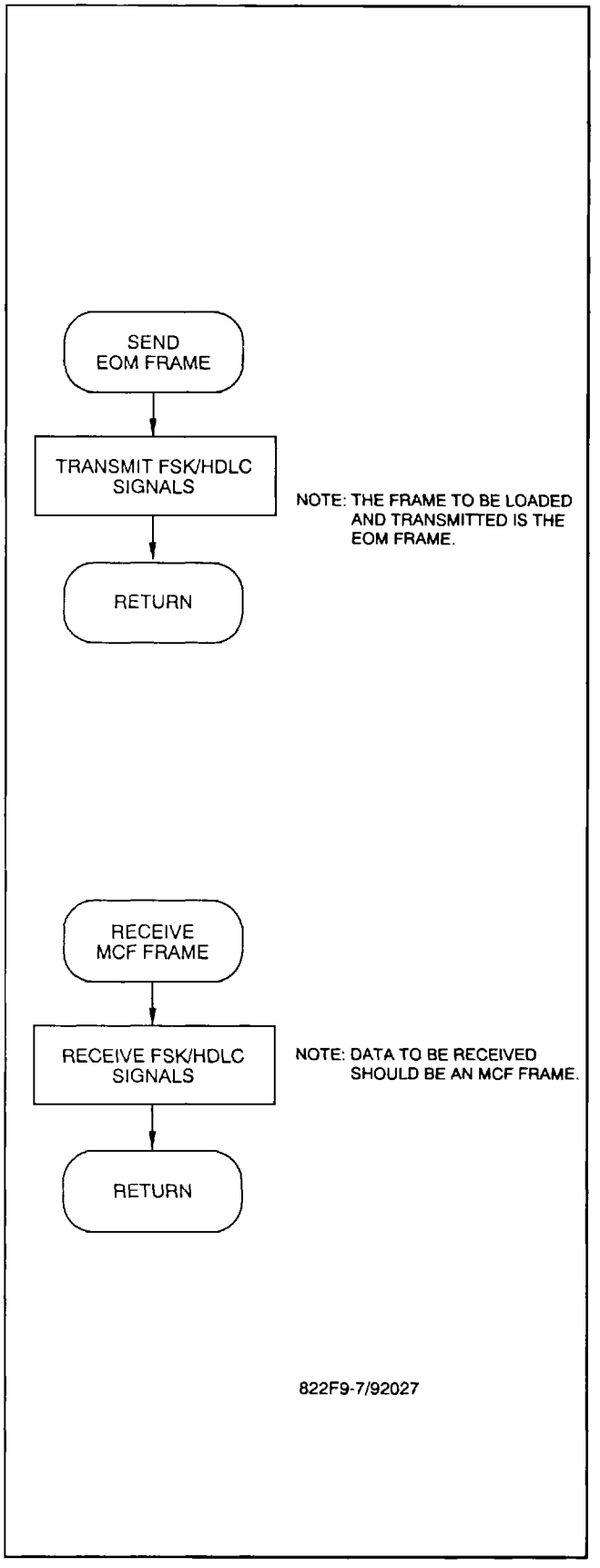


Figure 9-7. Originating a Fax Call - Phase D

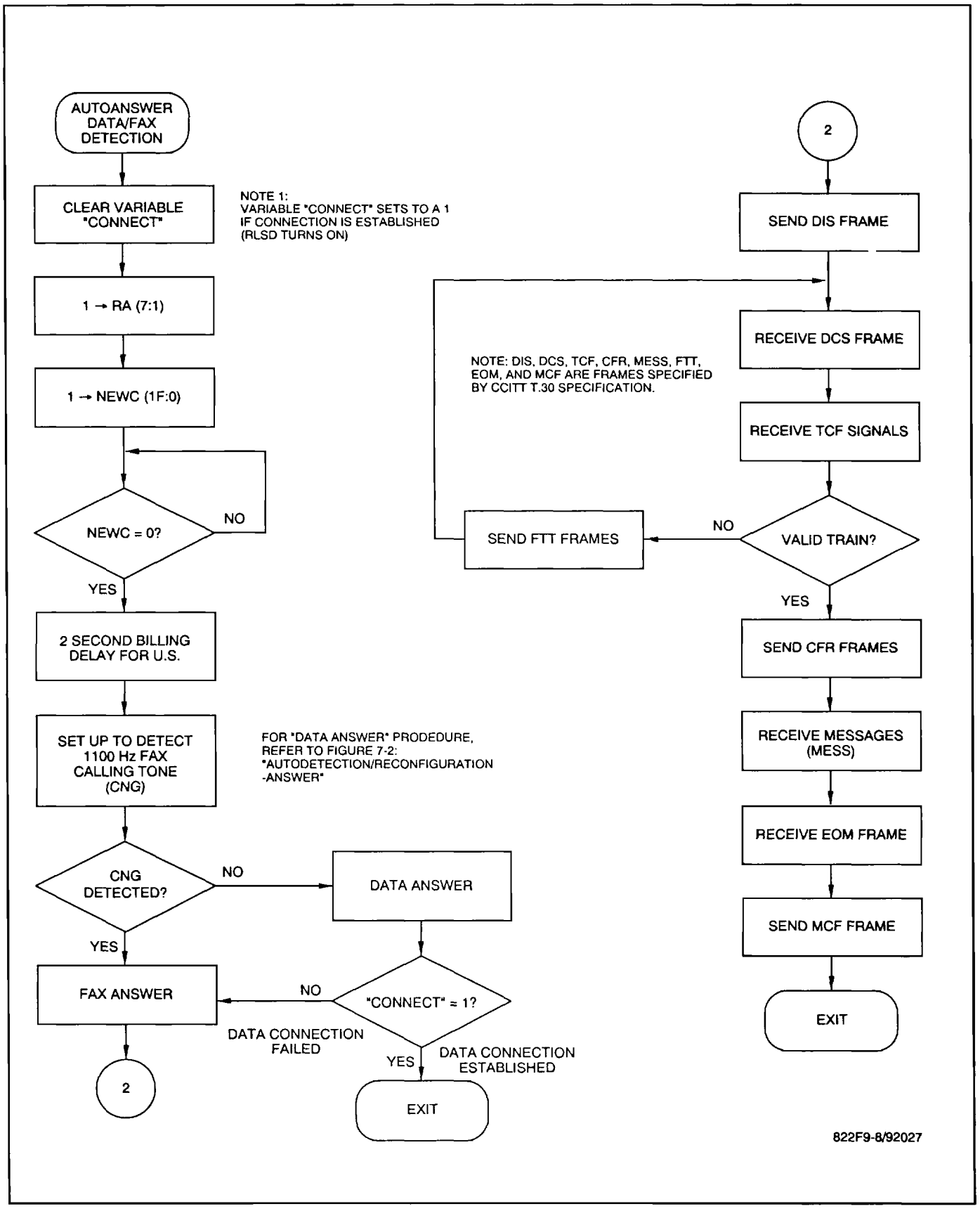


Figure 9-8. Answering a Fax Call - General

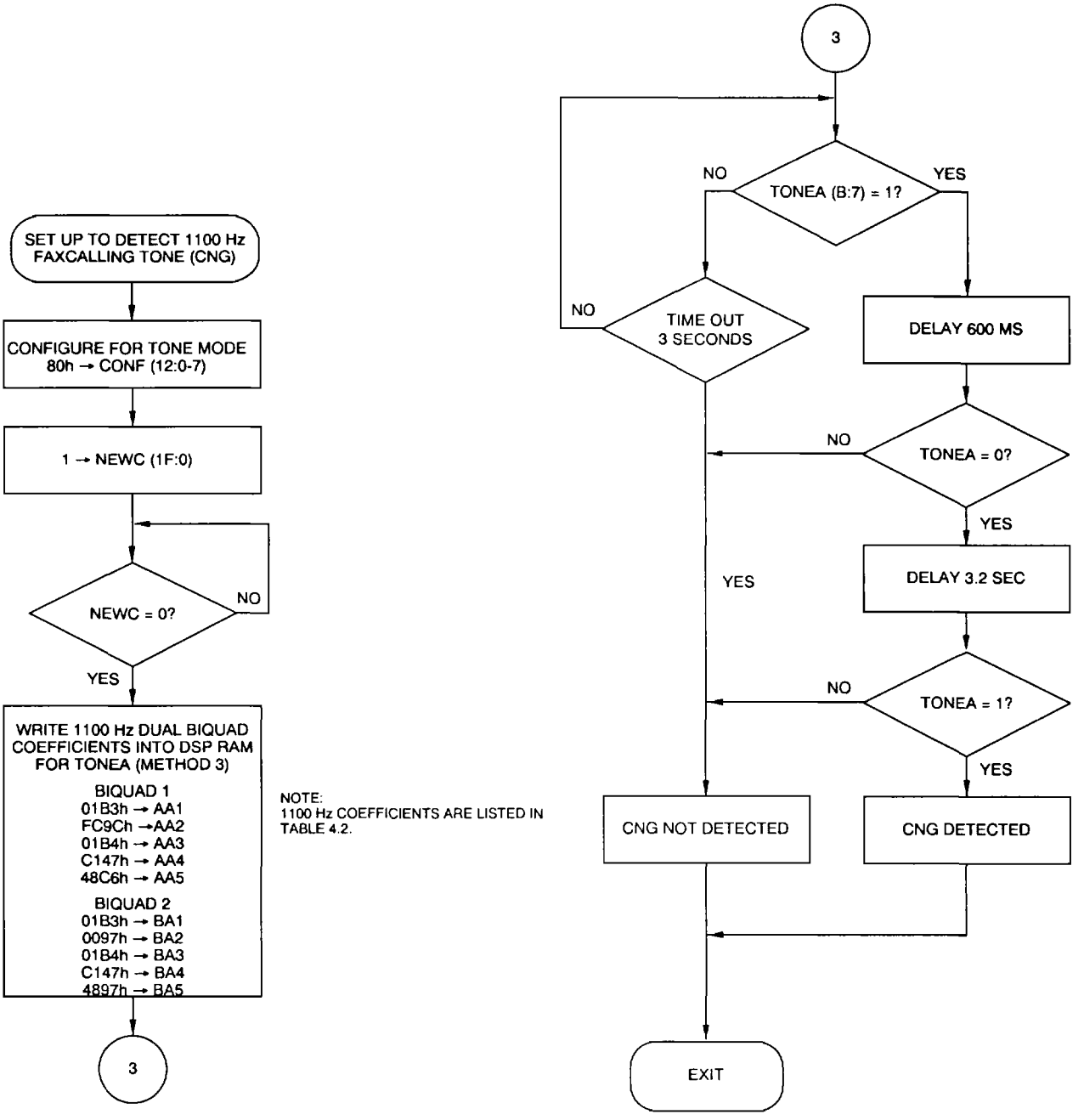


Figure 9-9. Answering a Fax Call - Phase A (CNG)

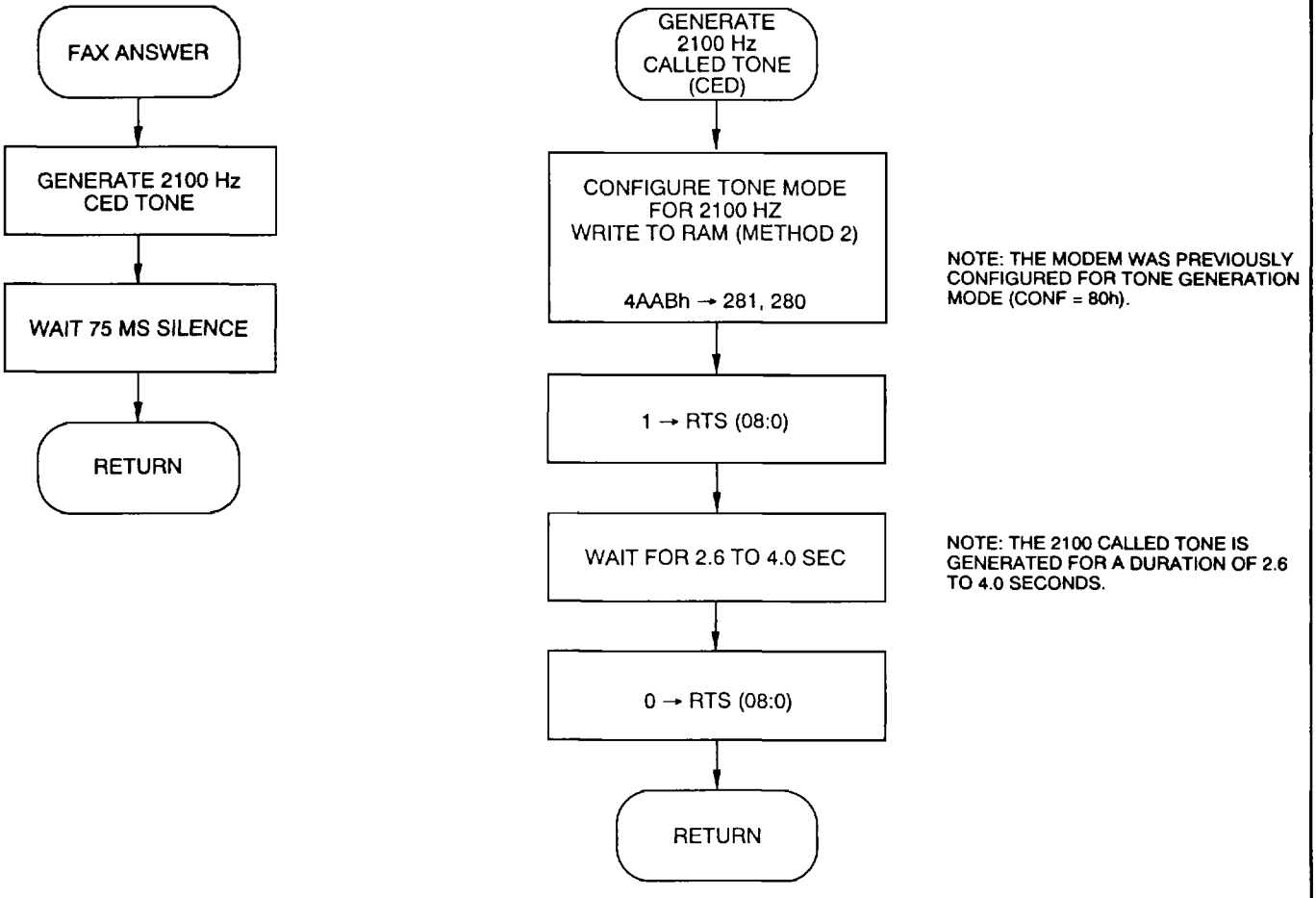


Figure 9-10. Answering a Fax Call - Phase A (CED)

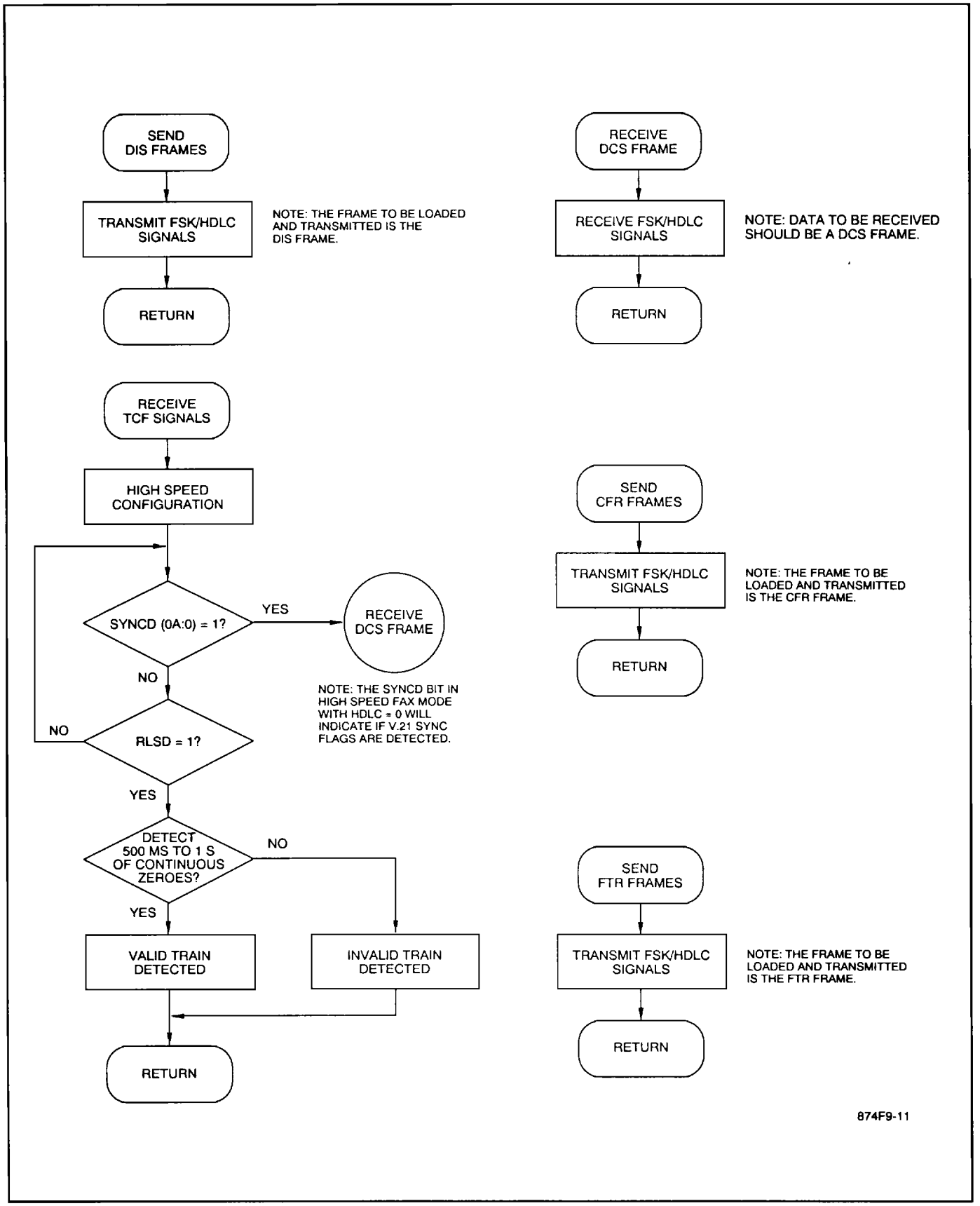


Figure 9-11. Answering a Fax Call - Phase B

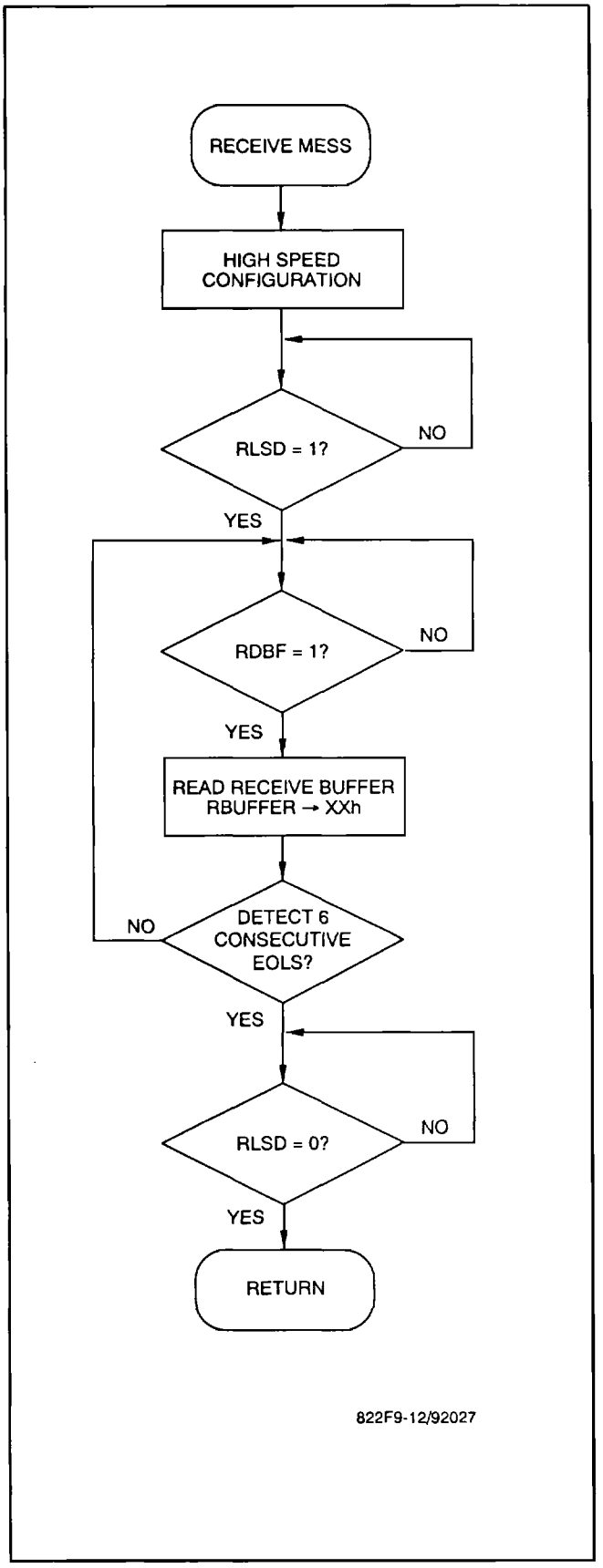


Figure 9-12. Answering a Fax Call - Phase C

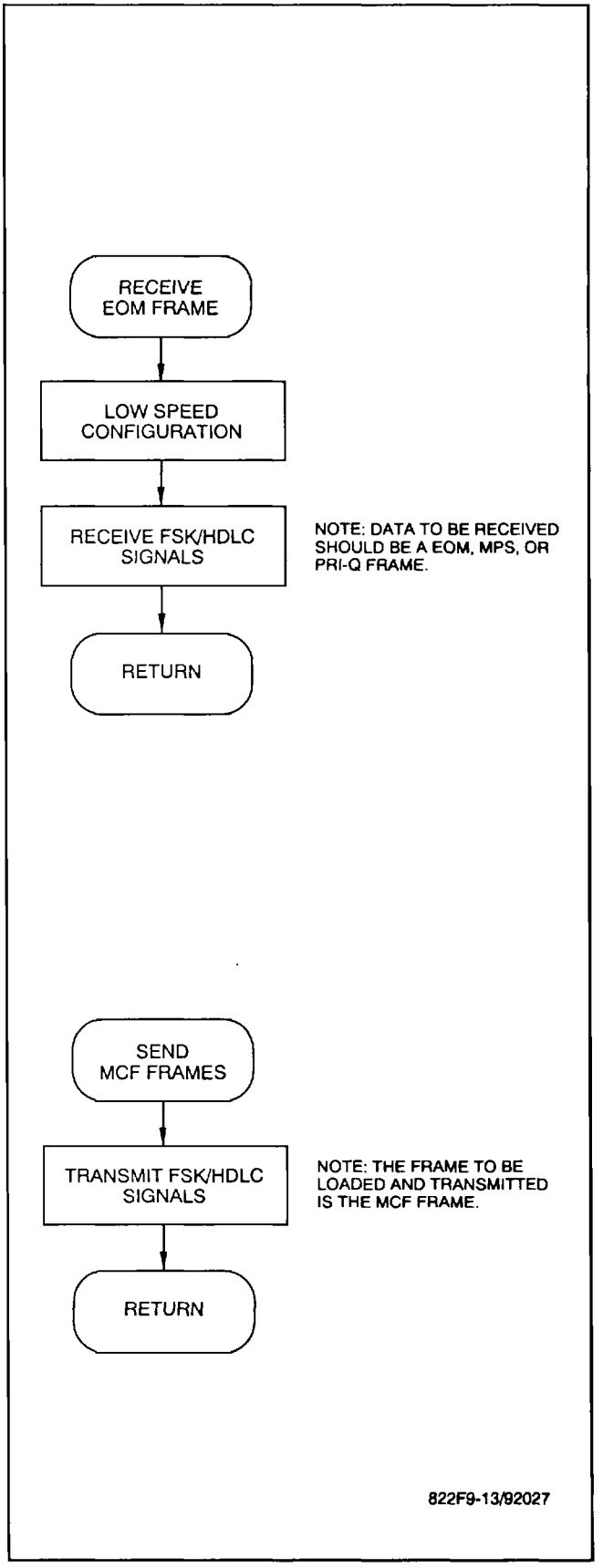


Figure 9-13. Answering a Fax Call - Phase D

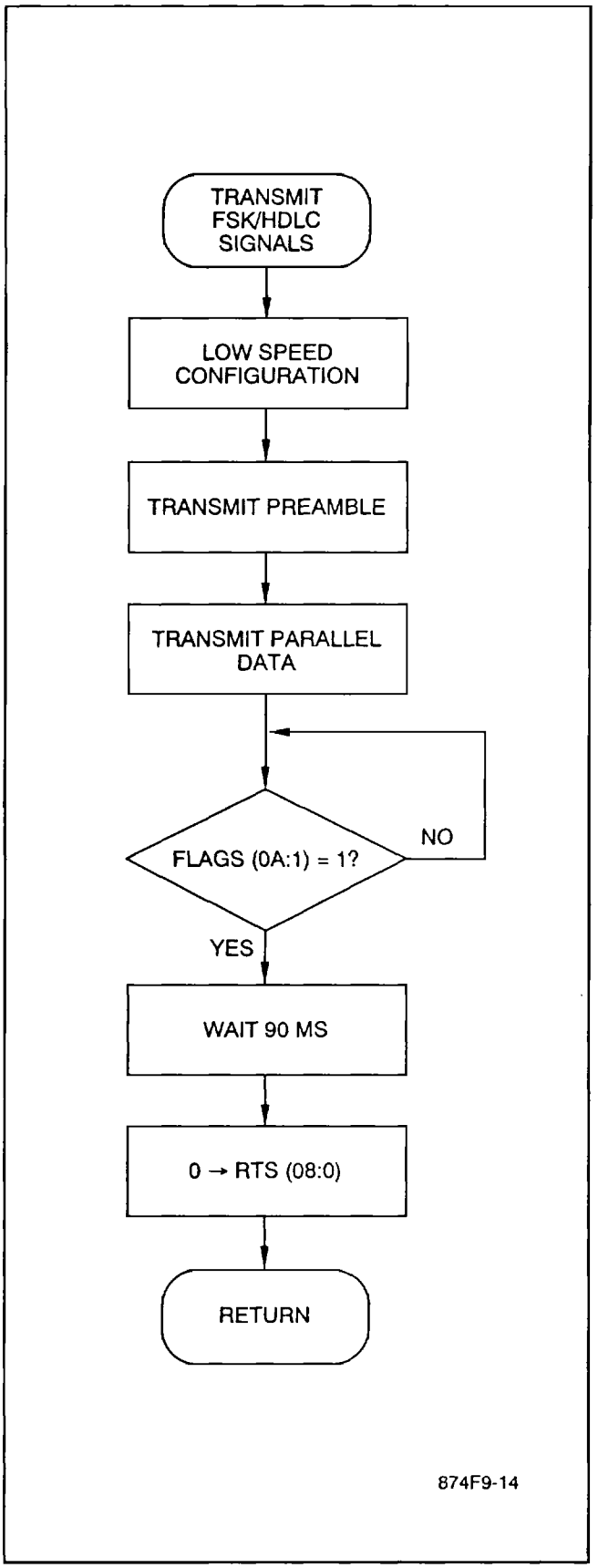


Figure 9-14. Transmitting FSK/HDLC Signals

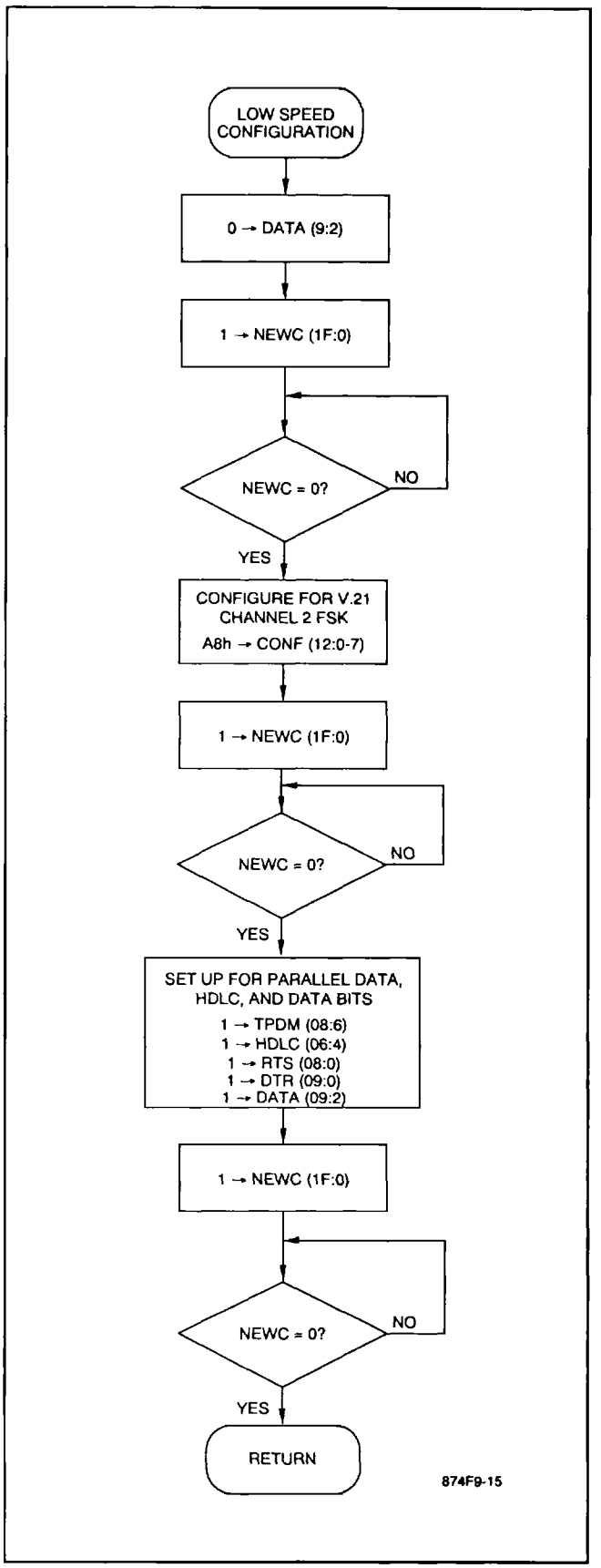


Figure 9-15. Low Speed Configuration Routine

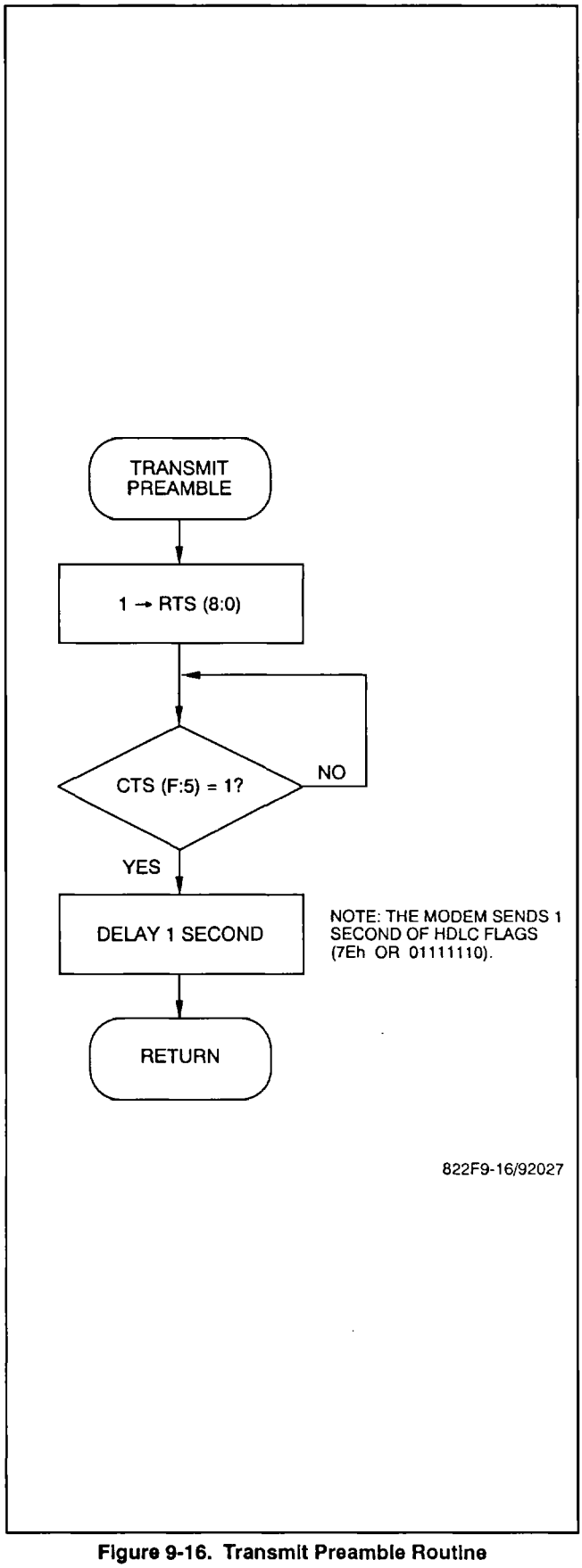


Figure 9-16. Transmit Preamble Routine

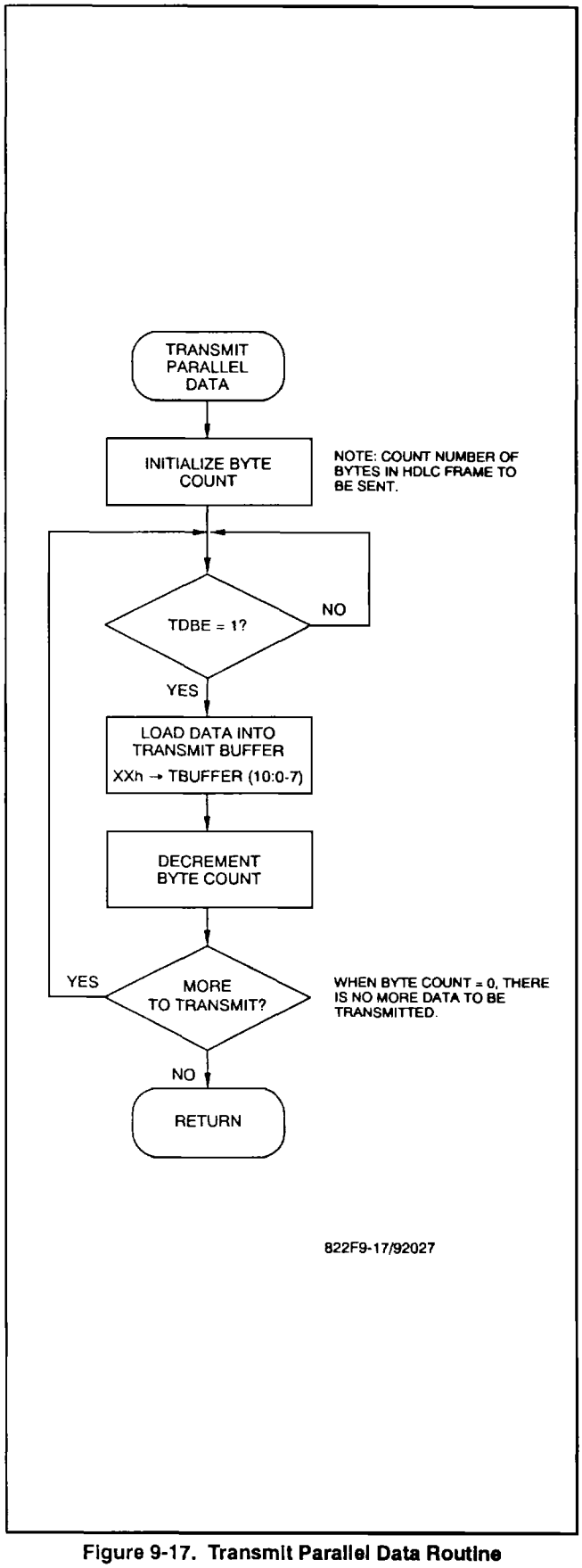


Figure 9-17. Transmit Parallel Data Routine

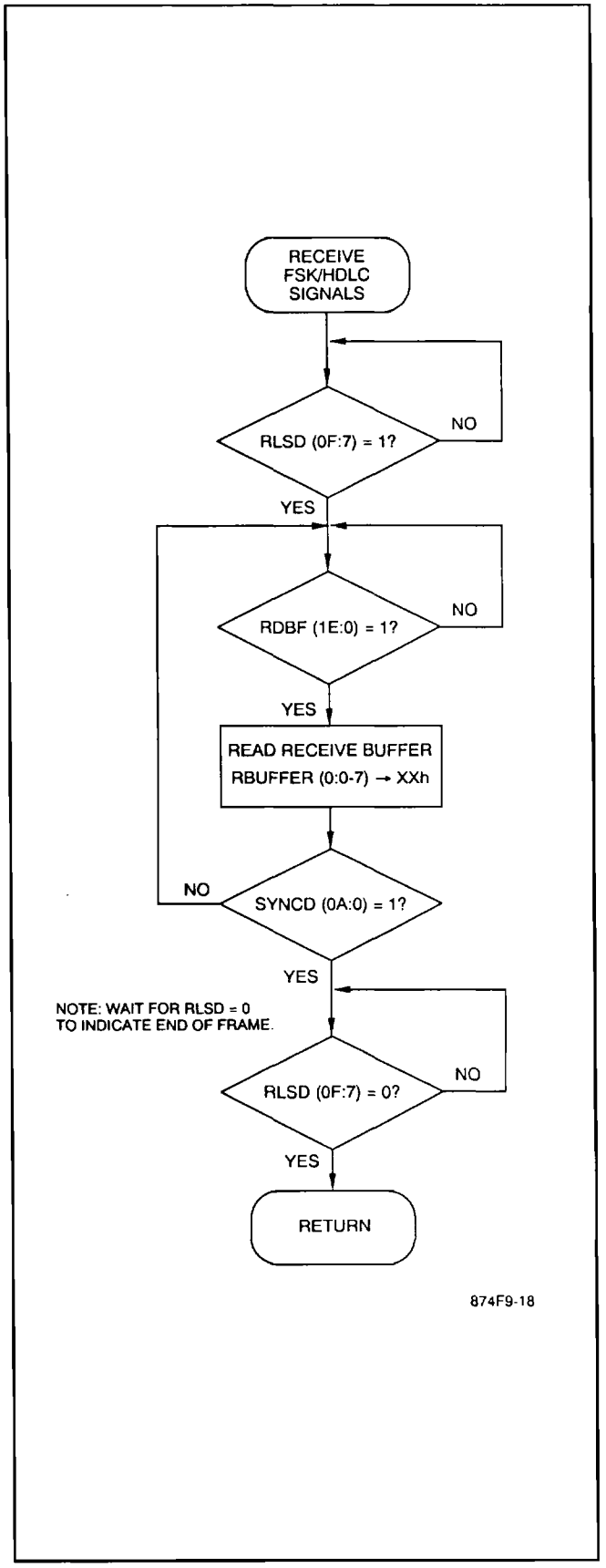


Figure 9-18. Receive FSK/HDLC Signals

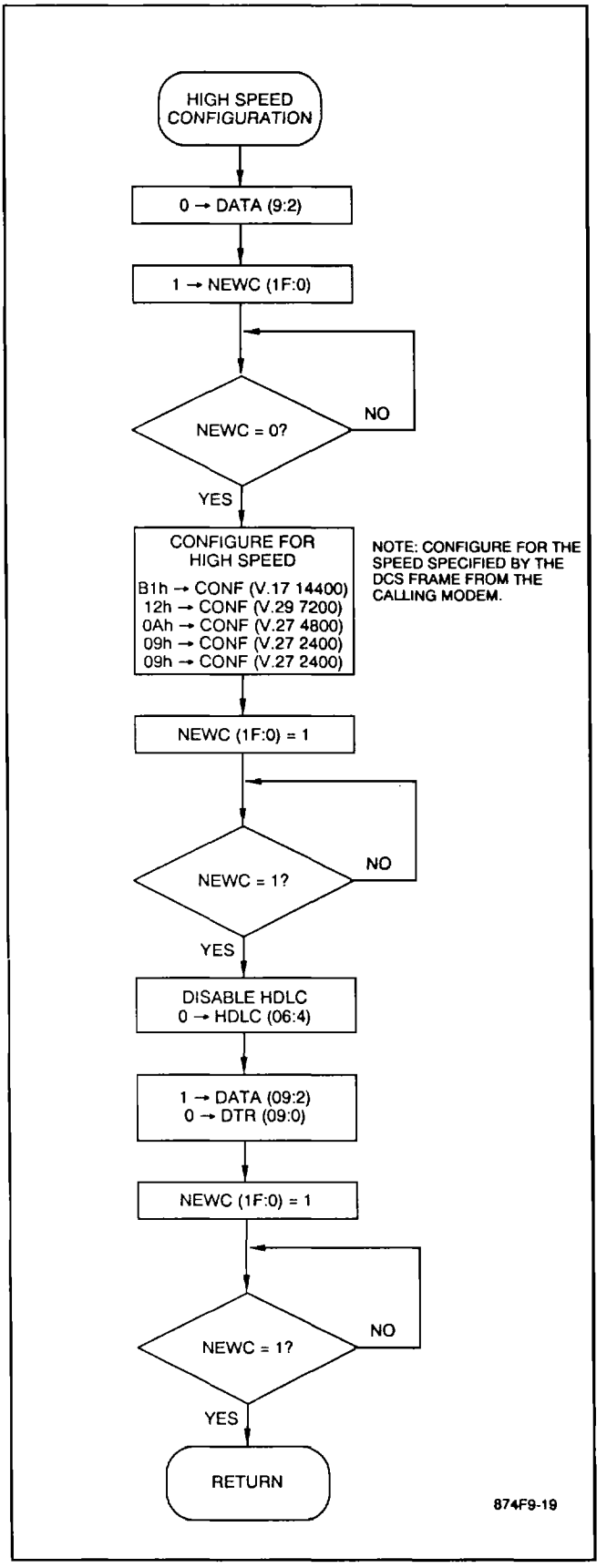


Figure 9-19. High Speed Configuration Routine

9.2.2 ECM Frame Structure

In Error Correction Mode, one frame of facsimile data consists of 256 or 64 octets of data. Each page may contain 1 to 256 frames. Also, 1 to 256 pages may be transmitted. The ECM frame structure is illustrated in Figure 9-22. Following the high speed training sequence, the flag, address field, and control field is transmitted. In ECM, Flag=7E, Address=FF, and Control=B0. The Facsimile Control Field for the Facsimile Coded Data block (FCD) is 60. The frame number follows the FCF for FCD, followed by the facsimile data. Pad bits such as EOL, Tag, and Align bits follow the facsimile data. Finally, the FCS check and the ending flag is transmitted.

After 256 frames, a Return Control for Partial page (RCP) block is transmitted three times. The RCP block consists of the same Flag, Address Field, and Control field followed by the FCF for RCP. The FCS immediately follows with the ending flag. After the third RCP, a maximum of 50 ms of flags are transmitted.

An ECM message protocol example is shown in Figure 9-23. The bold arrows are high speed transmissions and the other arrows are FSK transmissions. The example is self-explanatory. If more information is needed, refer to the T.30 ECM specification.

In this paragraph, the Q refers to the NULL, EOP, MPS, or EOM Facsimile Control Field commands. The Partial Page Signals (PPS-Q) and Partial Page Request (PPR) frame structures are shown in Figure 9-24. The PPS-Q frame begins with the same Flag, Address field, and Control field. Two FCF commands follow. The first FCF transmitted is to indicate PPS. The second FCF is either NULL, EOP, MPS, or EOM. The page count followed by the block count, followed by the total number of frames in the block are transmitted next. The FCS and ending flag are finally transmitted.

The PPR frame structure also begins with the same Flag, Address, and Control field. The FCF for PPR is the next octet. The FIF consists of 256 or 64 bits depending on how many frames were transmitted. The contents of FIF is either a 0 or a 1. The bit number corresponds to the frame number and a 0 indicates the frames was received correctly and a 1 indicates an incorrect frame was received.

9.3 SIGNAL RECOGNITION ALGORITHM

A method of determining whether a high speed message or FSK handshaking is being received by the modem is necessary when implementing the T.30 recommendation. When the calling unit transmitter and called unit receiver configure for V.29 or V.27 ter, sometimes the high speed message may not be received (typically due to a noisy line). In this case, the calling unit transmitter will try to send the message up to three times before re-negotiating in FSK signalling. The called unit receiver must, therefore, be able to distinguish between a high speed message and FSK handshaking.

The algorithm shown in Figure 9-25 can be used to perform the signal recognition. The use of the P2DET and PNDET status bits may also be incorporated for qualifying high speed PSK carrier.

High speed PSK reception in high noise environments can be optimized by setting the RTH bits so that the level of the noise is below the modem's receiver threshold. This can be accomplished by measuring the received signal level via the AGC gain word RAM access while receiving the V.21 channel 2 carrier. Then, after configuring to a high speed configuration, RTH should be set to a value which will provide a threshold range centered around the expected receive level.

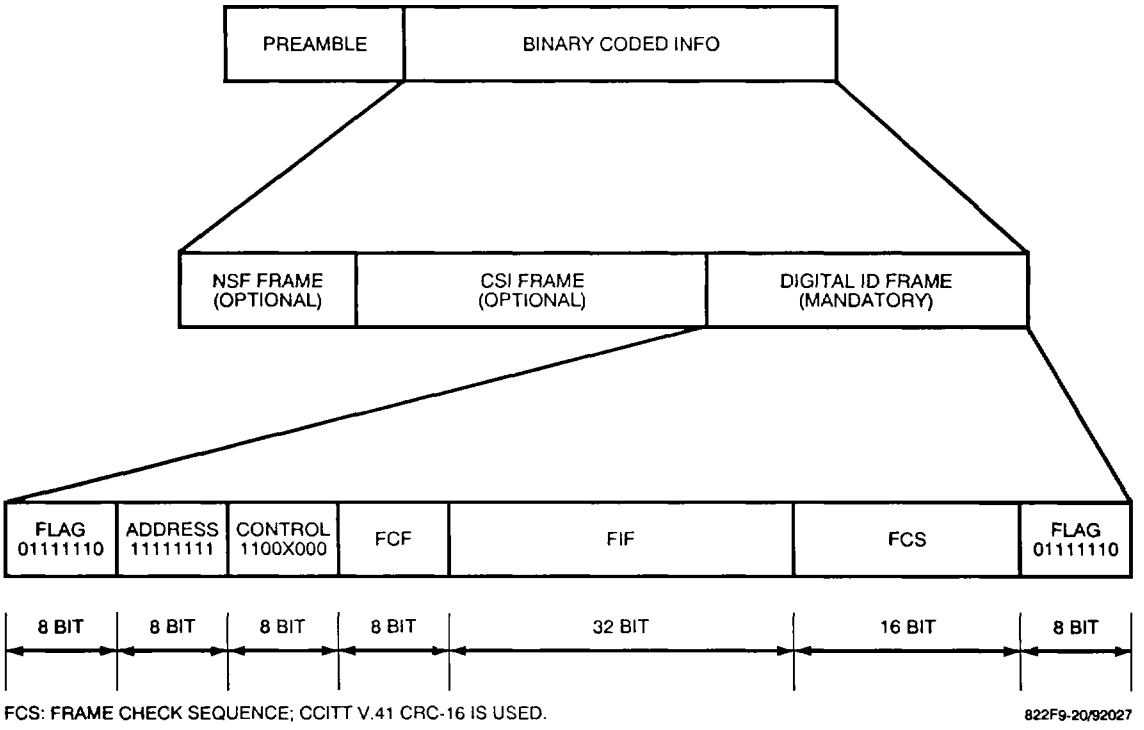
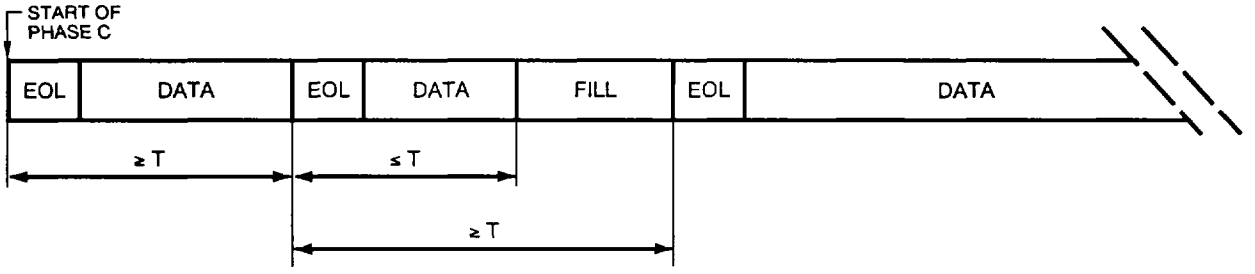


Figure 9-20. HDLC Frame Structure

RETURN TO CONTROL (RTC) INDICATING END OF DOCUMENT TRANSMISSION
FORMAT: SIX CONSECUTIVE EOLS.



T MINIMUM TRANSMISSION TIME OF A TOTAL CODED SCAN LINE.

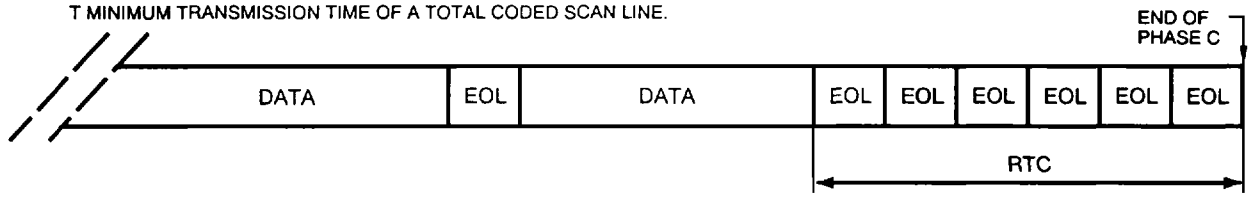


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Figure 9-21. Phase C Format

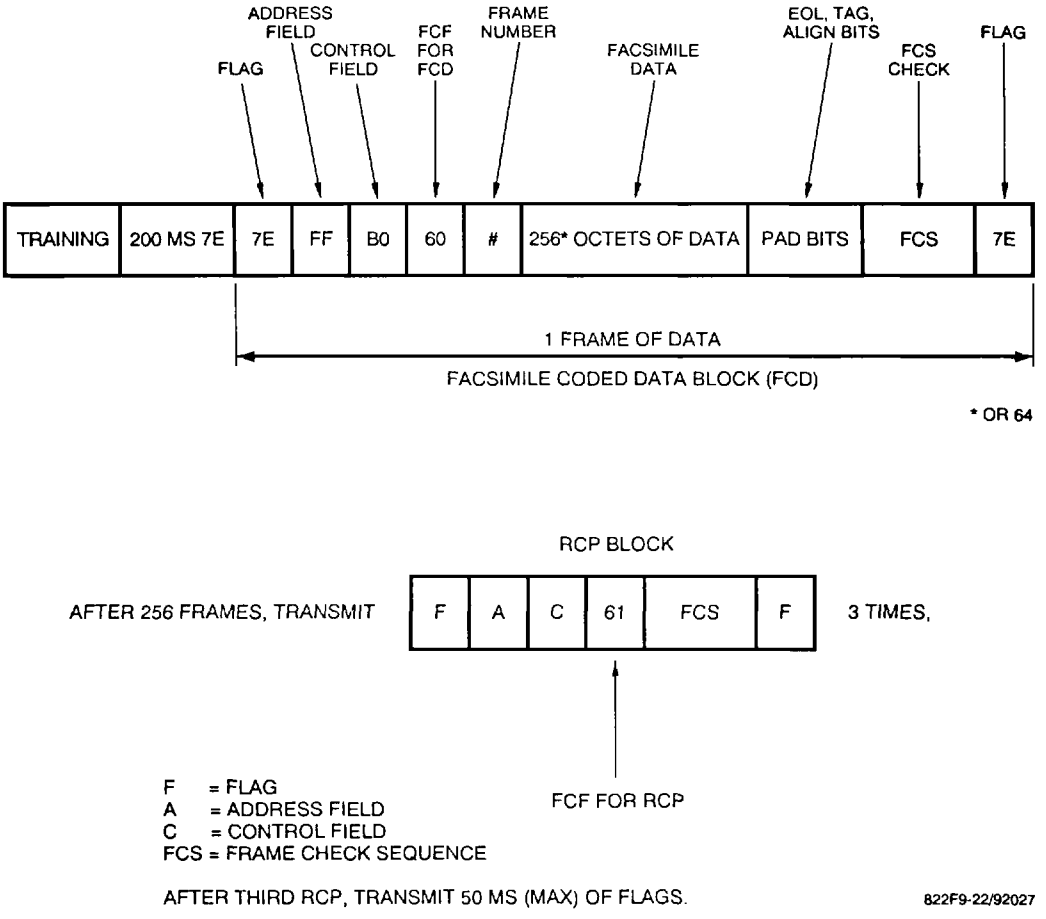


Figure 9-22. ECM Frame Structure

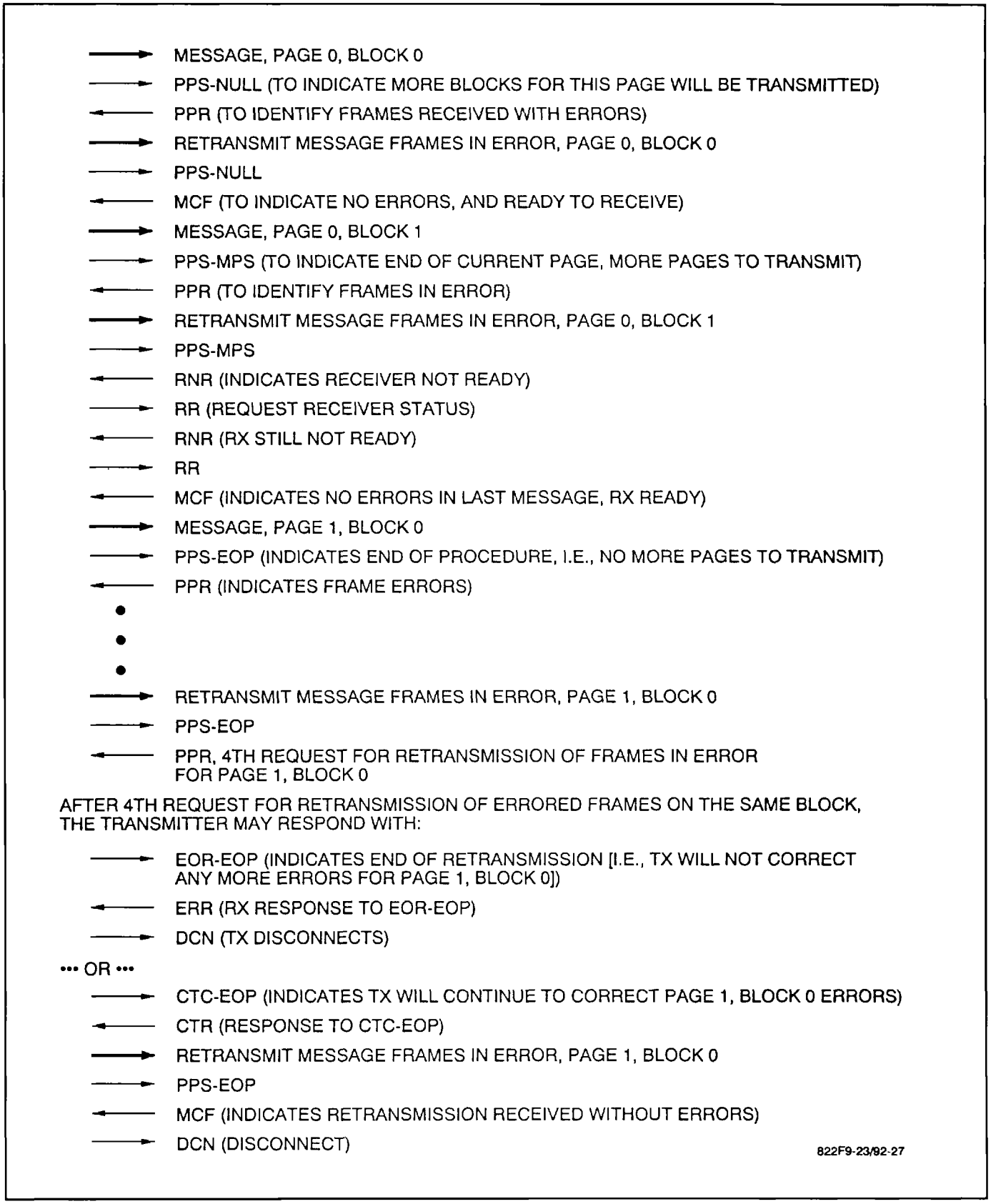
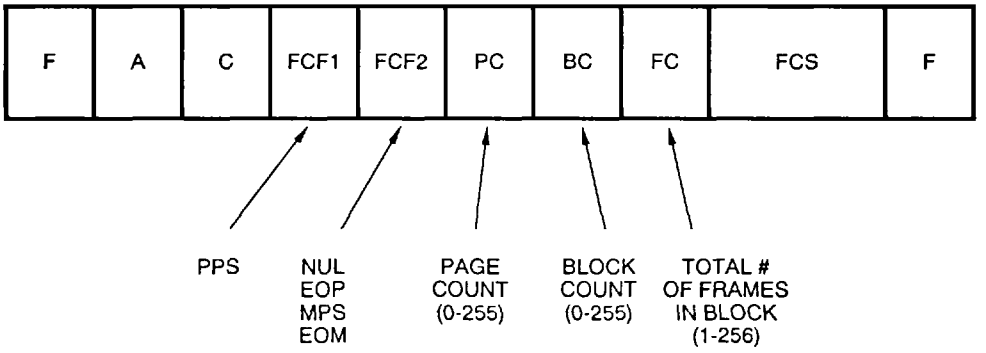


Figure 9-23. ECM Message Protocol Example



FSK 300 BPS

F = FLAG
A = ADDRESS FIELD
C = CONTROL FIELD
FCS = FRAME CHECK SEQUENCE

PPR FRAME STRUCTURE

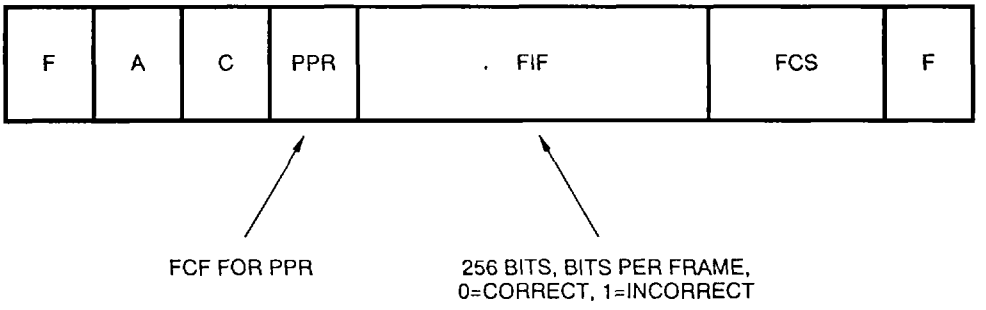


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Figure 9-24. PPS and PPR Frame Structure

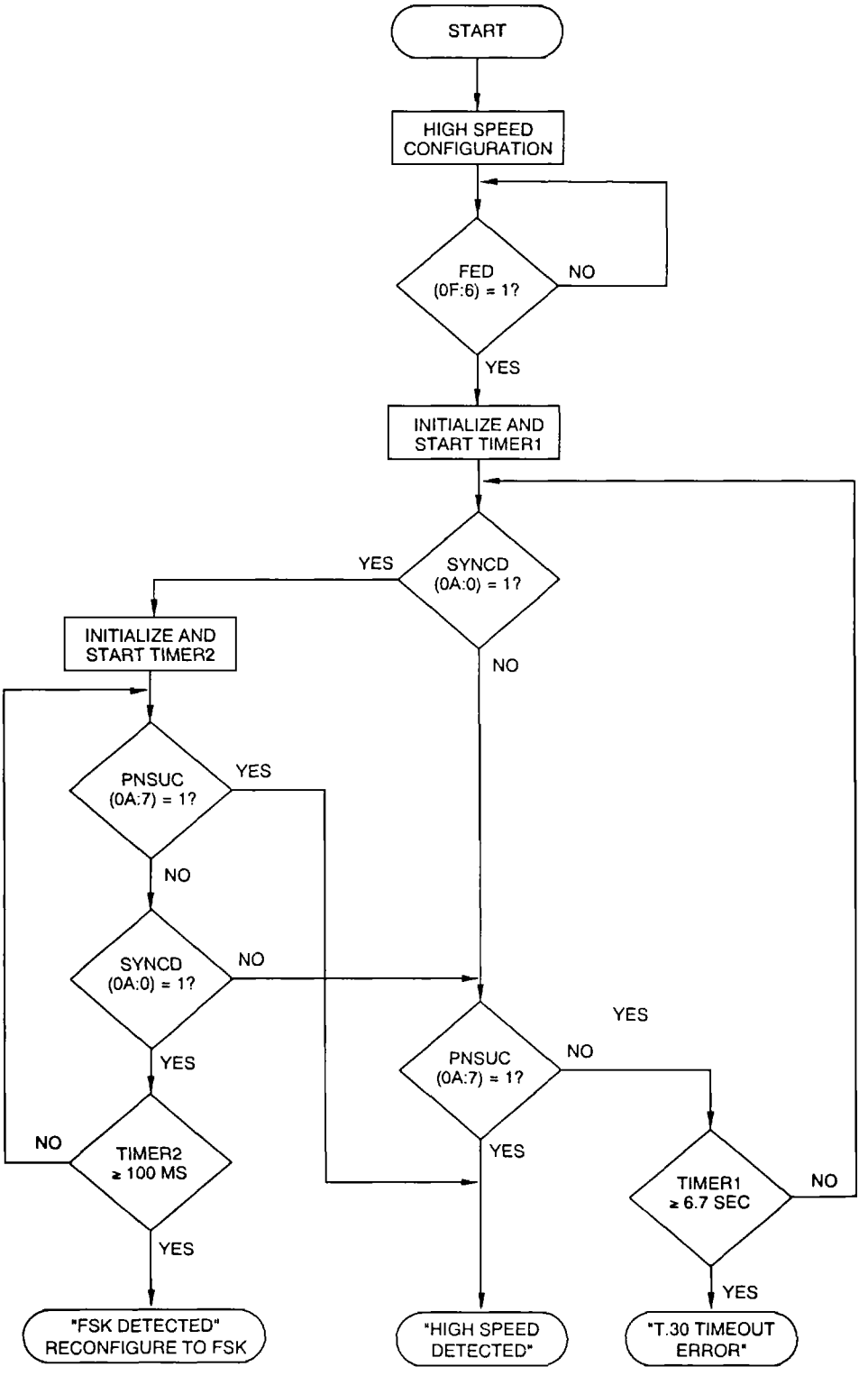

Figure 9-25. FSK Signal Recognition Algorithm